**Minutes of the BM@N STS DAQ meeting 06.07.2018**

Present: Dmitrii Dementev (VBLHEP JINR), Wojciech Zabolotny (WUT), Anatoly Kolozhvari (VBLHEP JINR), Christian Joachim Schmidt (GSI, Darmstadt), M.Shitenkow (VBLHEP JINR), Vladimir Sidorenko (KIT), Ilya Slepnev (VBLHEP JINR)

Integration of the CBM-like readout chain of the STS in the DAQ system of BM@N experiment was discussed. The following aspects were stated:

1) Timing system of BM@N experiment is based on White Rabbit network. Supported frequencies are 125 MHz and 125/3 MHz. There is no 40 MHz clock, which is used in CBM. Two different options for STS were suggested:

* To run at 125 MHz and link speed of 5 Gb/s instead of 4.8 Gb/s (still problems with PPS)
* To install additional time receiver and create a time base with 40 MHz

The second option is preferable because the same codes for BM@N and CBM will be used. For the TFC system board-level jitter cleaning should be implemented.

2) Integration of the self-triggered STS electronics in the triggered BM@N experiment was discussed. Current bandwidth of the BM@N DAQ is 1-5 GB/s. SSD storage network has much higher bandwidth, but capacity is limited. Probability of using a ring buffer for the data storage before receiving of a trigger decision was discussed. Alternative solution is to use embedded computers for that. Probably it will be feasible to use DRAM for buffering.

Trigger latency for BM@N is ~1 µs. There is also a low-level trigger with a latency of 200 ns. Probably it should be possible to store the data for the latency of low-level trigger, but still problems with unsorted data.

3) UPnP is used in BM@N for the board identification, DHCP for IP assignment. RARP used in IPbus control system currently is not supported. STS group can organize separate network segment.

STS group have to implement kernel driver for the PCIe cards.

Also during the readout session susceptibility of the GBTxEMU boards to the SEUs was discussed. Can be tested at mCBM.