Karlsruher Institut für Technologie

The 3-d Mini Work Meeting “Making-up a Work Plan for building hybrid DSSD-GEM Tracking System for the BM@N-2”
5-6 July 2018

TFC Development Status

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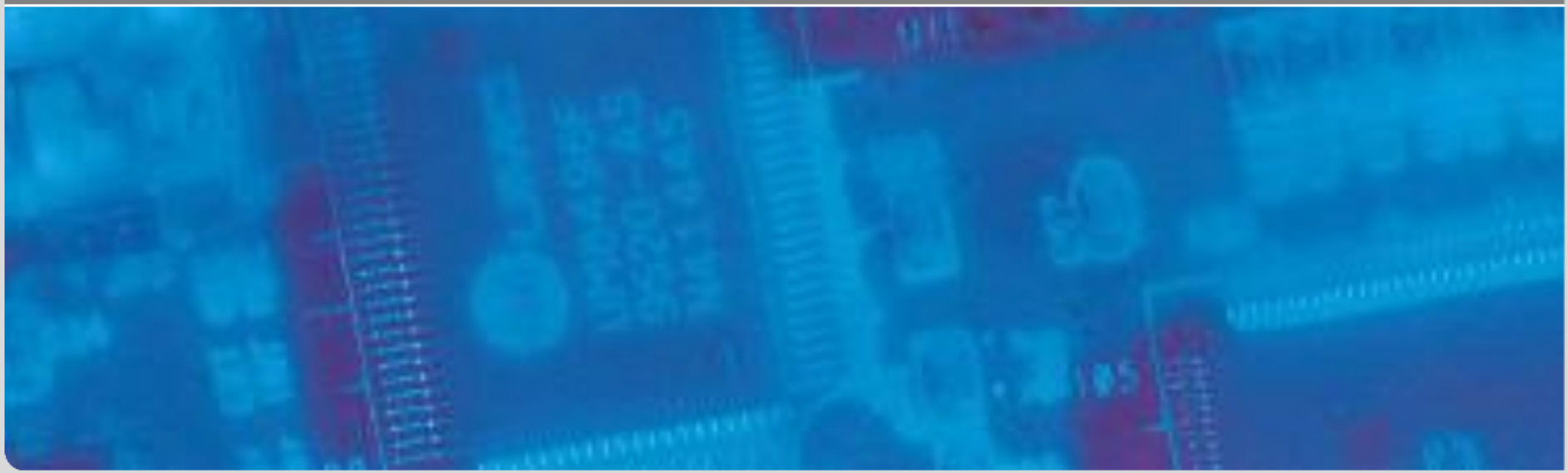


TFC system

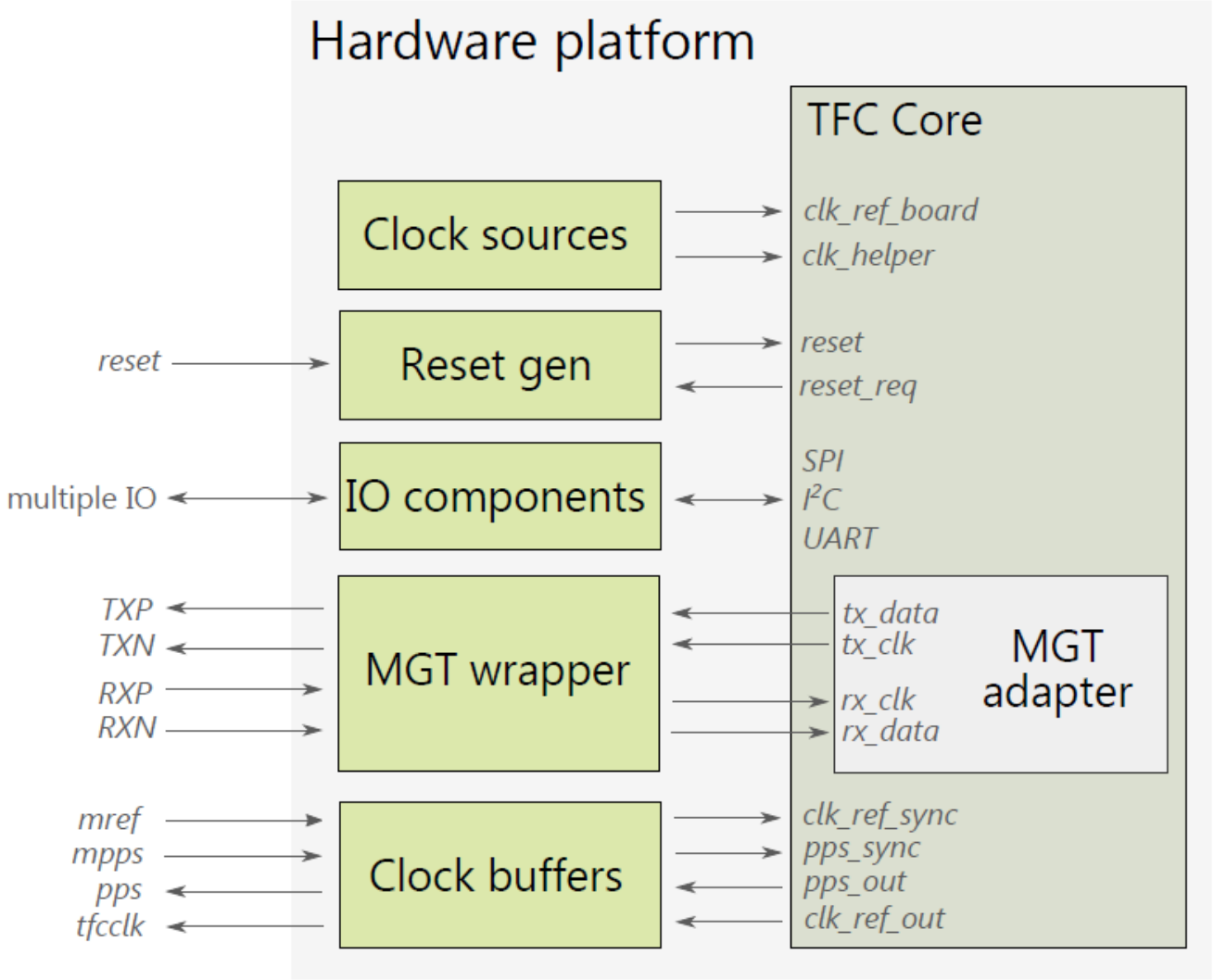
Goal:

- Clock distribution to FEE
- Synchronization of data processing (timestamp assignment, framing, transmission) with the master clock
- Time-deterministic command interface with a defined (if any significant) delay

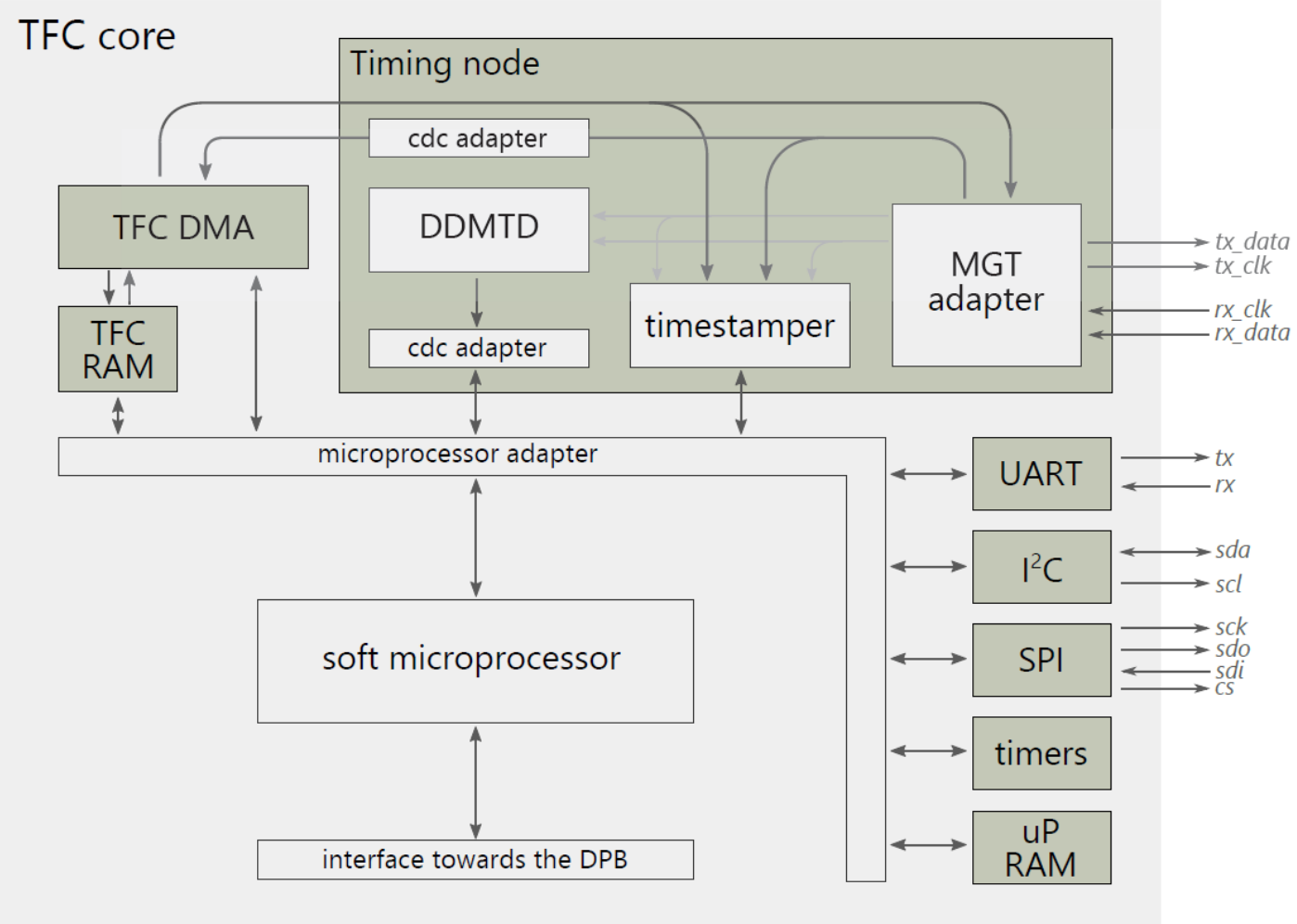
Features:

- Clock period alignment
- Sub-clock phase alignment
- Phase/frequency unlock detection
- Same hardware structure used on both the master and the slave sides

Hardware structure

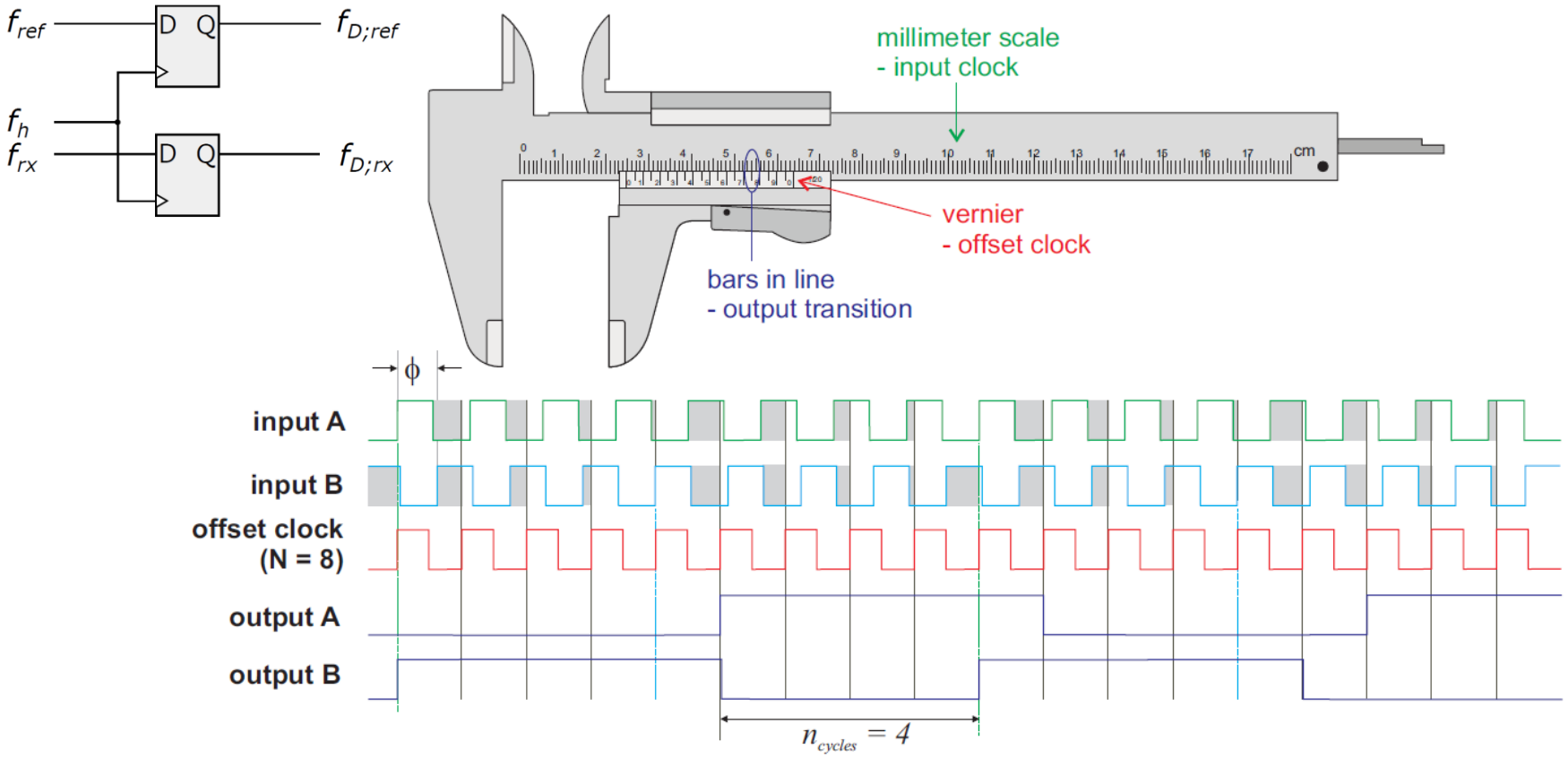


Hardware structure



DDMTD

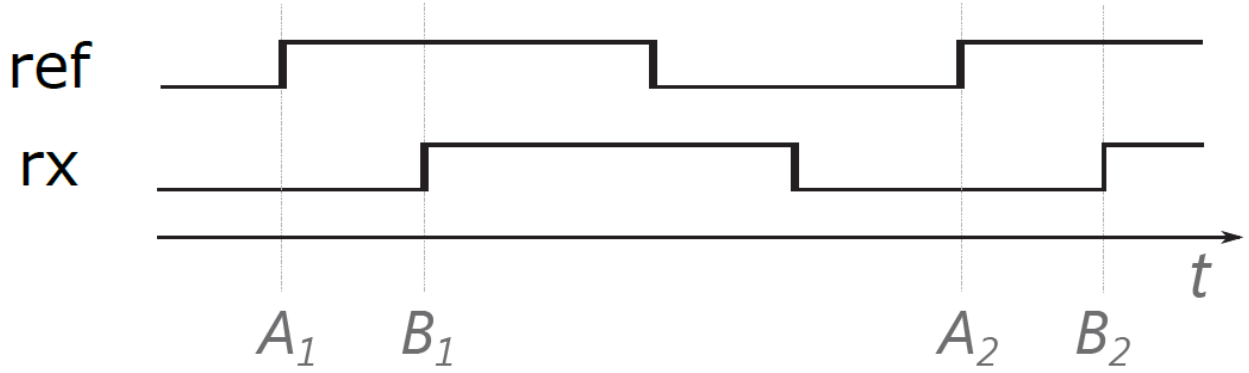
$$f_h = \varepsilon \cdot f_{\text{ref}} = \frac{2^N - 1}{2^N} \cdot f_{\text{ref}}$$



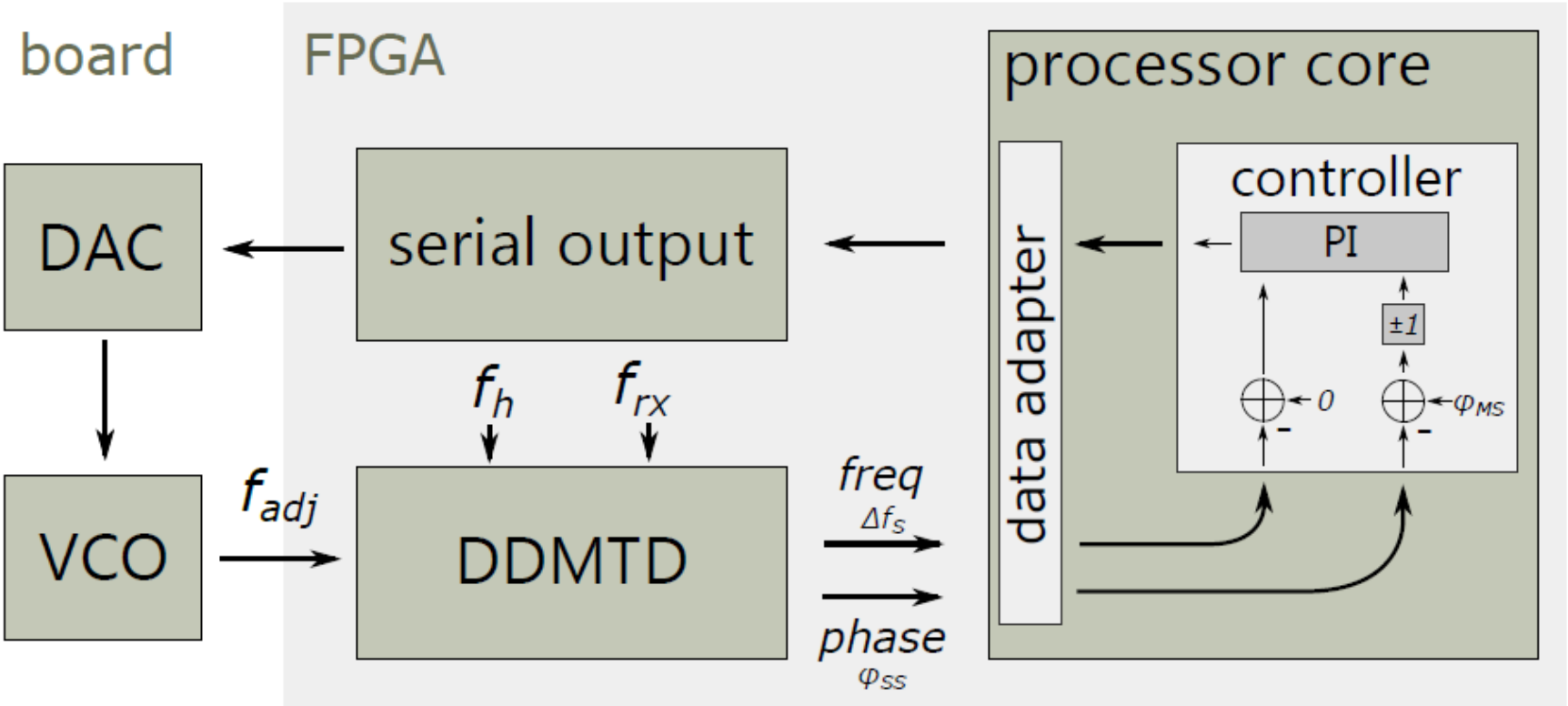
Tomasz Włostowski - Precise time and frequency transfer in a White Rabbit network

DDMTD

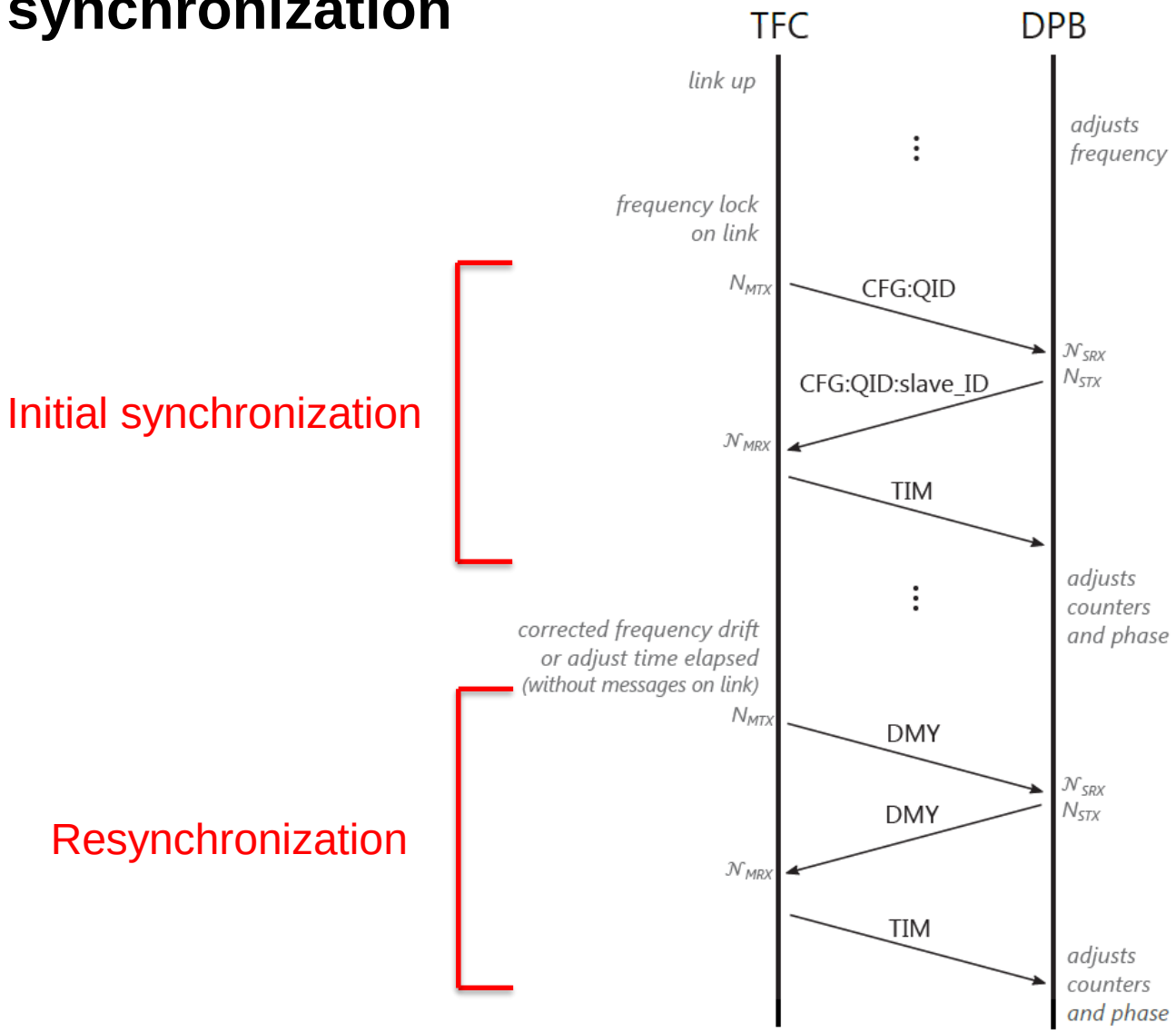
- [B2 – B1] is stable and equals [A2 – A1]
  -> calculate *phase offset* [B1 – A1]
- [B2 – B1] does not equal [A2 – A1] or is unstable
  -> calculate *frequency offset*
- [A2 – A1] is unstable
  -> helper signal frequency mismatch



Soft-PLL

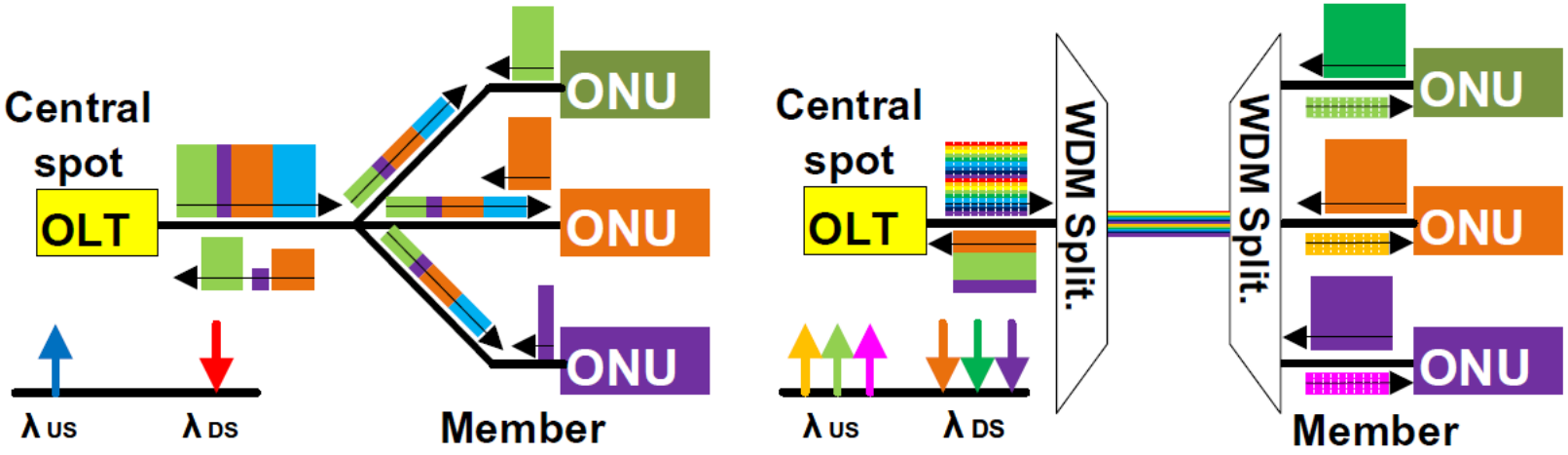

board
FPGA
processor core
DAC
serial output
data adapter
controller
PI
±1
0
φMS
fh
frx
fadj
VCO
DDMTD
freq
Δfs
phase
φss

Link synchronization



PON – a subject to research

- Usage of a passive optical network (PON) might be a way to improve TFC links concentration ratio at the cost of latency



Further steps

- Reproduce previous evaluation results
- Upgrade the projects to a newer Vivado version
- Adapt the design for Xilinx UltraScale+ devices used in the newly proposed CRI platform
- Increase the number of TFC links for use on the master side