FPGA and firmware solutions for the system

Wojciech M. Zabołotny

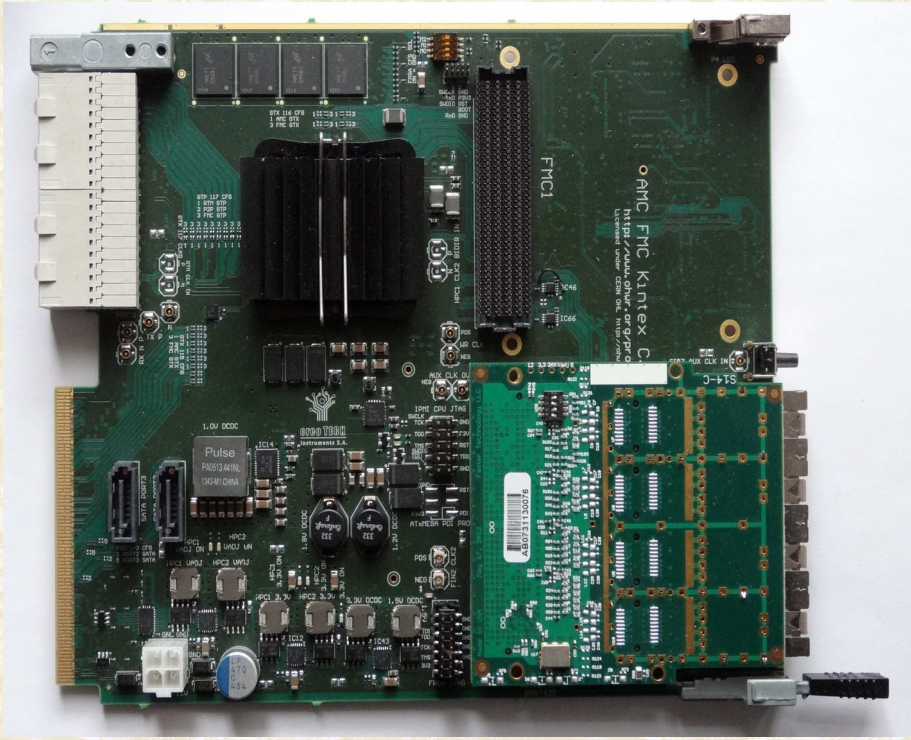
Institute of Electronic Systems, Warsaw University of Technology

Introduction – our CBM involvement

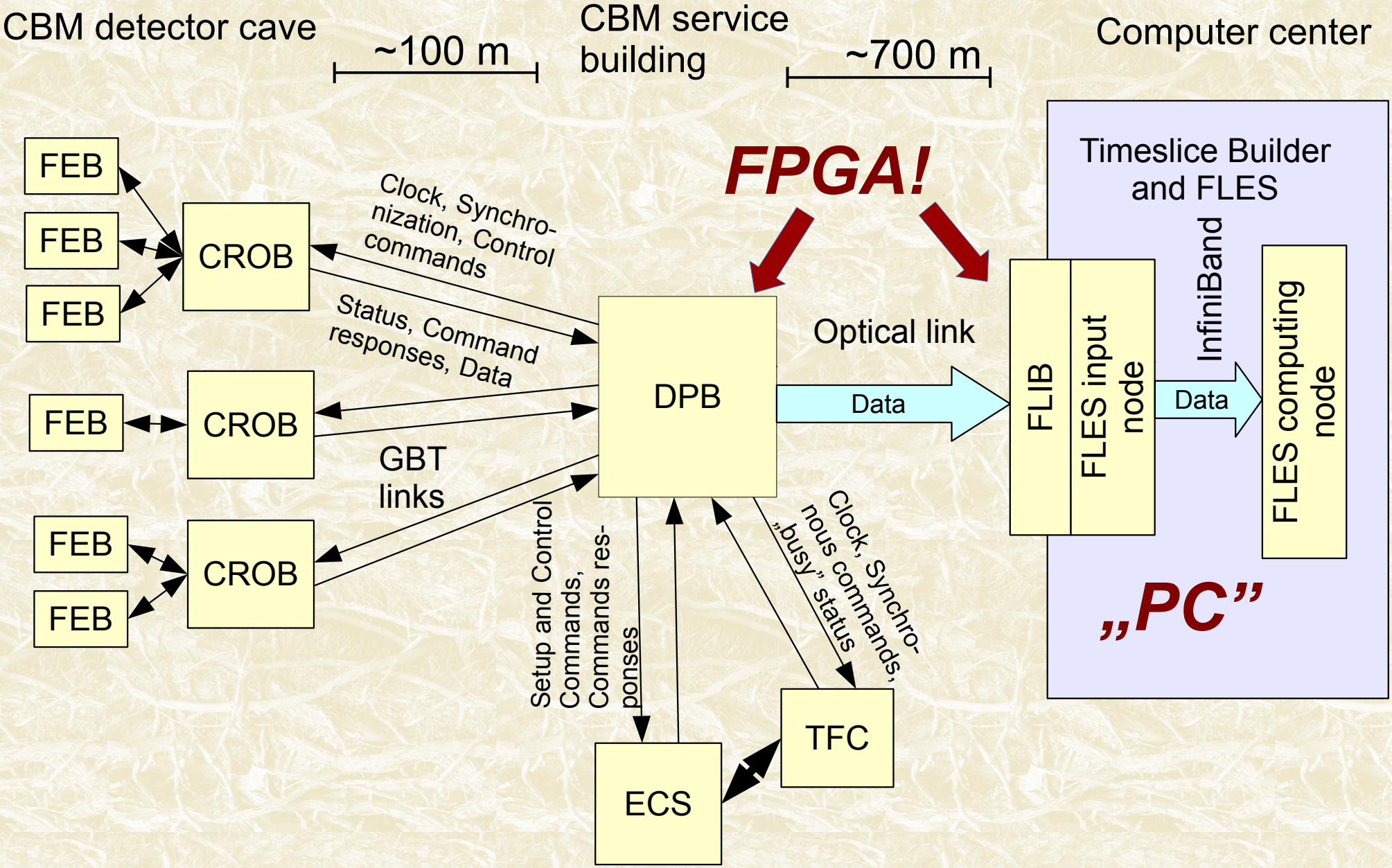
- Our team is involved in development of firmware for CBM readout.
- We have participated in development of AFCK – the hardware platform used for prototyping of the readout chain.
- We have prepared the firmware framework implementing the core functionality of the DPB boards.
- We are involved in the development of the CRI firmware

AFCK – main prototyping platform

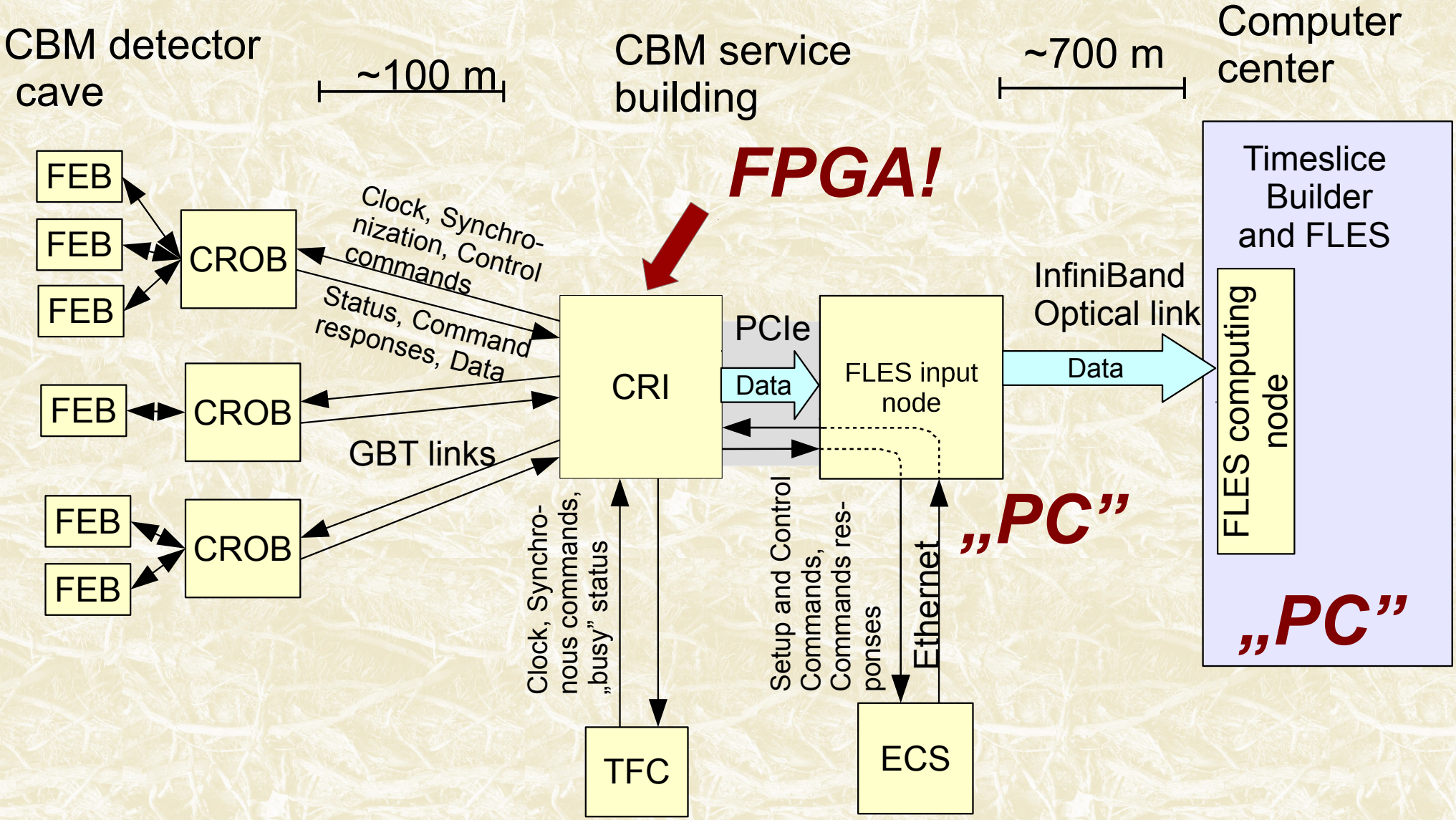
- Prototype board with Kintex-7 325T FFG900 FPGA
- Ready for MTCA crate but usable in stand-alone mode
- Flexible routing of MGT links
- Flexible clock matrix and Si570 VCXO



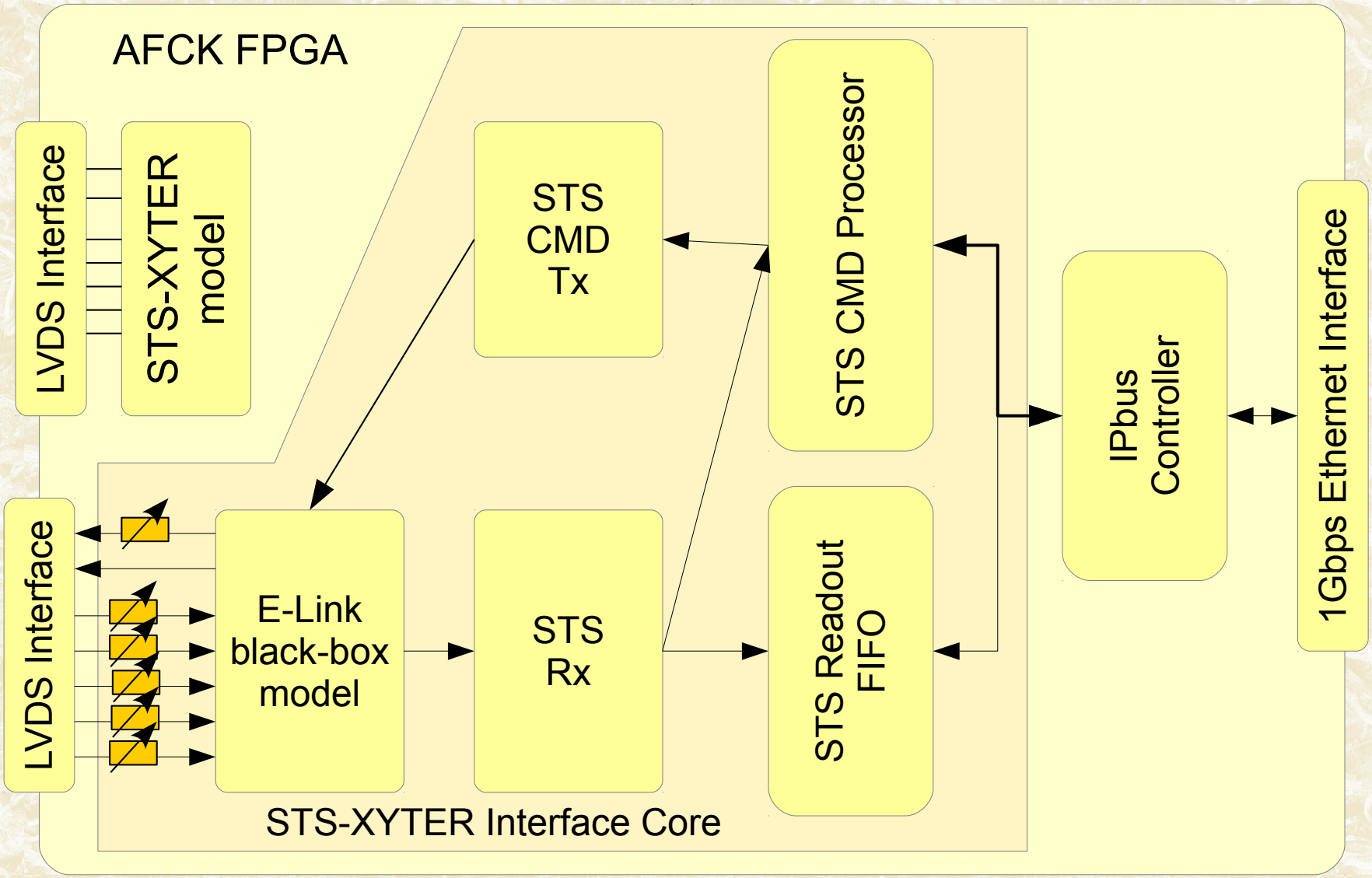
DPB-based concept of the CBM readout



CRI-based concept of the CBM readout



STS-XYTER tester and model



IPbus as a control interface

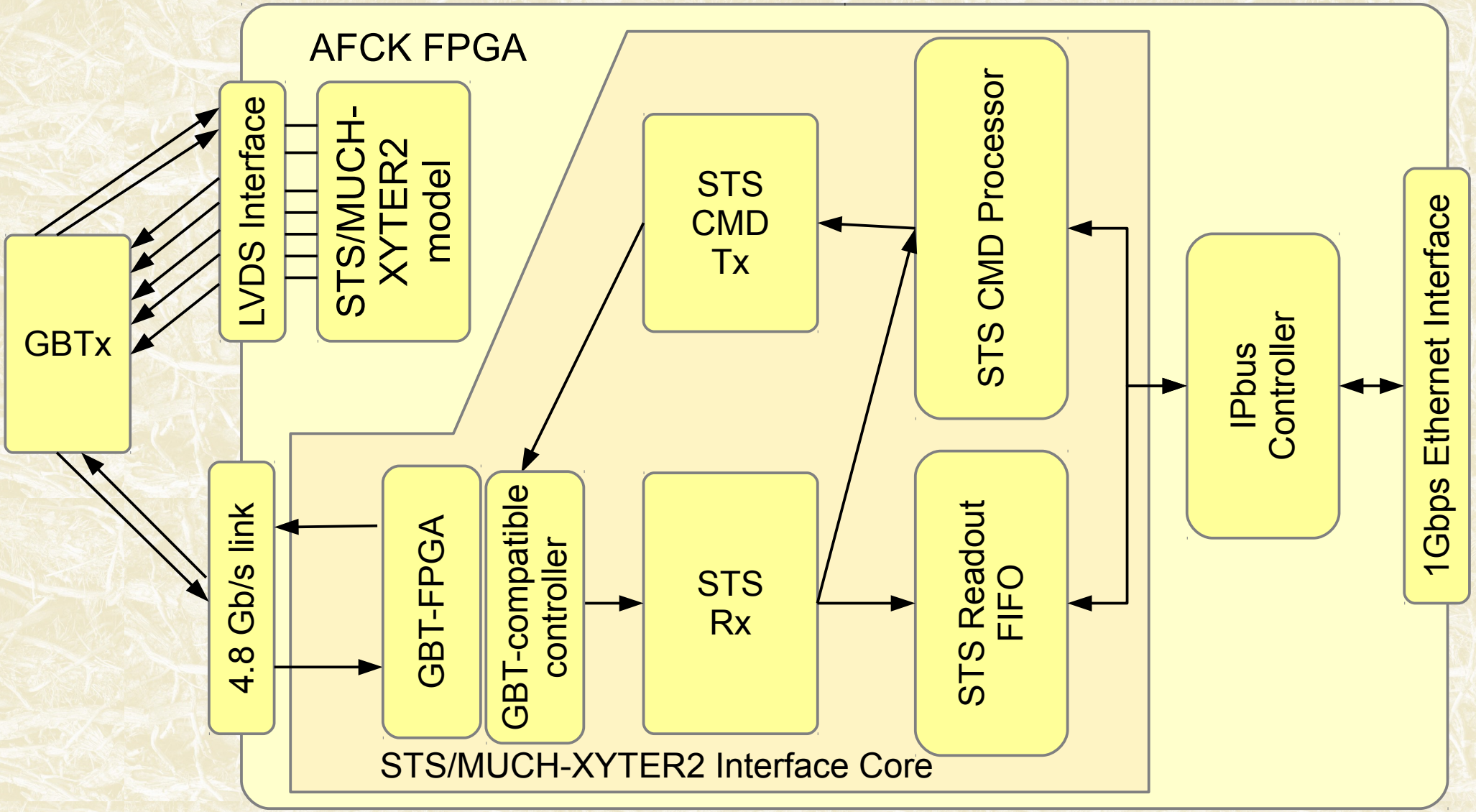
- The IPbus has been used as a control interface for the DPB firmware
  - Supports Python for quick development and interactive testing
  - Supports C++ for easy development of high-performance production-quality final software
- For more complex designs it was necessary to support IPbus with scripts for automatic generation of address tables.

STS-XYTER from FW point of view

- Necessity to synchronize the E-Links – adjustment of clock phase and input data to assure reliable transmission.

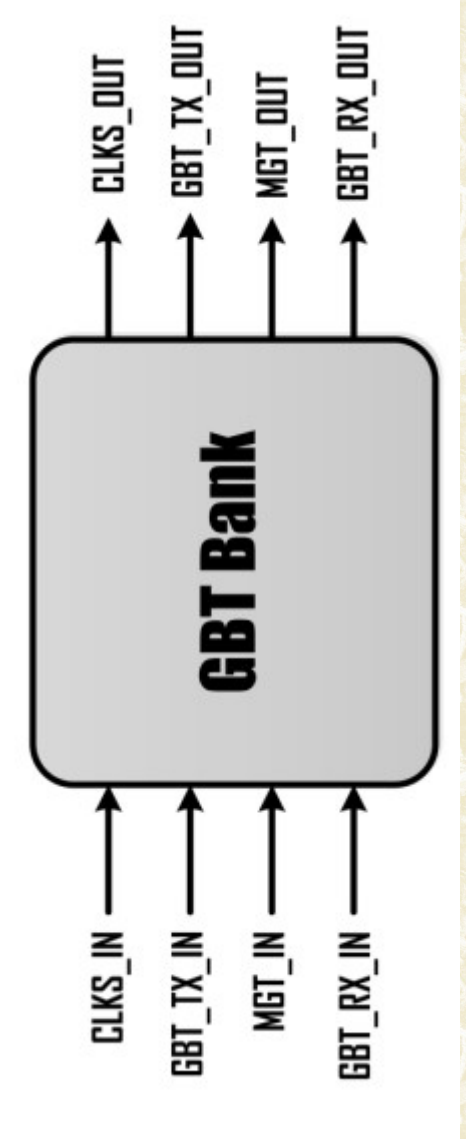
  Special synchronization procedure was developed.
- Need to sort the incoming hit data (because the STS-XYTER may send data out of order, due to different channel occupancy and amplitude-dependent hit processing delay)
- Implementation of the special STS command processor allowing to transmit commands to STS-XYTERs and receive confirmations/responses
- Implementation of special mechanism for sending of “time-deterministic” commands.

GBT-compatible STS-XYTER tester



GBT-FPGA IP-core

- Communication with GBTX requires integration of GBT-FPGA IP-core (provided by CERN).
- The core is offered for various FPGA architectures, however for Artix-7 and UltraScale+ porting is necessary.
- Small adjustments are usually needed to utilize the core in the User's firmware.

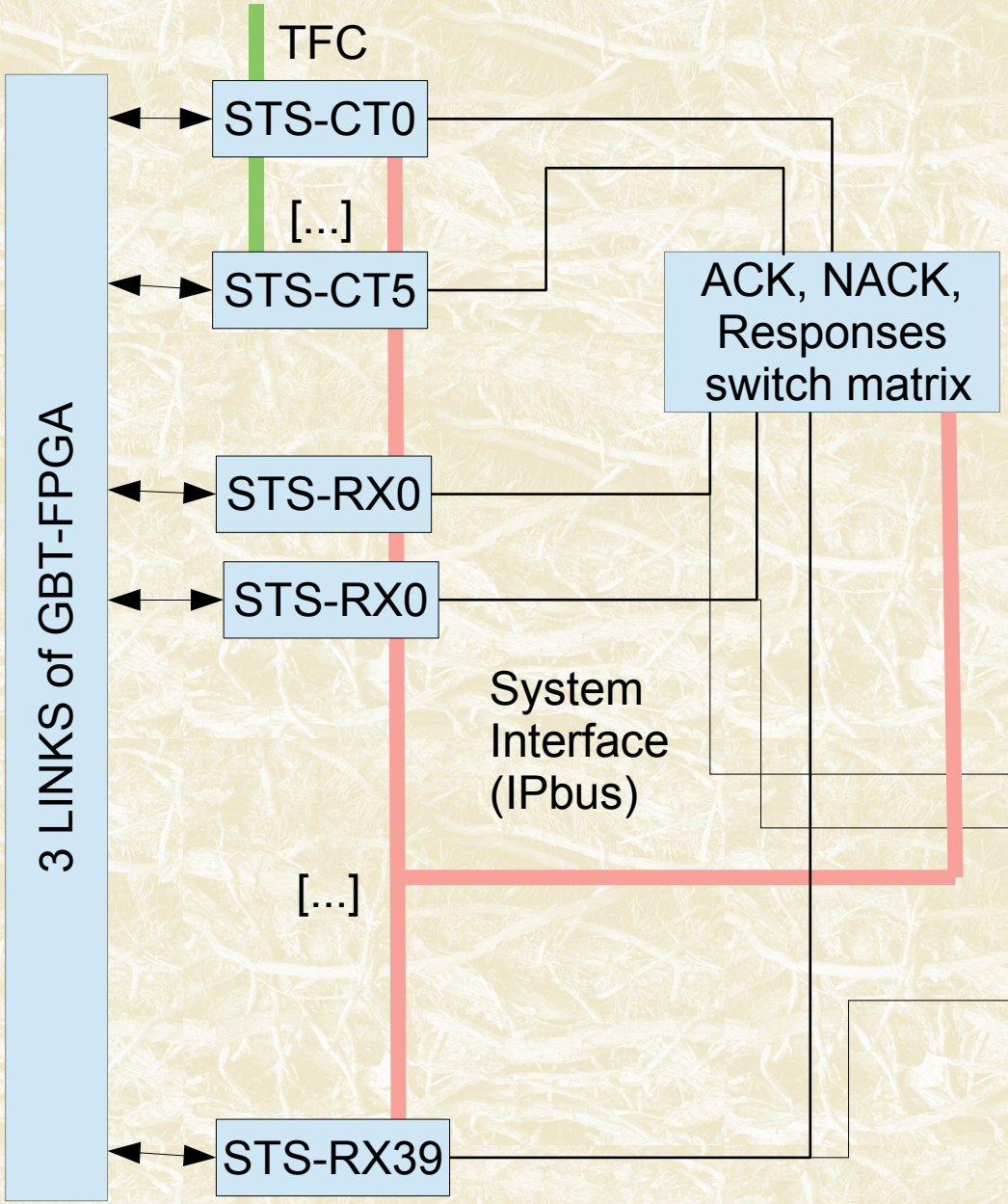


Source: GBT-FPGA User Guide

GBT as an intermediate node

- Addition of GBTX support eliminated the necessity to implement the E-Link phase adjustment (it is done in GBTX itself)
- It was necessary to add IP-cores able to control the GBTX (in fact 3 GBTXes – one master and two slaves in the CROB3 board)
- The GBTX handles the data in GBT frames transmitted at 40 MHz rate. Therefore for 160 MHz downlinks it was necessary to repackage the STS frames into 4-bit chunks. Similarly, the data received at 320 MHz are delivered in 8-bit chunks.

CROB controller in GBT-based DPB

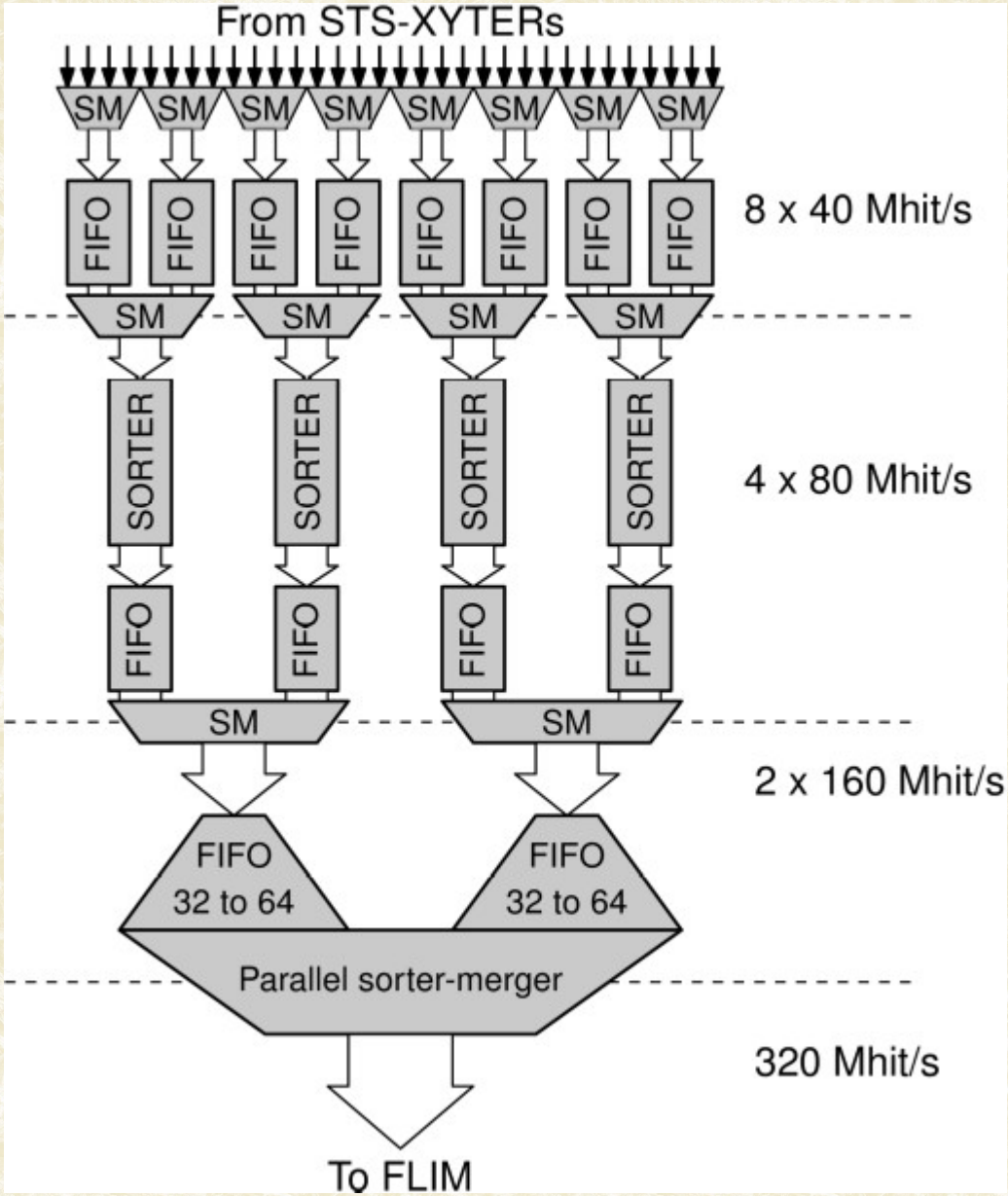


The GBT-based readout uses CROB boards connected to multiple FEB boards with multiple STS-XYTERs. That enforced creation of multilevel complex hierarchy of cores.

Additional complexity results from the fact, that a few STS-XYTERs may be connected to an individual downlink. That requires selective handling of ACKs and responses.

Sorter system

- The hit data received from multiple STS-XYTERs are time sorted and merged.
- The hits are then split into microslices covering the appropriate time periods.
- The microslices are transmitted via FLIM module and 10 Gb/s links to FLES



Current status of the DPB firmware

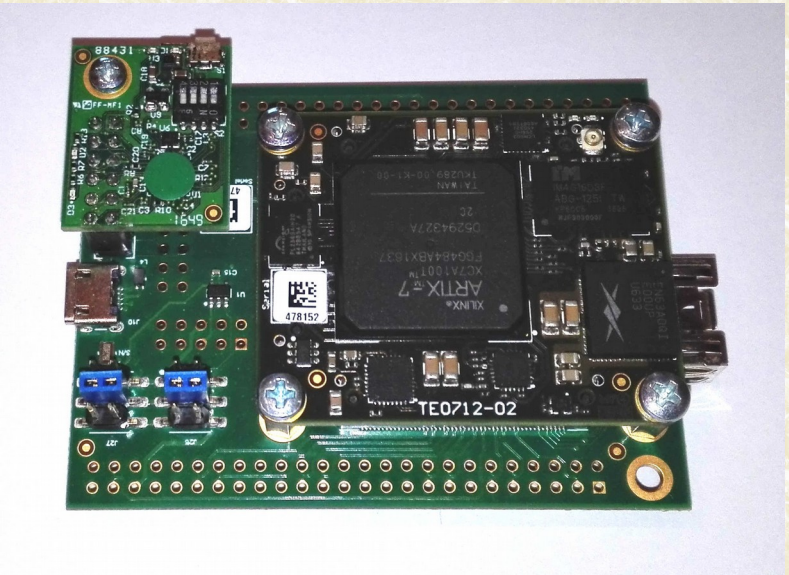
- Two versions of the firmware are ready
  - E-Links based with support for up to 6 STS-XYTERs
  - GBT-based with support for 2 CROBs on AFCK
- IP-cores provided by other teams were integrated (TFC-slave from KIT, FLIM from FIAS, GBT SC controller…)
- Dedicated cores were developed:
  - for control of STS-XYTERs including sending of time-deterministic commands
  - for reception of hit data, including sorting and aggregation of data into microslices
- The firmware is reused also by other CBM subsystems

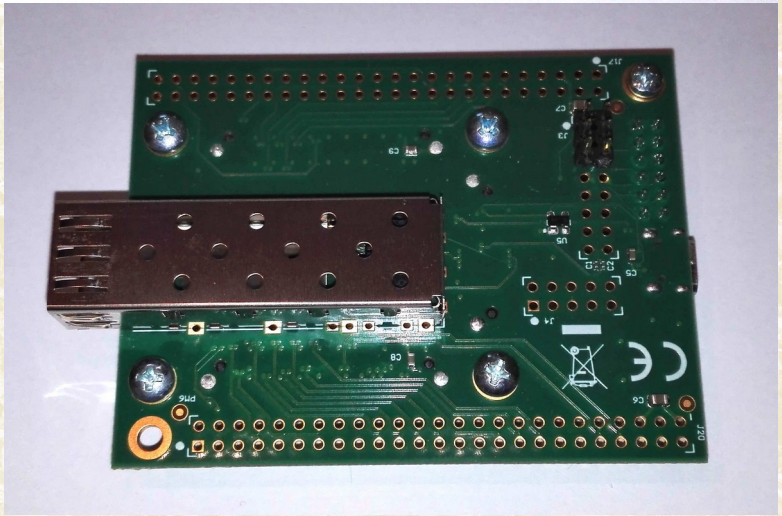
Current developments

- Preparation of CRI
  The PCIe-based data concentrator with newer FPGA – UltraScale or UltraScale+
- GBTx emulator
  The FPGA-based functional replacement for experiments and development in countries where GBTx usage is restricted.

GBTx Emulator (GBTxEMU)

- Aim – emulate the necessary subset of GBTx functionality in a price-optimized way
- Preferrably should be done on Artix 7 platform
- Current development platform – Trenz TE0712-02-100-2C with carrier board TEBA0841
  - 4 GTP (high-performance transceiver) lanes (one SFP+ on carrier board)
  - GTP (high-performance transceiver) clock input
  - 10/100 Mbit Ethernet PHY in RMII Mode with MAC address EEPROM
  - Programmable Low Jitter PLL (Silicon Labs Si5338)





GBTxEMU specification

- Support for 1 or 2 MGT links with 4.8 Gb/s (6 Gb/s if possible) speed
- 48 E-Links with 40 MHz clock and 80 Mb/s data rate (80 MHz clock and 160 Mb/s data rate if possible)
- Control interfaces
  - IPbus via 100 Mb/s Ethernet
  - Additional emulated E-Link (similar to GBTX SC) controlled via MGT link
- Clock recovery
  - Board is equipped with Si5338 chip – similar to the Si571 used in AFCK

GBTxEMU development

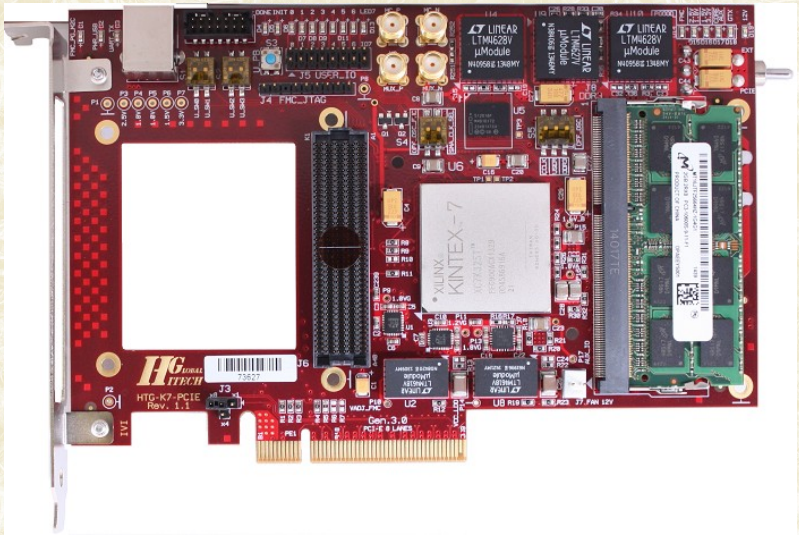
- Port of GBT-FPGA IP-core to Artix 7 platform
  - Possibility of porting the required subset of features must be verified
  - It may be impossible to implement FEC in Artix 7, we may be forced to implement a simpler mechanism (e.g. based on CRC and TR)
  - There is a risk, that a more expensive Kintex 7 FPGA should be used…
- Necessity to simplify the E-Link interface. Full phase adjustment of clock and input data may be not possible.
  - We may need to use the length-matched cables to ensure reliable operation.

GERI proposal

- The basis – The GBT-based DPB firmware prepared for AFCK
- Necessary changes due to usage of GBTxEMU instead of GBTX
- Possible hardware platforms
  - Initially AFCK (AFCK-GERI with output via FLIM to FLIB, or alternatively via FADE-10G to 10Gb/s Ethernet)
  - Finally the HTG-K700 with PCIe output

HTG-K700

- Board based on Xilinx Kintex-7 K325T-2, K325T-3, K410T-2, or K410T-3
- x8 PCI Express Gen 2 through hard-coded PCI Express controller inside the FPGA or Gen3 through soft IP core
- FMC HPC connector with 160 Single-ended (HR I/Os ranging from 1.2V-3.3V) and 8 GTX (12.5Gbps) Serial I/Os.



Source: HighTech Global

Conclusions

- Experience gained during the development of readout chain for CBM may be used for preparation of solutions for BM@N-2 system.
- The firmware solutions for BM@N-2 system may significantly reuse (after necessary adjustments) IP-cores developed for CBM.
- The GBTxEMU (currently developed), and GERI (planned) designs may be core components of the proposed readout system.

Thank you for your attention!