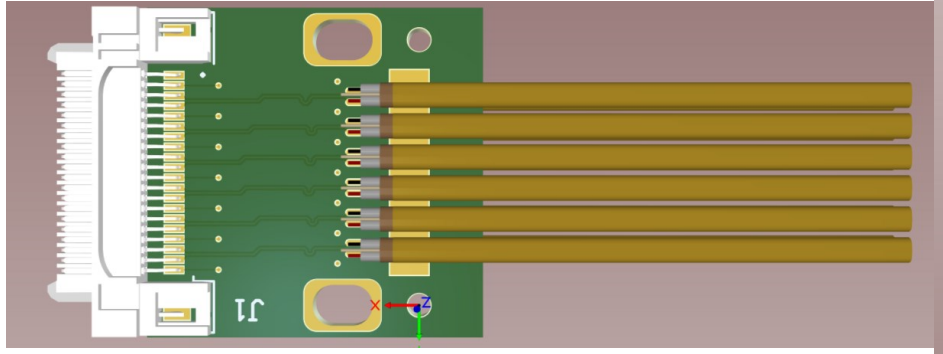
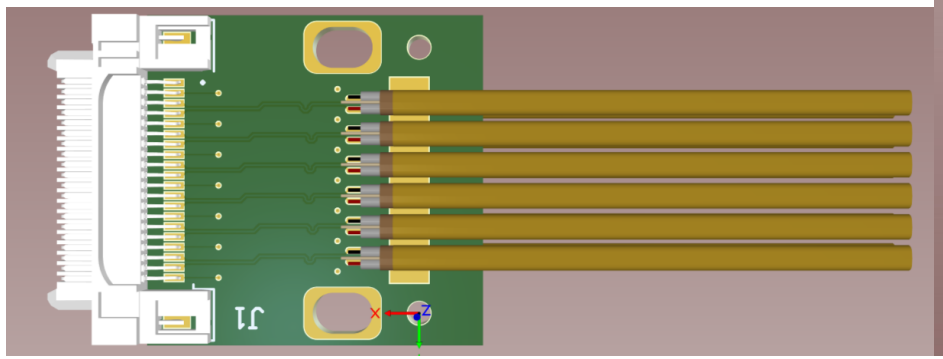
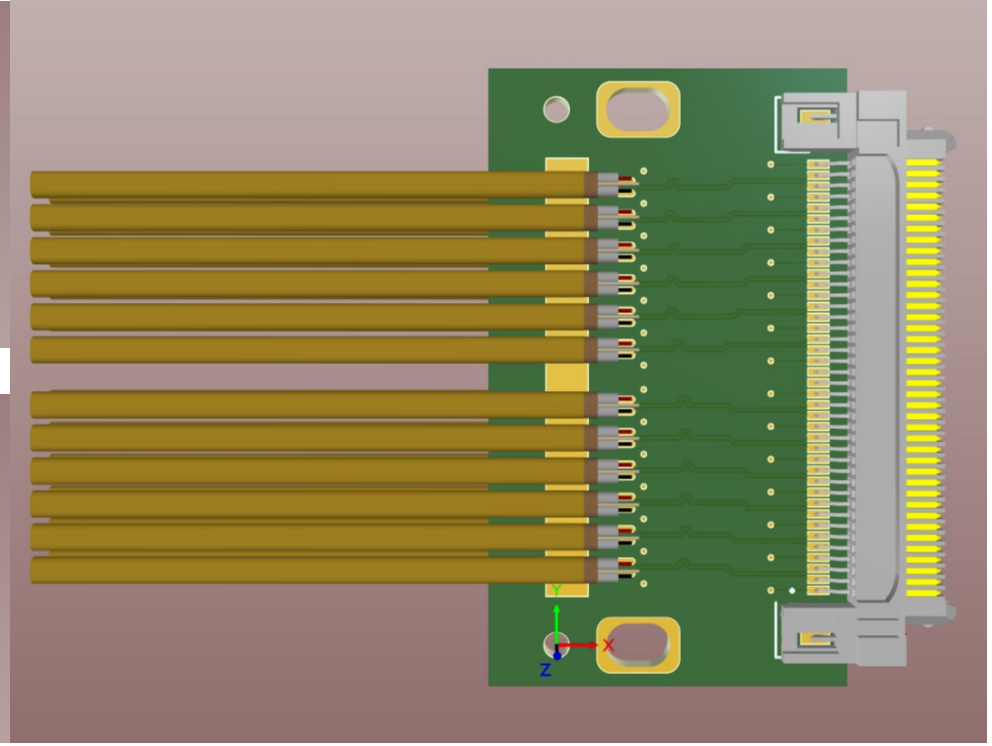
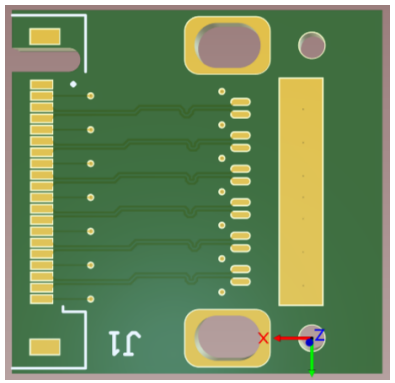
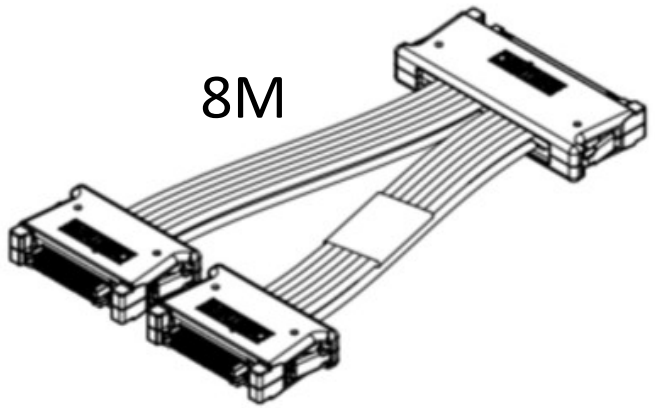
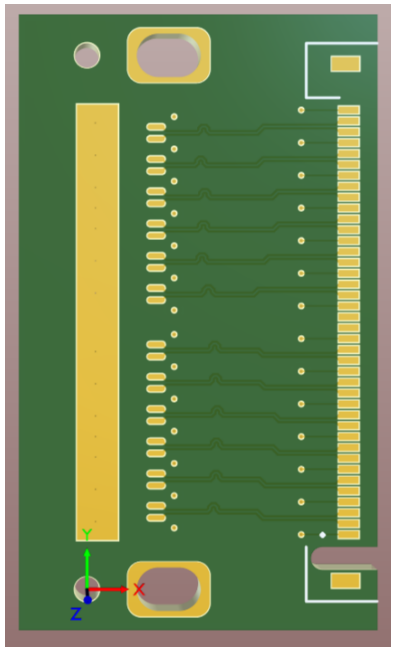

J1


J1




J1


8M



GBT-FPGA IP example design for AXKU041, AXKU15 V2.0 and AXU9EGB ALINX development boards

This repository is based on the original GBT-FPGA IP (https://gitlab.cern.ch/gbt-fpga/gbt-fpga) but has been ported to the ALINX AXKU041, AXKU15 V2.0 and AXU9EGB development boards. The main difference in the cases of ALINX AXKU041 and AXU9EGB is the use of a 125 MHz clock as a reference for the GBT modules, this change implies that the transmit/receive speed will be 5Gbit/sec and the framing frequency will be 41.66667 MHz in comparison with the 4.8Gbit/sec and 40 MHz of the original implementation base on a 120 MHz reference clock.

AXKU041 GBT-FPGA example project

This example is based on the Kintex Ultrascale (KC105) example design, ported to the AXKU041 developement board. Standard (TX/RX) and latency optimized (TX/RX) have been tested successfully with internal loopback, external fibre loopback and with connection to GBT-FPGA IP impemented on a AUX9EGB evaluation board. The latency optimized implementation has not been validated or measured for actual fixed latency (TODO), only functional tests have been done.

Clocks:

- QSFP_REFCLK1: The 125MHz MGT reference clock is provided by the onboard SiT9102-125 located on the ALINX FH1224 fiber optic transceiver FMC card.
- USER_CLK: 200 MHz clock used to generate 125 MHz free running clock.

Connections:

- QSFP1 (link 1-4) is used from ALINX FH1224 fiber optic transceiver FMC card. (SFP1 on board was also tested)
- QSFP2 (link 1-4) is used from ALINX FH1224 fiber optic transceiver FMC card.

AXKU15 V2.0 GBT-FPGA example project

This example is based on the Kintex Ultrascale (KC105) example design, ported to the AXKU15 V2.0 developement board. Standard (TX/RX) and latency optimized (TX/RX) have been tested successfully with internal loopback, external fibre loopback and with connection to GBT-FPGA IP impemented on a AXKU15 development board. The latency optimized implementation has not been validated or measured for actual fixed latency (TODO), only functional tests have been done.

Clocks:

- QSFP_REFCLK1: The 120MHz MGT reference clock is provided by the onboard Si5332C located on the AXKU15 card.
- USER_CLK: 200 MHz clock used to generate 120 MHz free running clock.

Connections:

- QSFP1 (link 1-4) is used from ALINX FH1224 fiber optic transceiver FMC card.
- QSFP2 (link 1-4) is used from ALINX FH1224 fiber optic transceiver FMC card.

AUX9EGB GBT-FPGA example project

This example is based on the Kintex Ultrascale (KC105) example design, ported to the AUX9EGB developement board. Standard (TX/RX) and latency optimized (TX/RX) have been tested successfully with internal loopback, external fibre loopback and with connection to GBT-FPGA IP impemented on a AXKU041 development board. The latency optimized implementation has not been validated or measured for actual fixed latency (TODO), only functional tests have been done.

Clocks:

- SFP_REFCLK0: The 125MHz MGT reference clock is provided by the onboard SiT9102-125.
- USER_CLK: 200 MHz - clock used to generate 125 MHz free running clock.

felix-server.tlp - work@159.93.50.70:22 - Bitvise xterm - work@felix-server:~/felix-distribution/x8...

```
[work@felix-server x86_64-el9-gcc13-opt]$ ./flxcard/flx-init -c0
2025-06-23 08:48:47 Opening card 0 (device 0)...
2025-06-23 08:48:47 Card type: FLX-15
2025-06-23 08:48:47 Firmware : GBT
2025-06-23 08:48:47 Clock    : Local
2025-06-23 08:48:47 FLX soft reset
2025-06-23 08:48:47 Configuring SI5332...
2025-06-23 08:48:48 SI5332 configured (73 registers)
2025-06-23 08:48:48 Links soft reset
2025-06-23 08:48:48 Setting up links...
2025-06-23 08:48:54 Done, number of links aligned: 2
2025-06-23 08:48:54 Initializing LTI...
2025-06-23 08:48:54 LTI alignment: NO
[work@felix-server x86_64-el9-gcc13-opt]$
```

hw_vios

hw_vio_1

Dashboard Options

Name	Value	Activity	Direction	VIO
countWordReceived[1][31:0]	[U] 3812732222		Input	hw_vio_1
countWordReceived[2][31:0]	[U] 3922045336		Input	hw_vio_1
countBitsModified[1][31:0]	[U] 1507520503		Input	hw_vio_1
countBitsModified[2][31:0]	[U] 2154459208		Input	hw_vio_1
mgtReady_from_gbtExmplDsgn[1:2]	[H] 3		Input	hw_vio_1
gbtRxReady_from_gbtExmplDsgn[1:2]	[H] 3		Input	hw_vio_1
txAligned_from_gbtbank_latched[1:2]	[H] 3		Input	hw_vio_1
rxFrameClkReady_from_gbtExmplDsgn[1:2]	[H] 3		Input	hw_vio_1
rxIsData_from_gbtExmplDsgn[1:2]	[H] 0		Input	hw_vio_1
txAlignComputed_from_gbtbank[1:2]	[H] 3		Input	hw_vio_1
gbtRxReadyLostFlag_from_gbtExmplDsgn[1:2]	[H] 3		Input	hw_vio_1
rxExtrDataWidebusErSeen_from_gbtExmplDsgn[1:2]	[H] 0		Input	hw_vio_1
rxDataErrorSeen_from_gbtExmplDsgn[1:2]	[H] 0		Input	hw_vio_1
rxBitSlipRstCount_from_gbtExmplDsgn[1][7:0]	[H] 00		Input	hw_vio_1
rxBitSlipRstCount_from_gbtExmplDsgn[2][7:0]	[H] 00		Input	hw_vio_1
latOptGbtBankTx_from_gbtExmplDsgn			Input	hw_vio_1
latOptGbtBankRx_from_gbtExmplDsgn			Input	hw_vio_1
txFrameClkPllLocked_from_gbtExmplDsgn			Input	hw_vio_1
txMatchFlag_from_gbtExmplDsgn			Input	hw_vio_1
reset_from_genRst			Input	hw_vio_1
shiftTxClock_from_vio	[B] 0		Output	hw_vio_1
txIsDataSel_from_user	[B] 0		Output	hw_vio_1
txShiftCount_from_vio[7:0]	[H] 00		Output	hw_vio_1
DEBUG_CLK_ALIGNMENT_debug[2:0]	[H] 0		Output	hw_vio_1
loopBack_from_user[2:0]	[H] 1		Output	hw_vio_1
testPatterSel_from_user[1:0]	[H] 3		Output	hw_vio_1
resetgbtfpga_from_vio	0		Output	hw_vio_1
resetDataErrorSeenFlag_from_user	0		Output	hw_vio_1
rxBitSlipRstOnEvent_from_user	0		Output	hw_vio_1
manualResetRx_from_user	0		Output	hw_vio_1
manualResetTx_from_user	0		Output	hw_vio_1
clkMuxSel_from_user	0		Output	hw_vio_1
resetGbtRxReadyLostFlag_from_user	0		Output	hw_vio_1
rxEncoding_from_vio	[B] 0		Output	hw_vio_1
txEncoding_from_vio	[B] 0		Output	hw_vio_1
txPllReset	0		Output	hw_vio_1