Development of the Readout Board for Highly Granular Neutron Detector at the BM@N experiment

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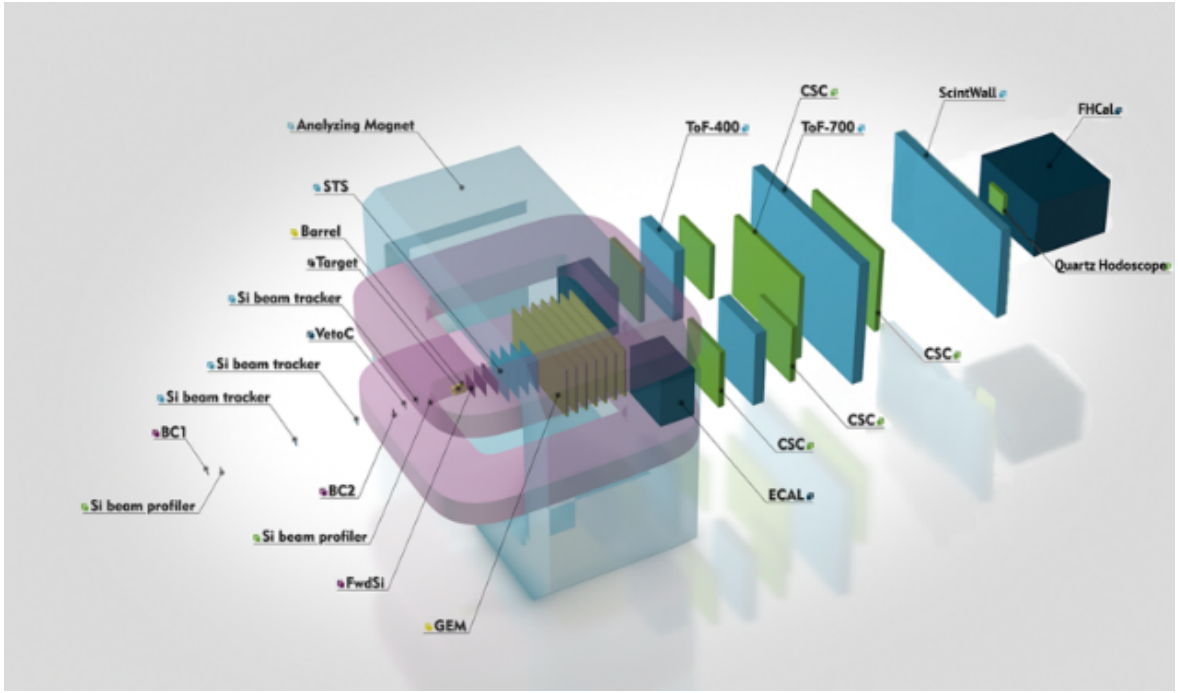
BM@N experiment

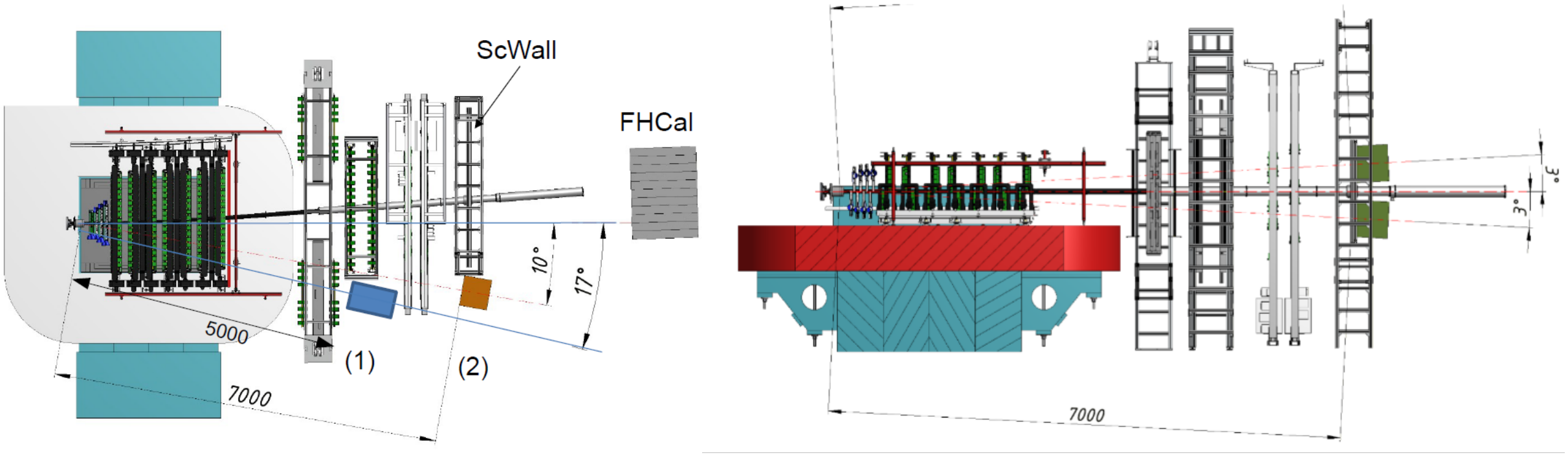


Barionic Matter at Nuclotron (BM@N) setup:

- Fixed target
- Ion beam with energy of up to 4.5 AGeV from Nuclotron of the NICA accelerator complex at JINR, Dubna
- Large aperture analyzing magnet

The BM@N experiment is designed to study the QCD state diagram in the region of high baryon density and azimuthal asymmetry of charged particle production in heavy nuclei collisions.

Planned location of the stand with 1 HGND module at the next session on BM@N

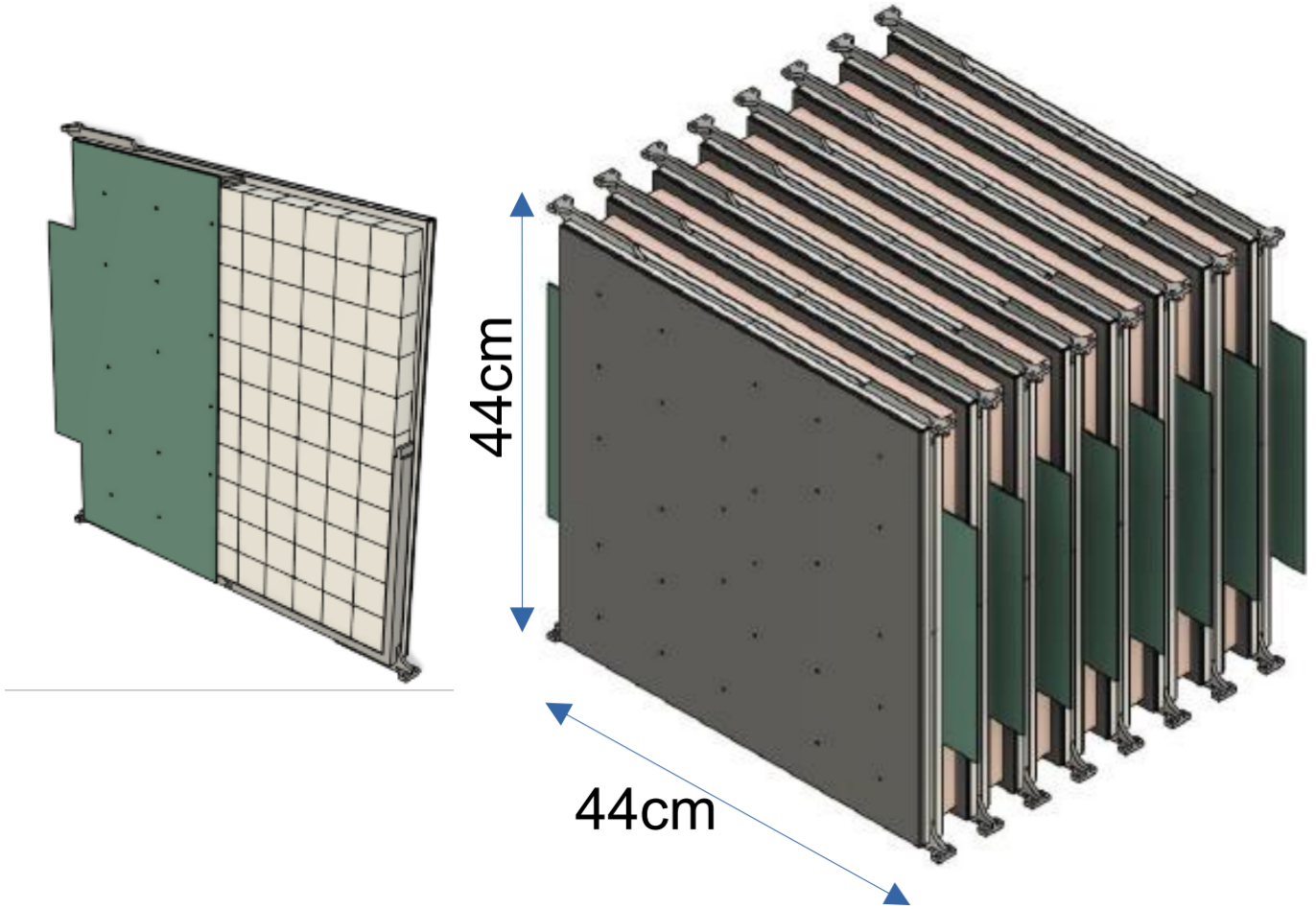


- ToF method with T0 as the “start” signal source
- 7m measurement distance
- Detector is split into 2 “blocks” for improved acceptance

The highly granular time-of-flight neutron detector: HGND

8 layers, two arms:

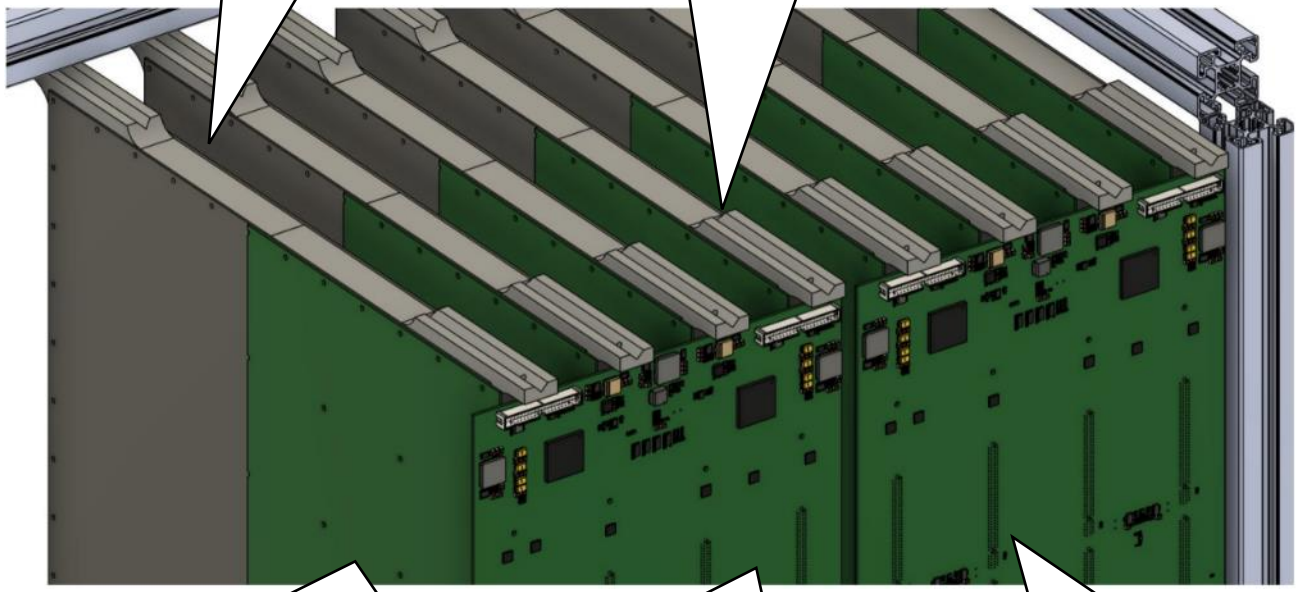
- First layer is used as veto
- 3cm Cu (absorber)
- 2.5cm Scintillator
- 0.5cm PCB
- Transverse size: 44x44 cm2
- 11x11 scintillator cell grid

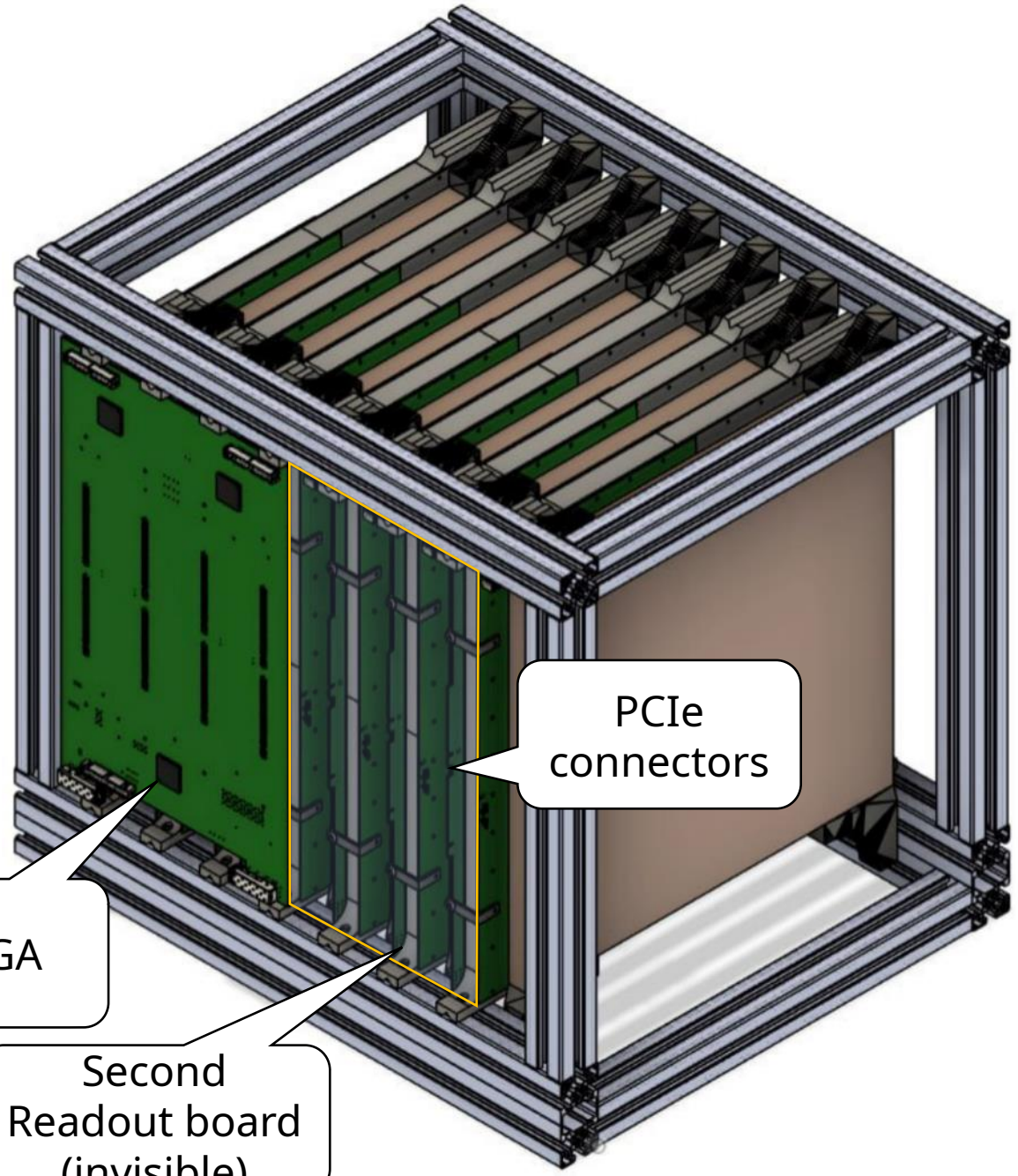


- **EQR15 11-6060D-S MPPC**
  - active aria 6x6 mm^2
  - quantum efficiency of 45% (420 nm)
  - gain of approximately 4×10^5

- polystyrene-based **scintillators** POPOP decay time 3.9±0.7 ns.
- Cell time resolution 150ps
- Nuclear interaction length: ~0.5m, ~1.5 λin
- Neutron detection efficiency: ~50% @ 1 GeV
- Energy resolution: - 2% (0.3 GeV); 20% (4 GeV)
- MIP light output value of 158±9 ph.e.
- Dynamic range: 1 – 8 MIP

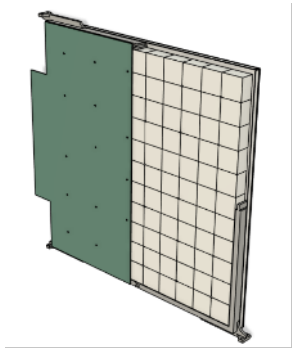
FEE & readout board: close-up



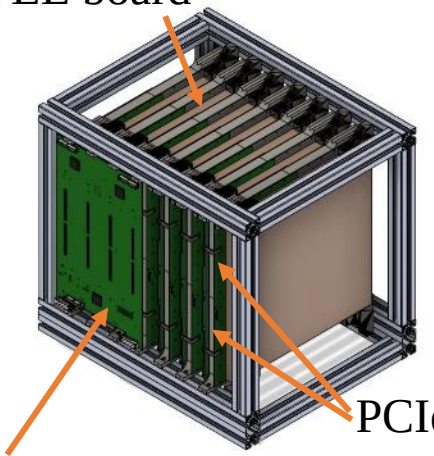


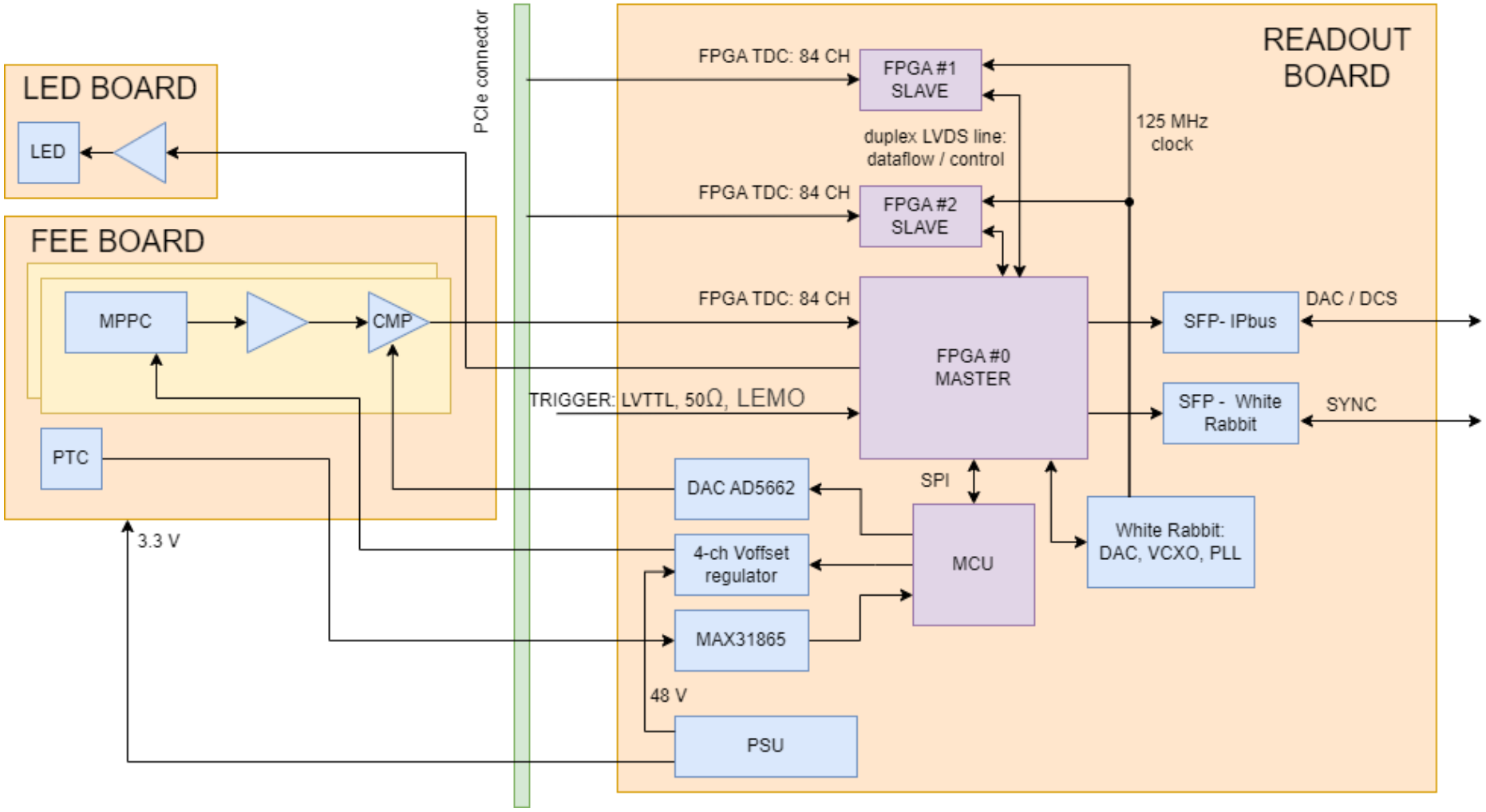
FEE & readout architecture

- 16 layers with scintillation matrix 11X11
- 16 LED boards
- 32 FEE boards
- 8 Readout boards
- 3 FPGA per board
- 84 channels per FPGA
- 2000 channels in total

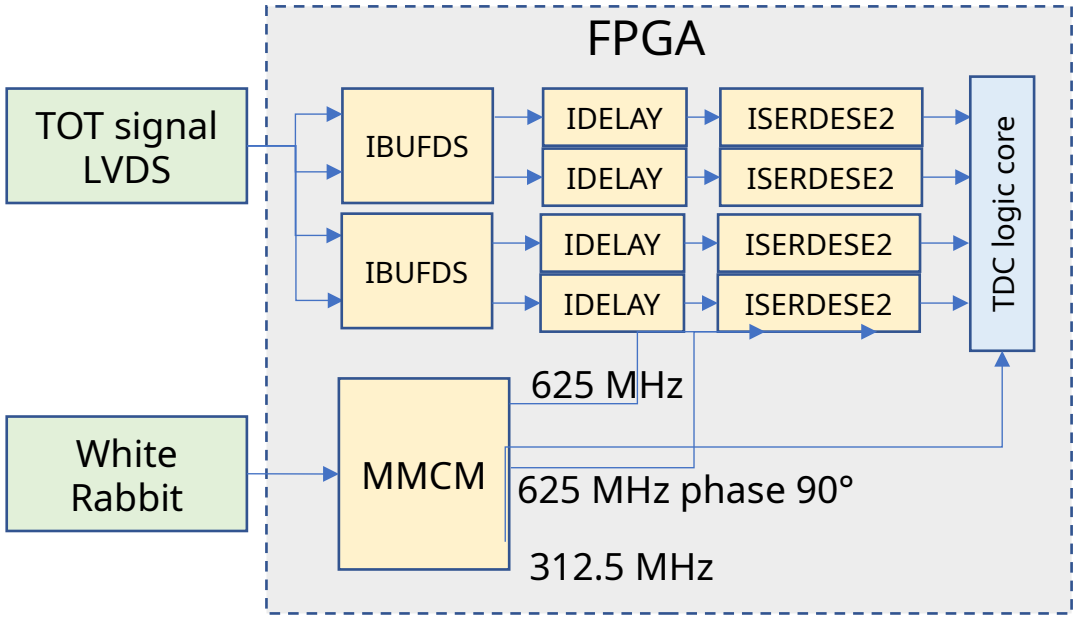


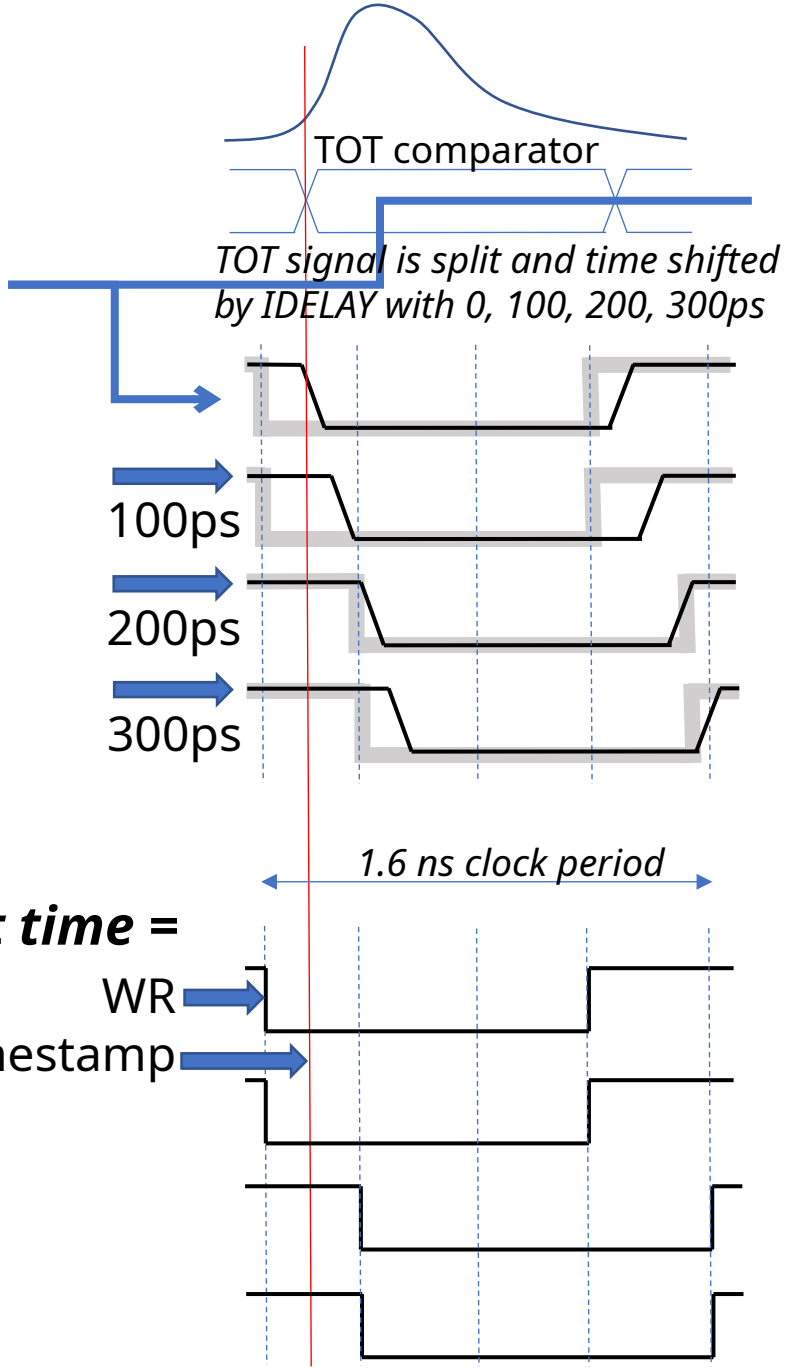
FEE board





The 100ps FPGA TDC principle of operation



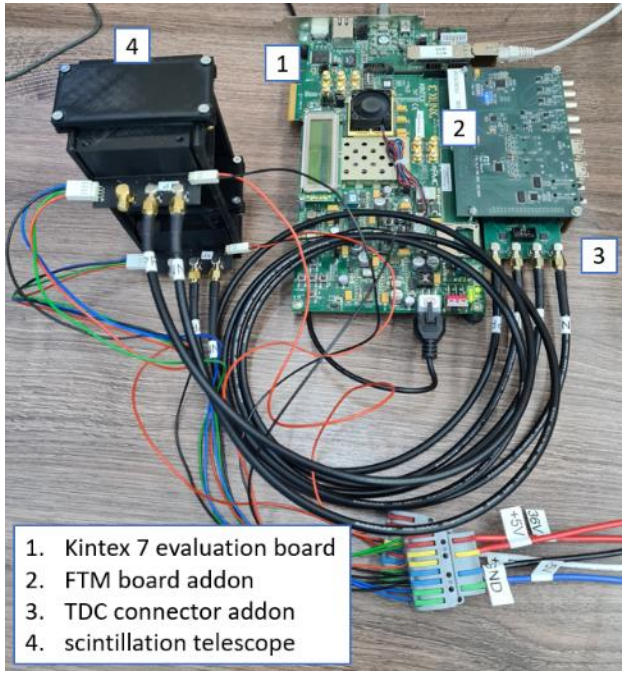


The TDC is **based on the Kintex-7** input serial-to-parallel converter with oversampling capability and programmable delay. The design is **based on Xilinx recommendations**, and uses **only documented features** of the FPGA within its specifications.

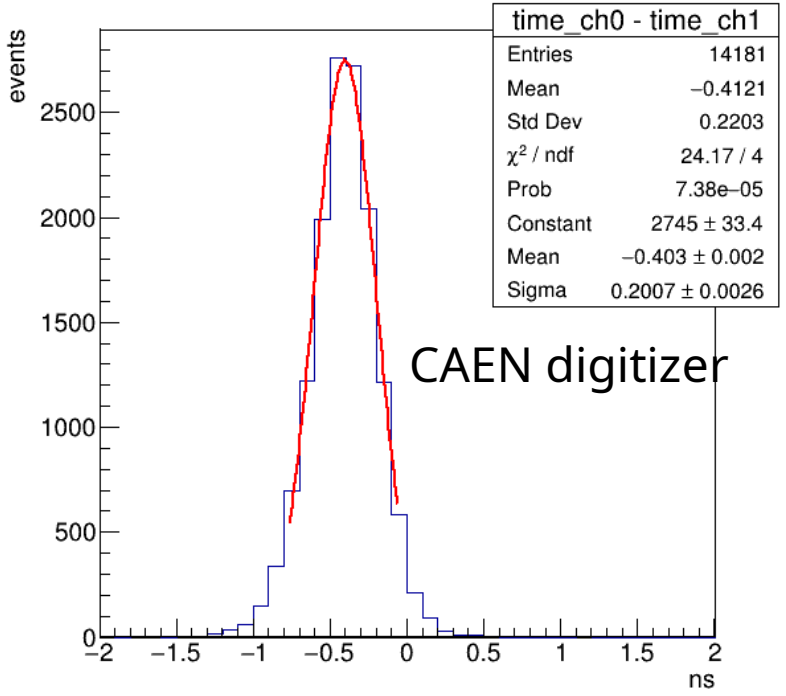
[3] D. Finogeev, F. Guber, A. Izvestnyy, N. Karpushkin, A. Makhnev et al., ***Development of 100 ps TDC based on Kintex 7 FPGA for the High Granular Neutron Time-of-Flight detector for the BM@N experiment,*** *DOI: 10.1016/j.nima.2023.168952*

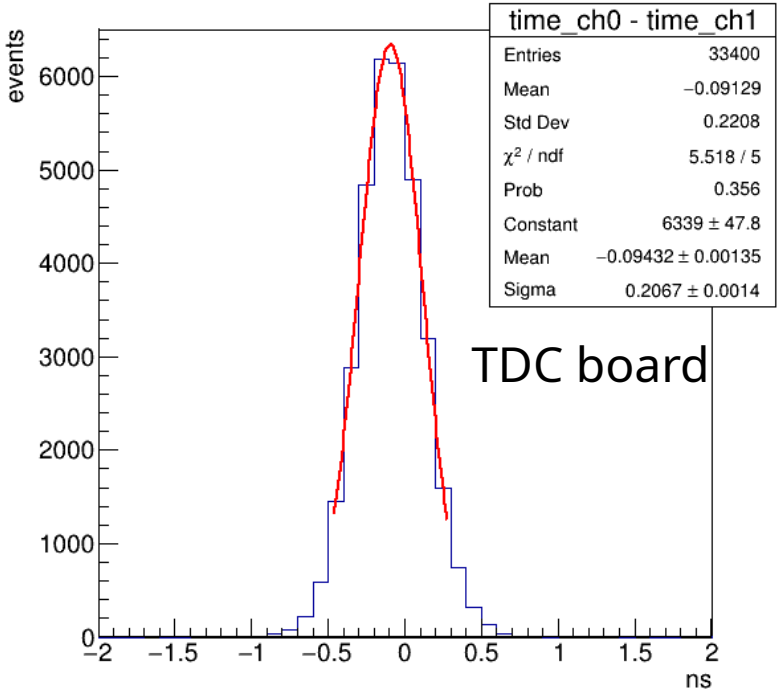
The FPGA TDC test results

The time resolution measurements with the FPGA TDC prototype board were performed with the 280 MeV electron beam on the “Pakhra” synchrotron in LPI (Moscow, Russia).



HGND scintillator cells telescope is connected to 2-channels TDC prototype based on KC705 evaluation board

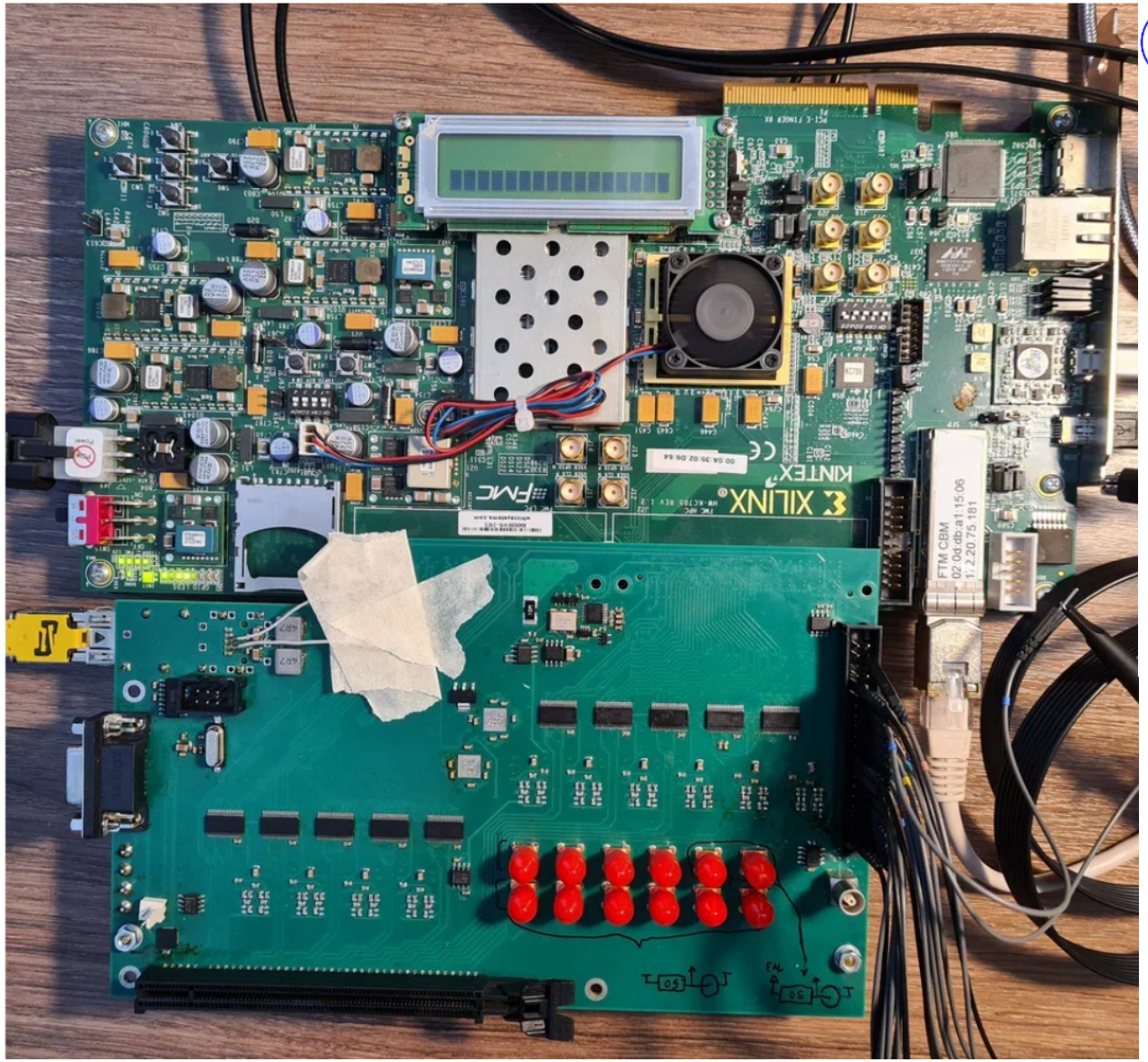


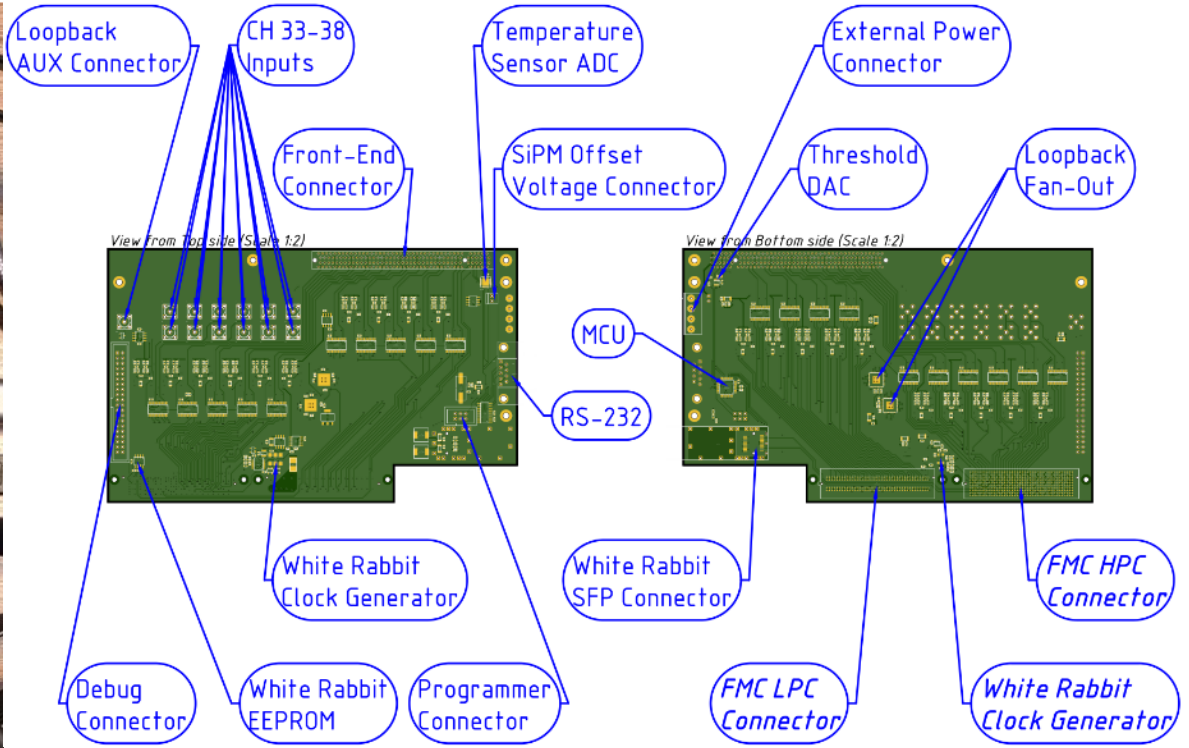


The time difference distributions of two cells of the telescope measured with the CAEN digitizer (left) and the FPGA TDC prototype board (right). Time resolution is ***146 ps*** per single HGND channel.

HGND readout v2 prototype (39 channels)

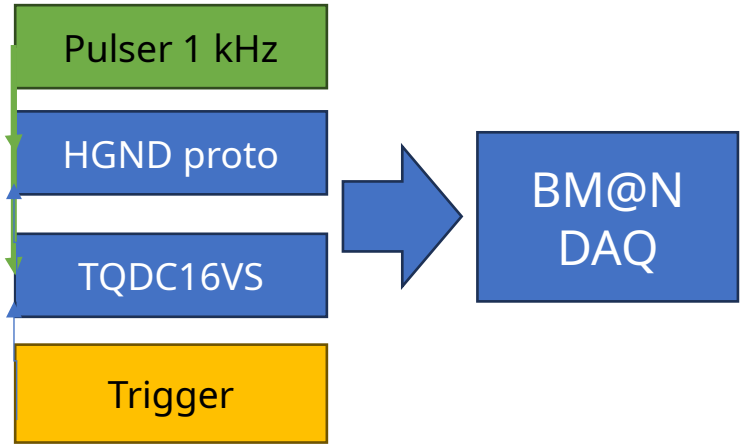
based on the Kintex 7 evaluation board (KC705)



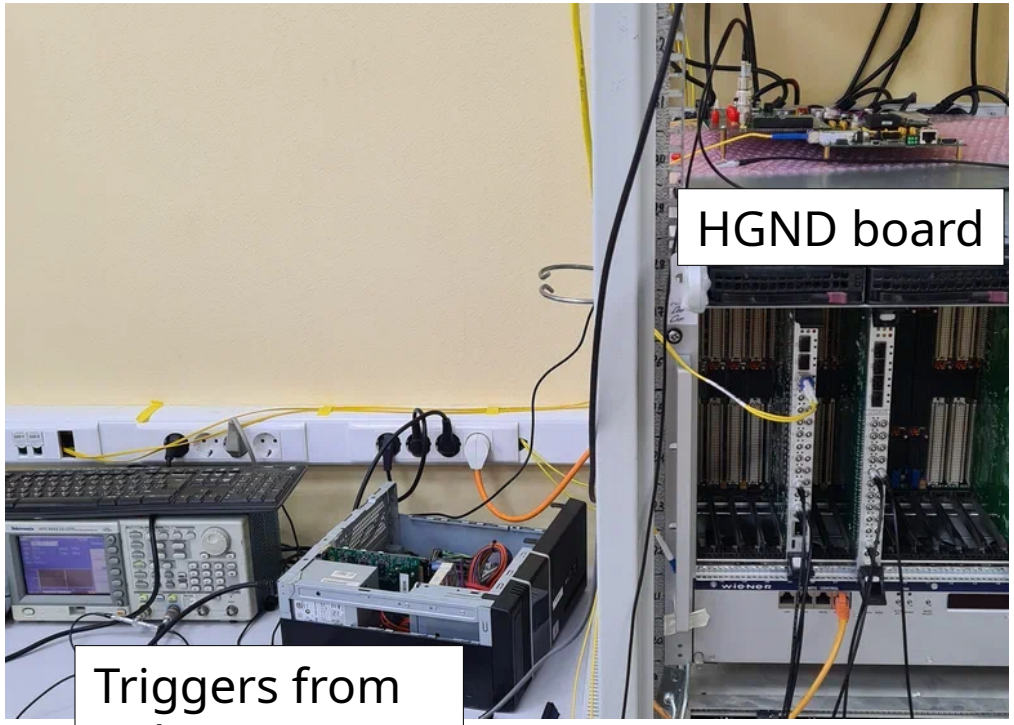


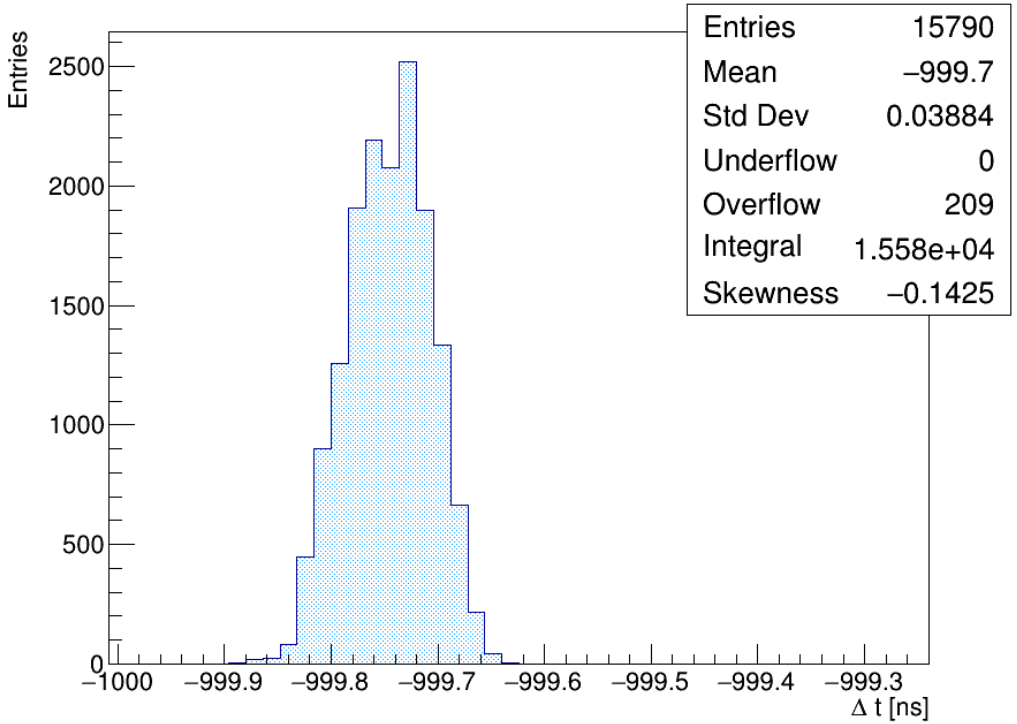
- Addon for Kintex 7 evaluation board
- 33 PCIe + 6 SMA TDC channels
- Ethernet readout
- White Rabbit synchronization
- FPGA loopback for TDC calibration
- Readout board functionality:
  - *PCIe connector for* scintillation matrix, *Temperature sensor, SiPM offset voltage control DAC threshold*

The HGND integration tests



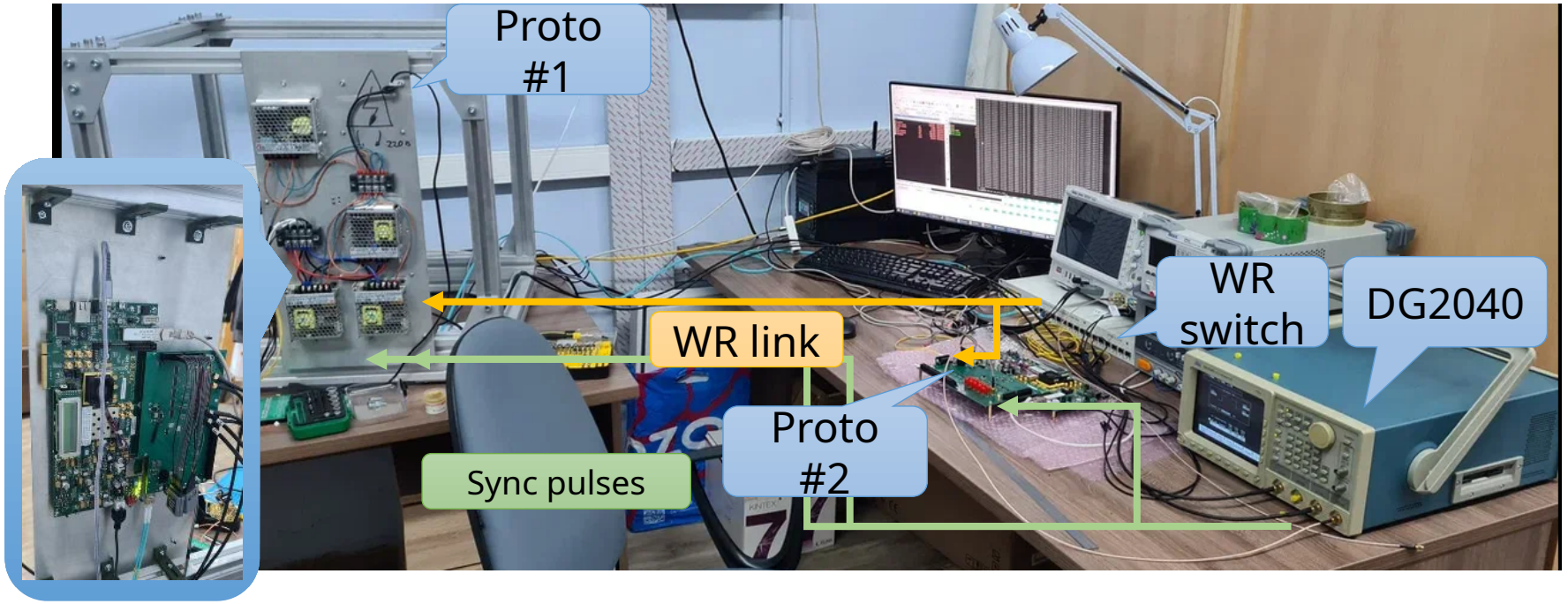
- The HGND readout prototype was connected to BM@N DAQ.
- Synchronous pulse was propagated to HGND and TQDC board.
- BM@N DAQ event builder and run control software used.
  - ✓ Continuous readout
  - ✓ Time synchronization (σ = 39 ps)
  - ❑ Triggered readout
  - ❑ Experiment DAQ control

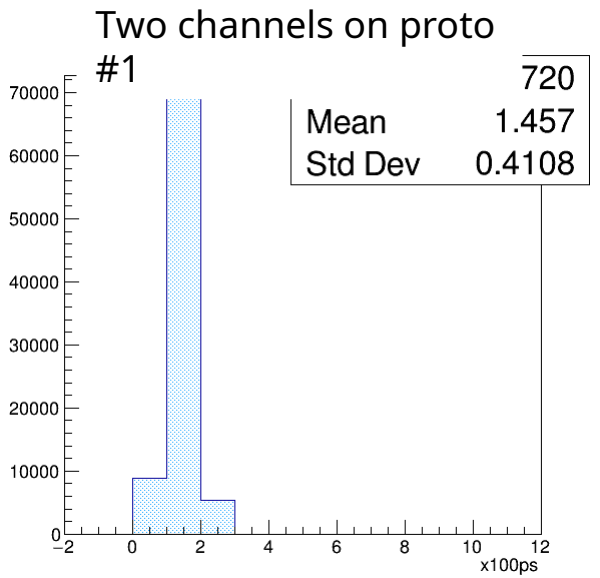


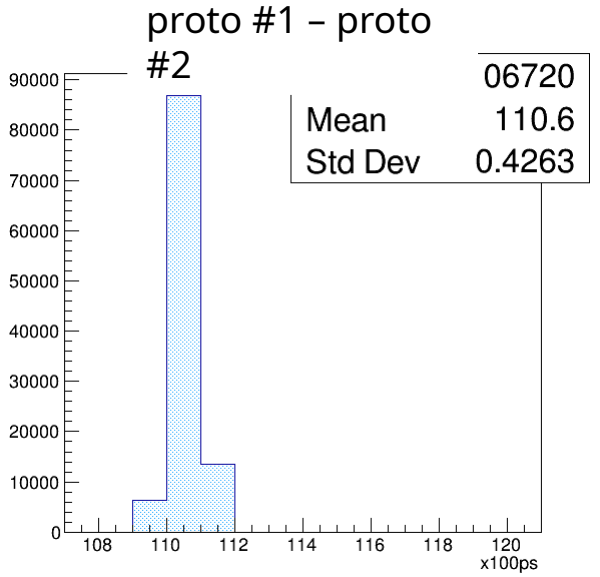


Time synchronization HGND – TQDC board

WR cross board synchronization test

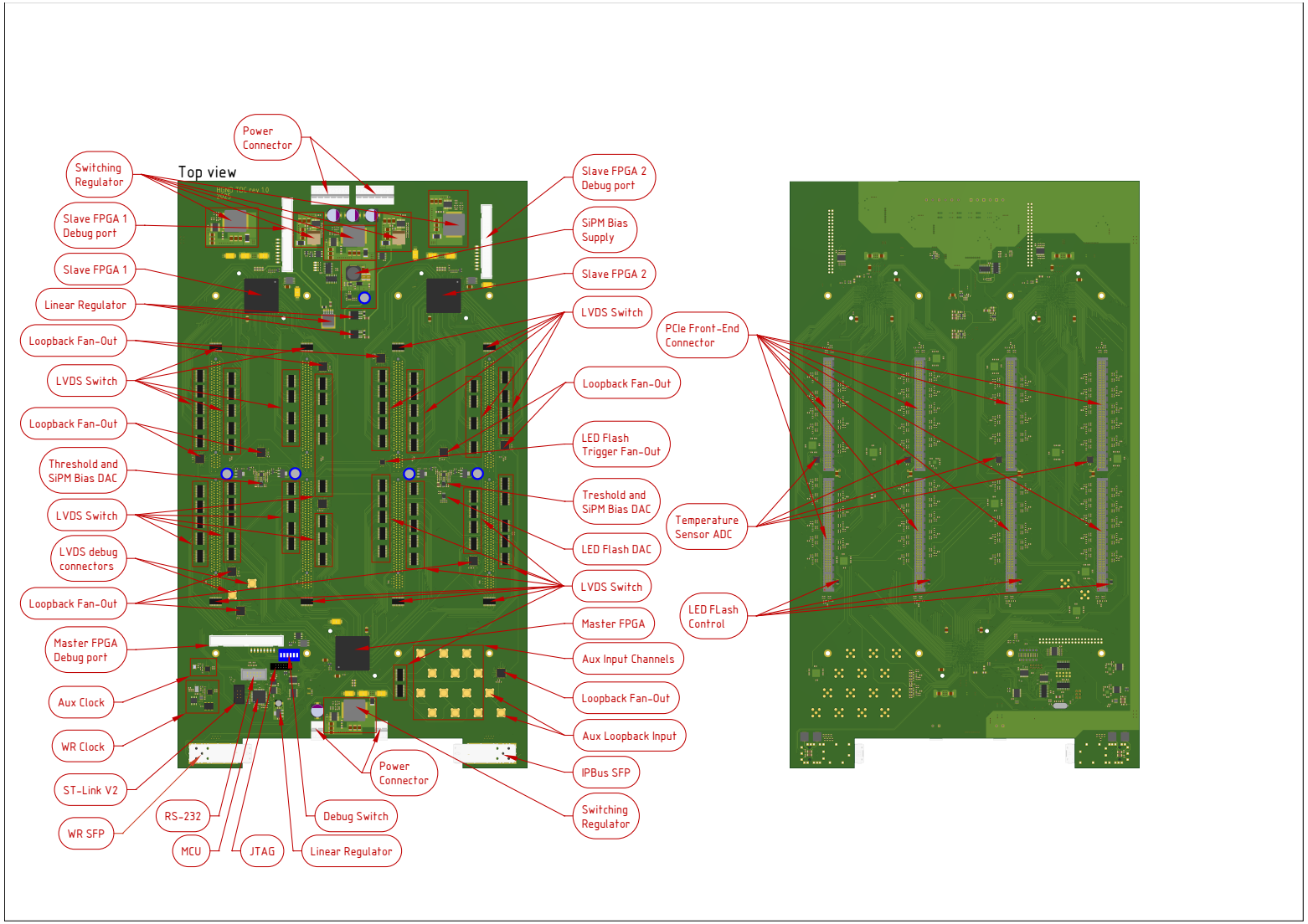






- Two prototype readout boards are synchronized using a White Rabbit switch.
  - Proto #1 receives pulses from two channels.
  - Proto #2 receives pulses from a single channel.
- The intrinsic jitter of the **DG2040** generator is **5 ps**.
- The TDC channel's time resolution is **30 ps**.
- The time difference distributions (both cross-board and single-board) is **42 ps** and match the TDC's resolution.

Readout Board design



Readout Board must perform following functions:

- TDC with at least 242 channels
- Synchronize time with WhiteRabbit network
- Supply SiPM bias voltage
- Set comparator tresholds in the Front-End
- Monitor detector temperature
- Control LED flash boards

Input channels

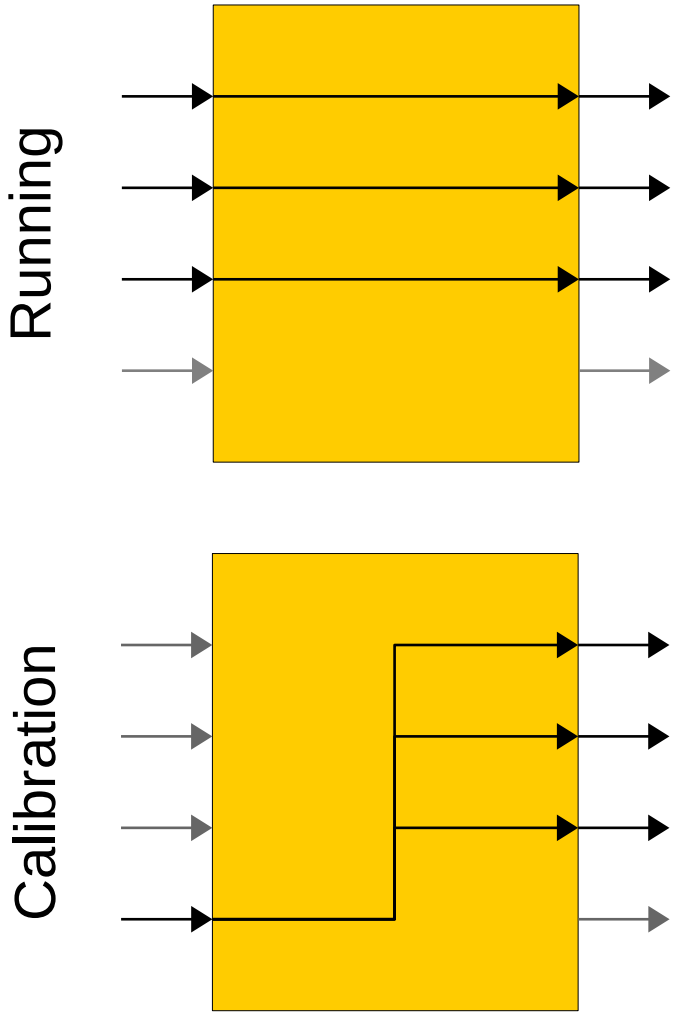
242 channels receive signals from Front-End boards via PCIe connectors

- PCIe was chosen as a commonly used inter-board connector capable of carrying high-speed differential signals
- Each Front-End board is connected by two PCIe x16 connectors carrying up to 66 differential lines
- Front-End board was designed to work with outputs terminated to ground by 50 Ohm resistors

6 channels are routed to coaxial SMA connectors

- These channels can be used for trigger connection or testing
- During assembly the termination of these channels can be configured for a variety of signal standards, including unipolar

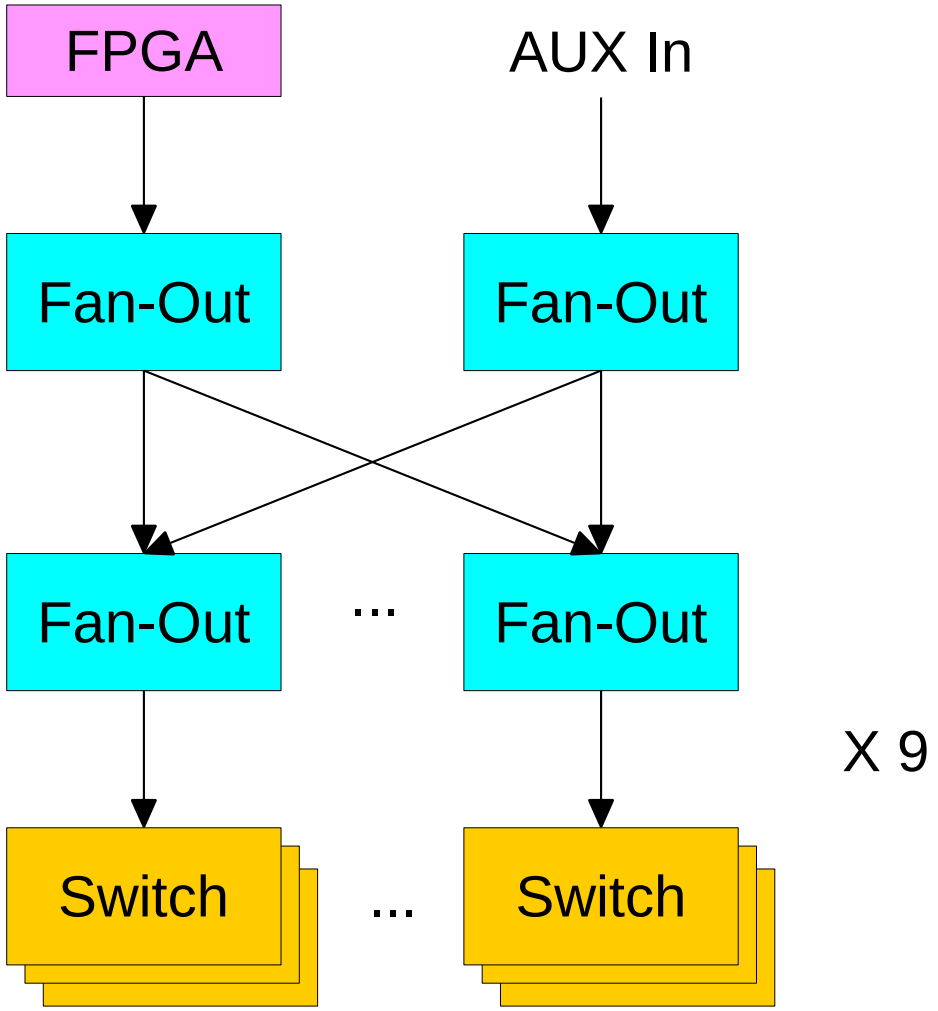
Switch modes



A total of 83 SN65LVDS125 4-by-4 crosspoint switches are used in the HGND Readout Board

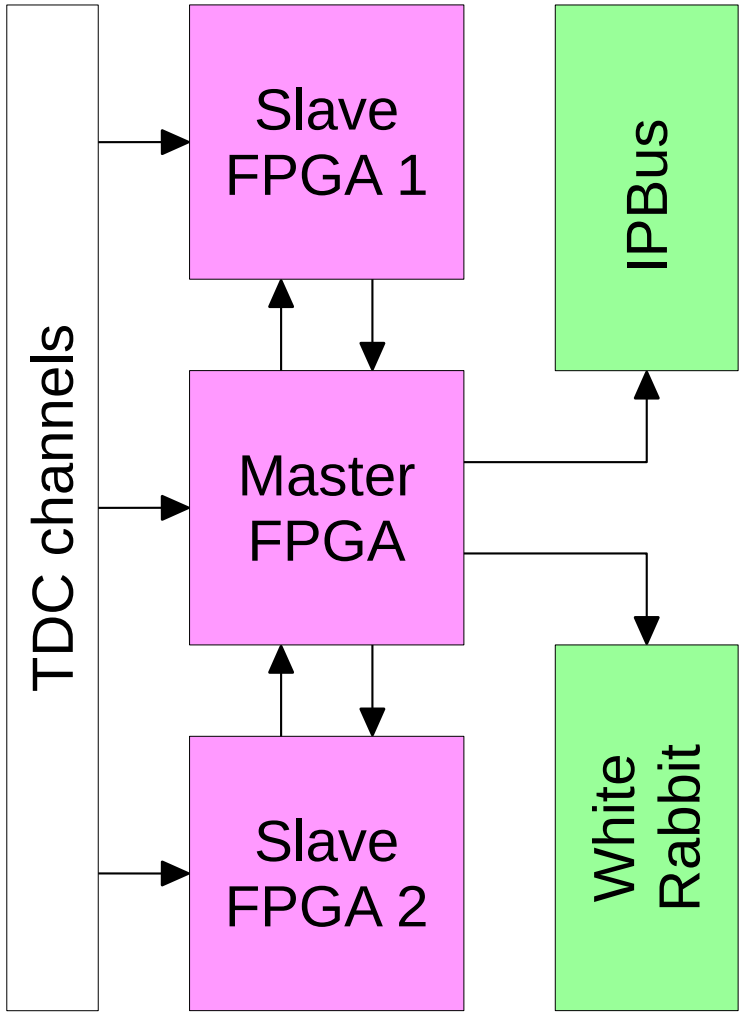
- Each unit can service 3 TDC channels
- Input signals are converted to LVDS standard
- Outputs can be switched between running and calibration configurations
- The performance of these devices was tested in the readout board prototype

Loopback tree



- To propagate the calibration signal to the switches a two-stage arrangement of ADCLK854 fan-out chips was designed
- Signals from the FPGA and from a pair of coaxial connectors are propagated to the nine second stage fan-out units by two independent units in the first stage
- Second stage units can be switched independently between FPGA and AUX signals, propagating these signals to 9 groups of channel switches
- Every group of switches is controlled as one unit

FPGAs

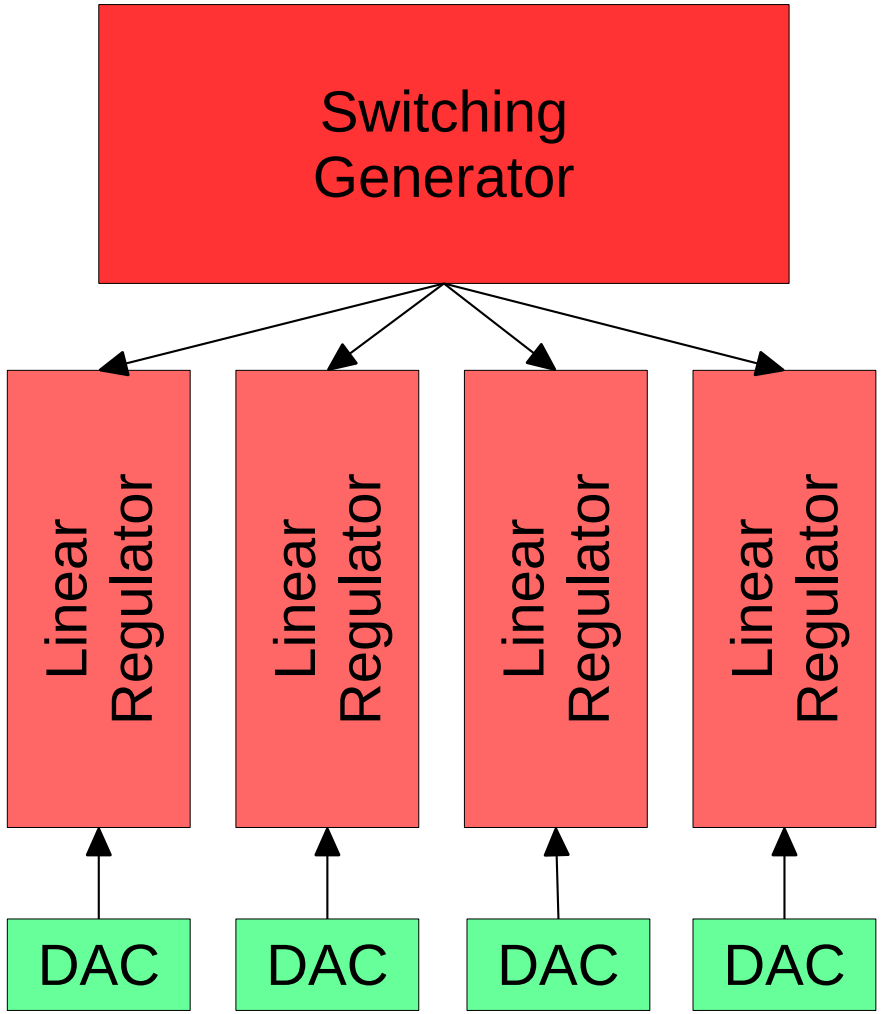


- Three XC7K160T FPGAs are mounted on each Readout Board
- Each TDC channel is connected to two LVDS inputs on an FPGA in parallel
- Two slave FPGAs are linked to the master FPGA and are used exclusively for TDC
- Master FPGA is equipped with extra debug inputs and is also used for WhiteRabbit implementation, calibration and LED flash signal generation, DAQ and control interface and controlling other functions via a connection to the MCU
- All FPGAs are equipped with a debug port and joined in a JTAG chain for programming
- FPGA configuration is controlled by the MCU

White Rabbit & clock

- WhiteRabbit clock system is based on a reference design and was tested in the readout board prototype
- 25 MHz clock from WhiteRabbit is propagated to all FPGAs
- Master FPGA has an RS-232 connection for WhiteRabbit debug
- Control interface of the SFP+ connector used in WhiteRabbit is fully implemented
- An independant 25 MHz clock generator is connected to all FPGAs for testing calibration purposes

SiPM bias supply



- An LM3481 based switching voltage generator produces +40 V supply
- Four channels of linear voltage regulators controlled by four channels of DAC provide bias voltages independently to each Fron-End board
- +40 V generator may be switched off by the MCU

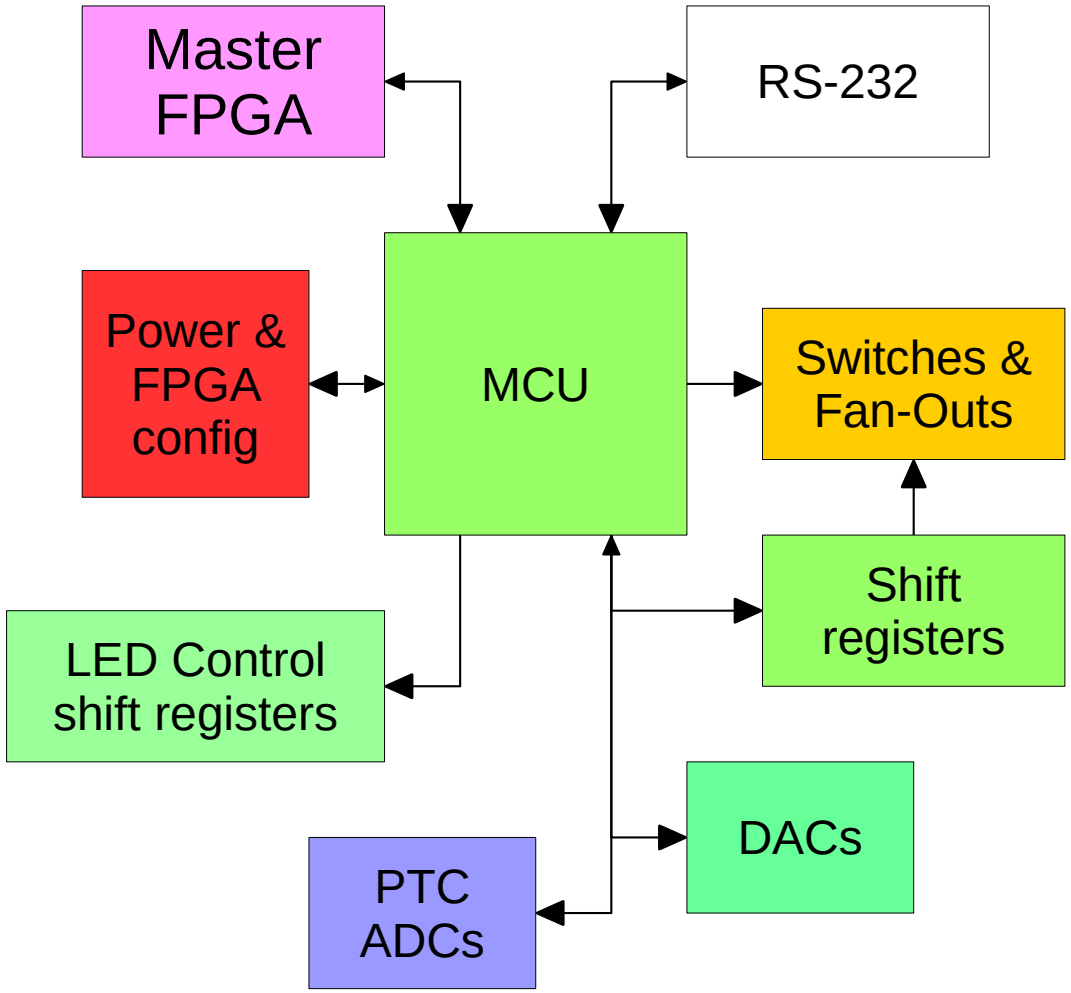
Comparator Thresholds and Temperature Sensors

- The AD5664 DACs that control bias voltage regulators also provide four channels for setting the tresholds of the comparators in the Front-End boards
- Thresholds are set independently for each Front-End board
- DAC output range is 0 V to +2.5 V
- Four MAX31865 ADCs read temperature information from platinum thermistors installed on the Front-End boards
- Data is collected by the MCU via an SPI conecion
- The temperature monitoring system was tested in the readout board prototype

LED flash controls

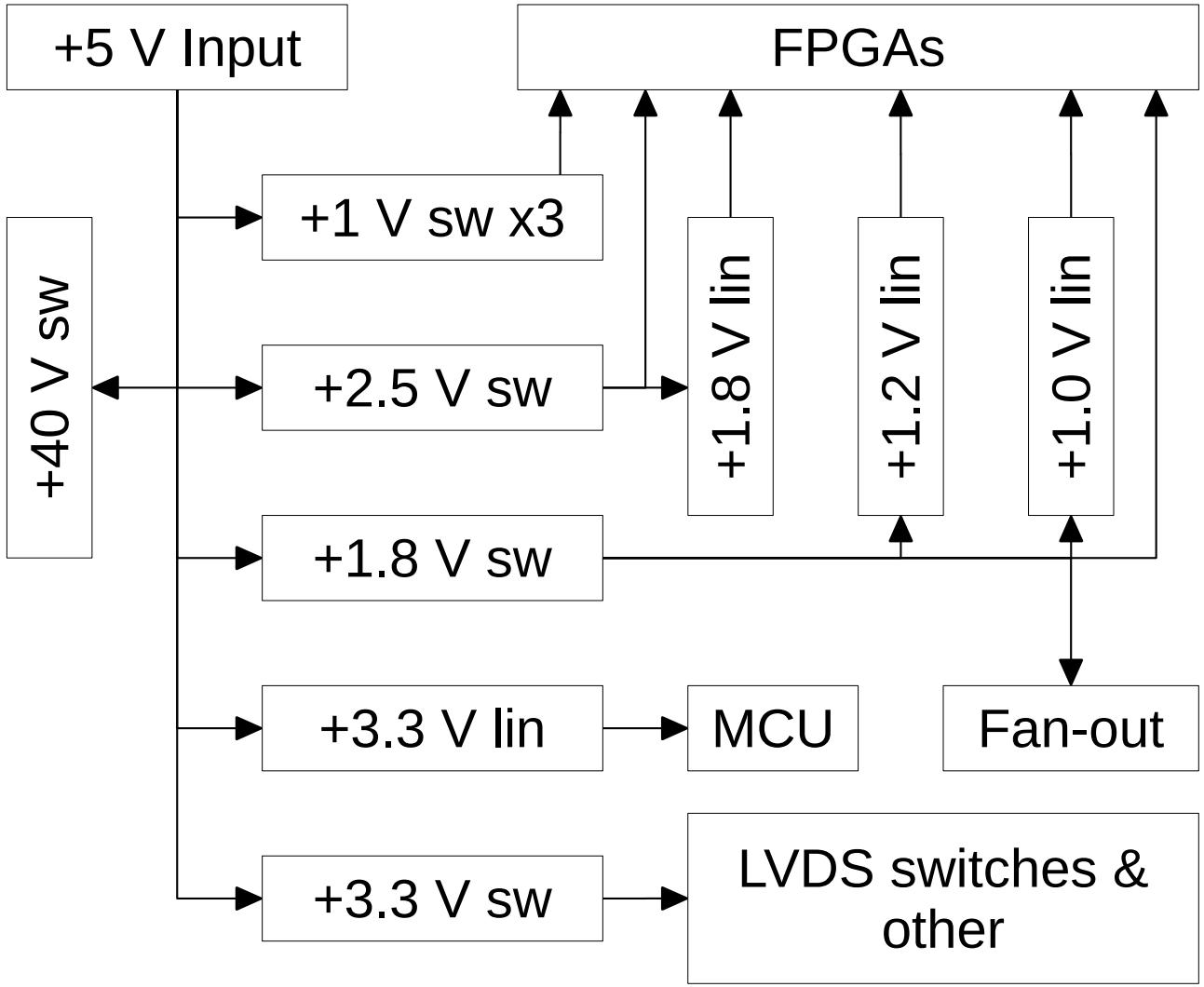
- LED flash is triggered by a signal produces by the master FPGA and propagated to all four Front-Ends
- Intensity of the flash is controlled independently in four Front-Ends by a four-channel DAC
- LED flash in each scintillator cell in a layer can be enabled or disabled individually; to write data into the shift registers in the Front-End that control the LED flash emitters a separate SPI connection with individual chip select lines was routed to the Front-End connectors

MCU



- The STM32F103RET6 MCU can be controlled from the master FPGA via SPI connection or from an RS-232 interface
- The MCU controls bias voltage regulation, threshold setting and LED flash intensity DACs and reads temperature ADCs via an SPI connection
- LVDS switches and loopback fan-outs are controlled directly or via shift registers
- MCU monitors power status and controls the start of power-up sequence and FPGA configuration
- MCU can be programmed and debugged via ST-Link V2 connection

Power



- Estimated total current consumption is about 25 A
- All power rails except MCU and bias supplies are monitored
- A power fault stops all FPGA supply generators
- Correct FPGA power-up sequence is performed automatically
- All switching voltage generators are synchronized

Production status

- Readout Board design is complete
- First Readout Board is being manufactured
- Active and exotic electronic components are stockpiled for 10+1 boards

Plans

- Prototype beam tests during BM@N run
- MCU firmware development
- First unit assembly and testing
- Preparation for serial production
- Adapting design for left-side variant