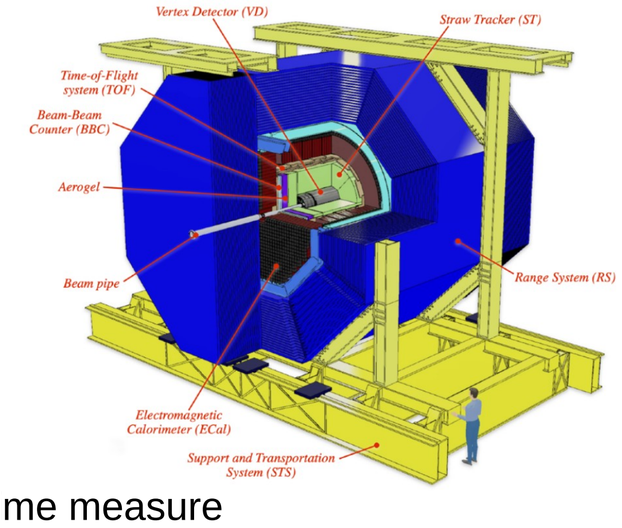
Development of a VMM3A-based Readout Solution for the SPD Stage-I Straw Tracker

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Motivation:

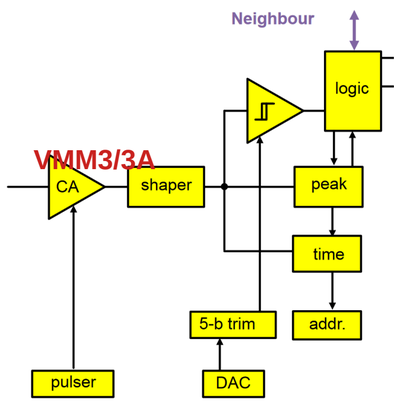
- 30k+ channels
- 150um spatial resolution
- dE/dX charge resolution
- Simultanious Charge & Time measure



In our recent design we have implemented several solutions prior to the **SPD-NICA** specifics. We have successfully integrated our new on-board DC/DC chain. By using the core-less coils new schematic is capable of operating in the magnetic fields of 1.5T. We have set up the tests with the real load and in real dimensions, checking the efficiency, testing cooling options and the noise level.

We have also added **SPD**-specific interface and protocols to our design in order to begin first integration tests with the DAQ group.

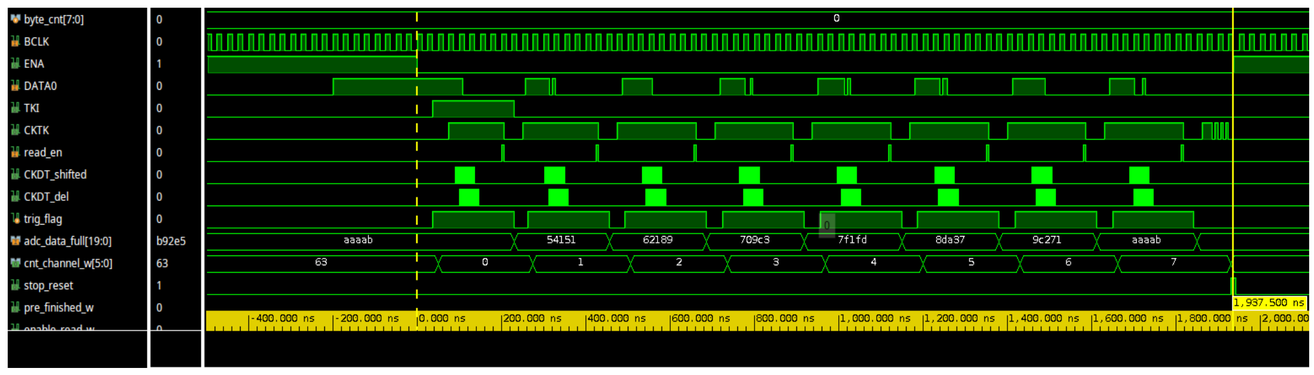
Investigating existing readout solutions



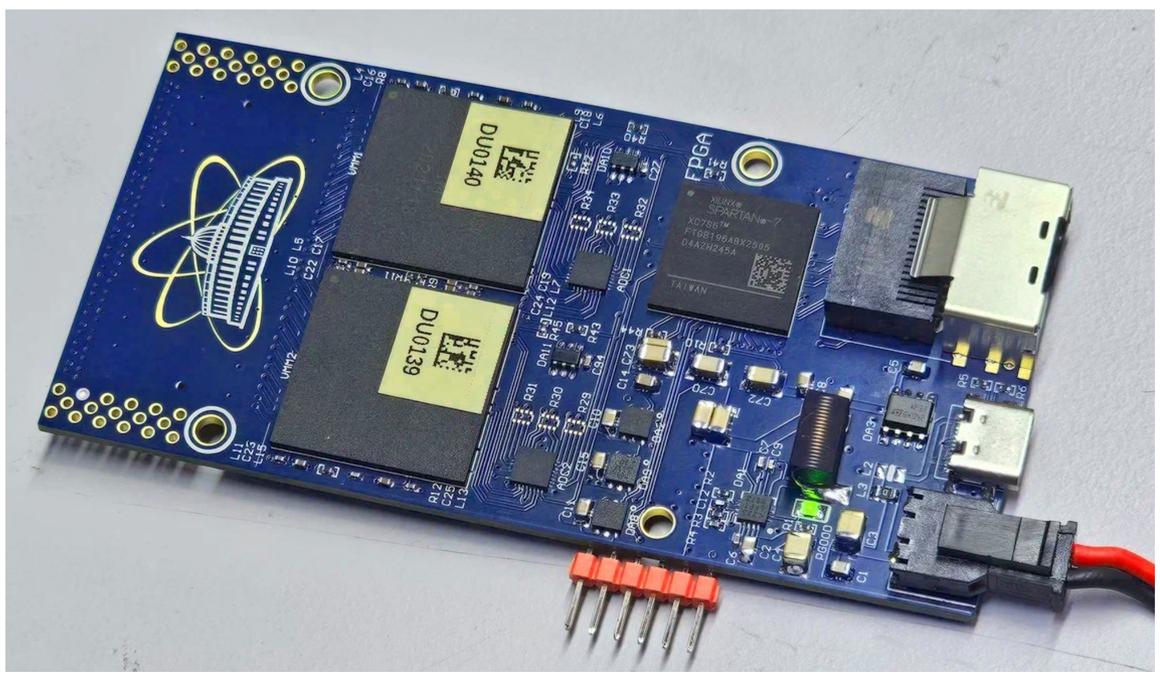
Number of channels	64
Clock frequency	10...80 MHz
Input capacitance	<300 pF
Dynamic range	up to 2 pC
Gain	0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC
Peaking time	25 / 50 / 100 / 200 ns
ENC (energy branch)	<3000 e^-
TDC binning	~1 ns
Maximum event rate	140 kHz/ch
Consumption	15 mW/ch

VMM3/3A ASIC is well known chip for gaseous detectors. It has amplifier and shaper adjustable in a wide range. But it was not really done for the timing measurements so fastest shaping is 25ns and ToA mode has some issues.

New VMM3A FEB designed

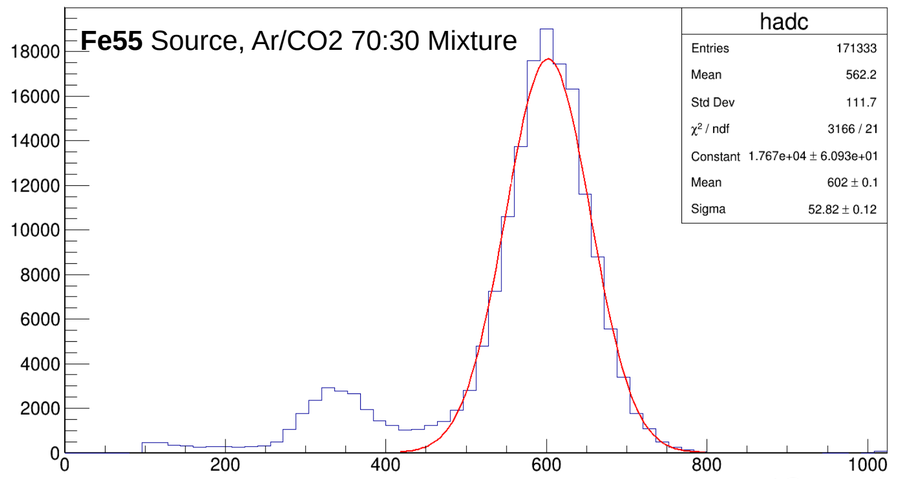


The main challenge was to achieve reasonable dead time. Typical event size in the straw tracker cell will be 8 channels. As shown on the plot above, in out new design with Spartan-7 FPGA we managed to reduce the dead time to less than 2us. While this time is still worse than the one in normal Continuous readout mode of the VMM3a ASIC, it is more that enough to operate with the hitrate of 10-20 kHz per channel which is reasonable for the **SPD Stage-I**.

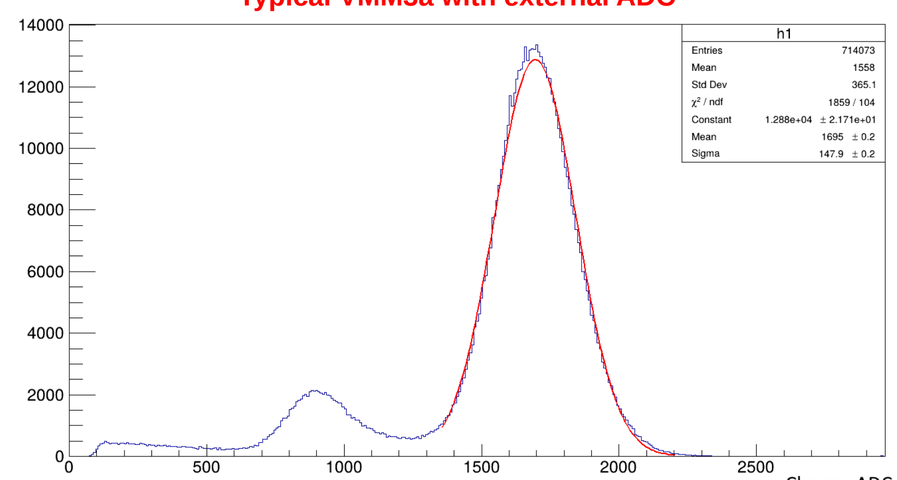


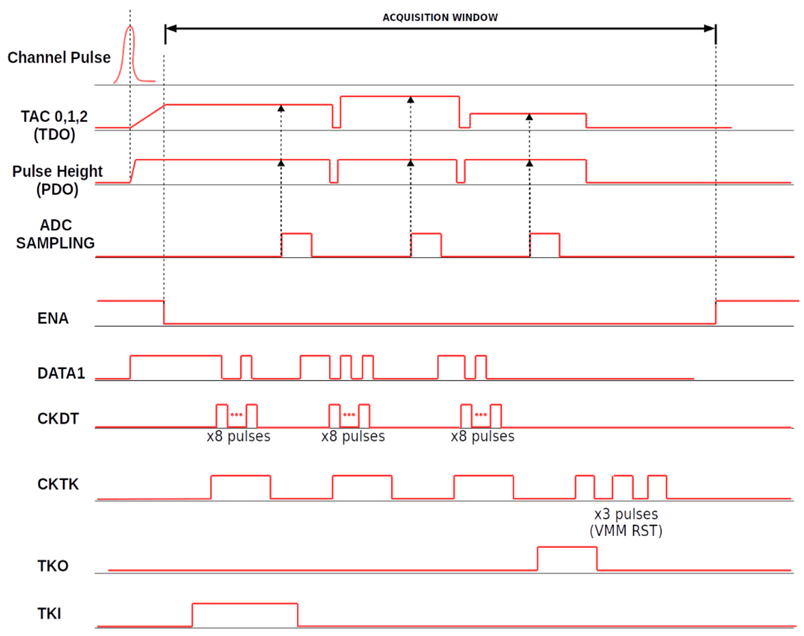
The new design utilize a non-commonly used mode of operation for the VMM3a ASIC. One can see significant improvement in the digitization resolution shown in the picture on the right. The main drawback is the speed. While digitizing the series of channels whole VMM3a ASIC needs to be shut down not getting new events.

Typical VMM3a with internal ADC



Typical VMM3a with external ADC





- Once the process is complete the **ASIC can be switched readout phase**. The first set of amplitude and time voltages is made available at the **analog outputs**. The **address of the channel is serialised** and made available at the digital output using **six data clocks**.

Conclusions:

- A new front-end electrics solution has been designed for the first stage of **SPD-NICA** Straw Tracker
- In order to achieve the best performance for the straw tubes, we have developed completely new schematic including differential buffering and external ADCs
- We managed to utilize the existing VMM3A ASIC originally designed for ATLAS Micromegas detector
- That helped us to achieve a low-cost design with a price of ~3-5$ per channel and a power consumption of about 20-30mW per channel
- The device is a complete multichannel solution for collection, amplification and digitization of incoming signals