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Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid-Argon Calorimeters

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The Large Hadron Collider (LHC) is foreseen to be upgraded during the shut-down period of 2018-2019 to deliver about 3 times the instantaneous design luminosity. Since the ATLAS trigger system, at that time, will not allow an increase of the trigger rate an improvement of the trigger system is required. The ATLAS LAr Calorimeter read-out will therefore be modified and digital trigger signals with a higher spatial granularity will be provided to the trigger. The new trigger signals will be arranged in 34000 so-called Super Cells which achieves a 5-10 better granularity than the trigger towers currently used and allows an improved background rejection.

The Super Cell read-out is composed of custom developed 12-bit combined SAR ADCs in 130 nm CMOS technology which will be installed on-detector in a radiation environment and digitizes the detector pulses at 40 MHz. The data will be transmitted to the back-end using a custom serializer and optical converter applying 5.44 Gb/s optical links. These components are installed on 124 LAr Trigger Driver Boards (LTDB) each handling up to 320 Super Cell channels.

The back-end system will receive the digitized data at a total rate of 25 Tb/s. LAr Digital Processing Boards (LDPBs) equipped with four Arria-10 FPGAs are foreseen to perform digital signal processing in real-time for precise energy reconstruction, pile-up suppression and identification of the correct bunch-crossing time. Each of the 32 LDPBs handles about 1100 Super-Cells on average.

In order to test the full functionality of the future LAr trigger system, a demonstrator set-up has been installed on the ATLAS detector and is operated in parallel to the regular ATLAS data taking during the LHC Run-2. One Front-End Crate (FEC) covering a region of $\Delta\eta \times \Delta\varphi = 1.4 \times 0.4$ of one LAr half-barrel is equipped with two prototype versions of the LTDB using commercial TI ADS5272 ADCs, and the data are received by two prototype LDPB boards implementing Stratix V FPGAs. The LDPBs are operated in a commercial Advanced Telecommunications Computing Architecture (ATCA) shelf system.

The talk will give an overview of the Phase-I Upgrade of the ATLAS LAr Calorimeter readout and of the custom developed hardware including their role in real-time data processing and fast data transfer. Performance results from the prototype boards in the demonstrator system will be reported with first measurements of noise levels and system linearity.

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