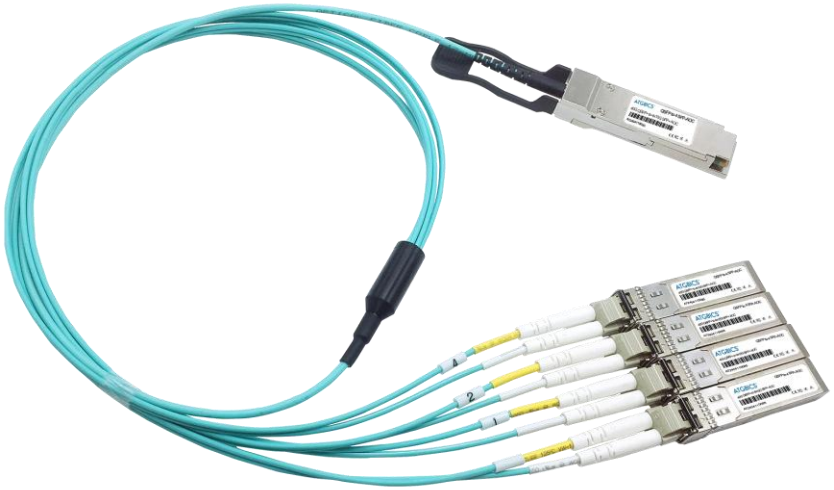


Hardware status report

Boikov A.V

New L2 platform (1)

QSFP to 4 SFP



Alinx z19







New L2 platform (2)

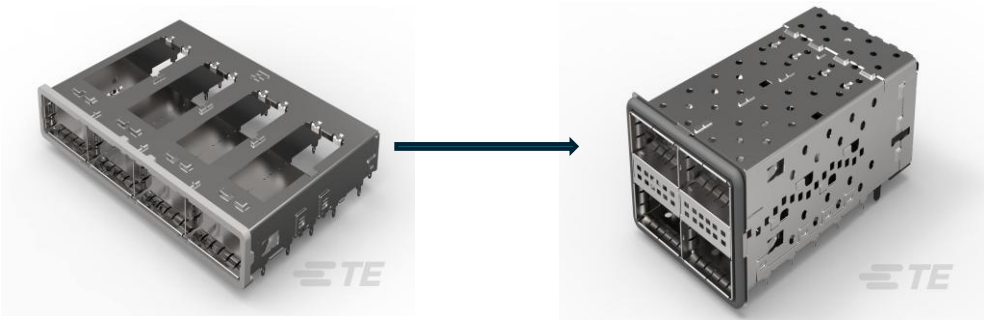
Main changes

- Integrated 4 QSFP transceivers. We can use 16 independent 10G links
- One RG-45 link. Slow control and monitoring

Currently new PCB is under production. One for JINR one for TSU

Next step

Change type of QSFP cage



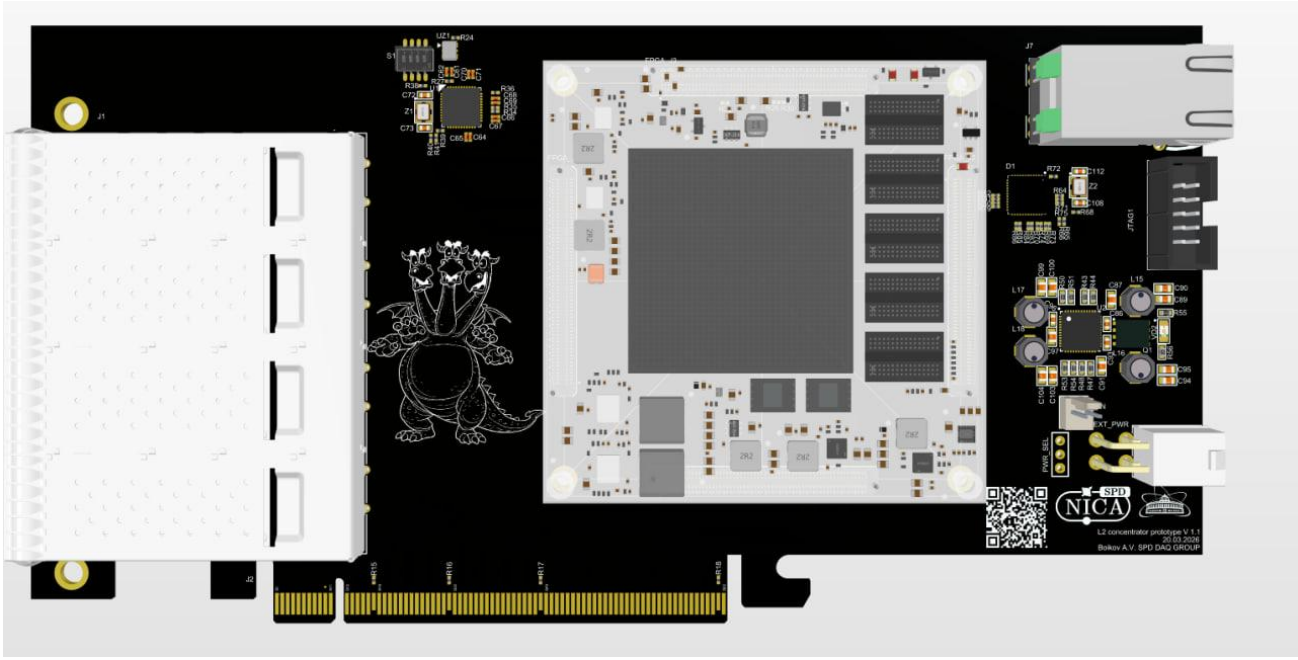
Will use an SFP module instead of standard RG-45. And place on the front panel



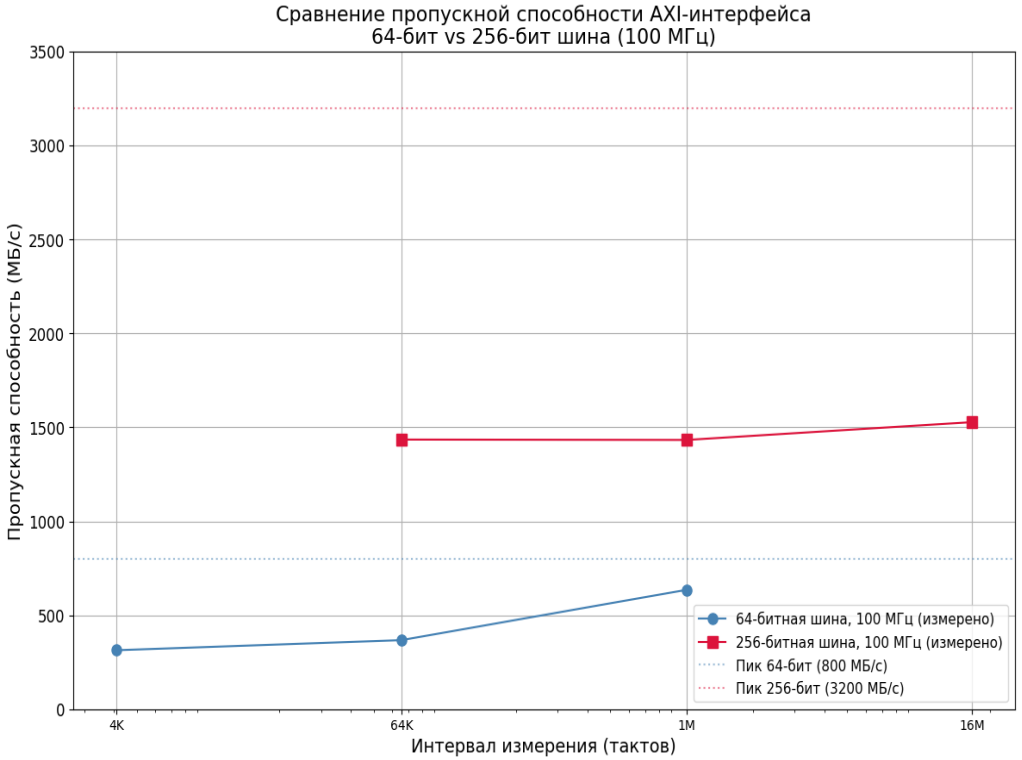
L2 without SOM???

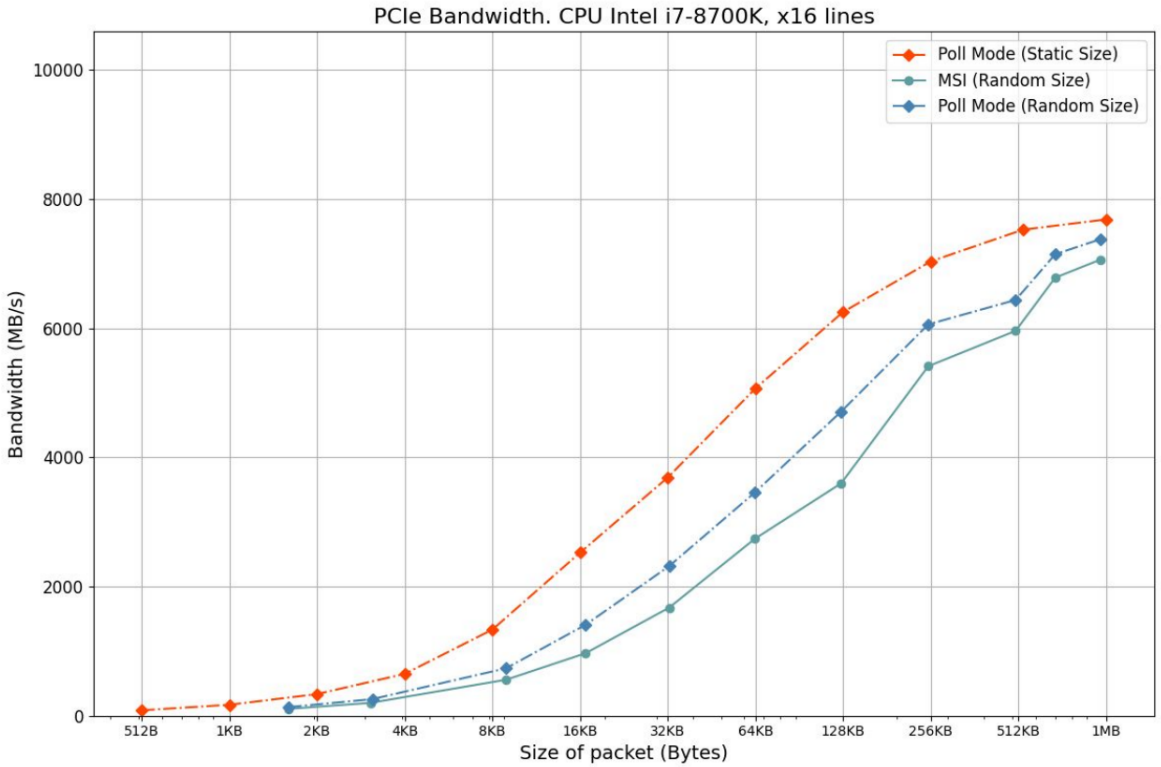
- ACKU15 FPGA SoM with AMD Kintex Ultrascale+™ XCKU15P
- 10 GByte (80-bit) DDR4 SDRAM
- 2 x 64MB QSPI Flash
- 1 x PCIe® Gen3 ×16
- 12V single supply
- Dimension: 80 x 80mm form factor
- Gigabit transceivers
  - 32 x GTH, up to 16.3 Gbps
  - 24 x GTY, up to 28.21 Gbps





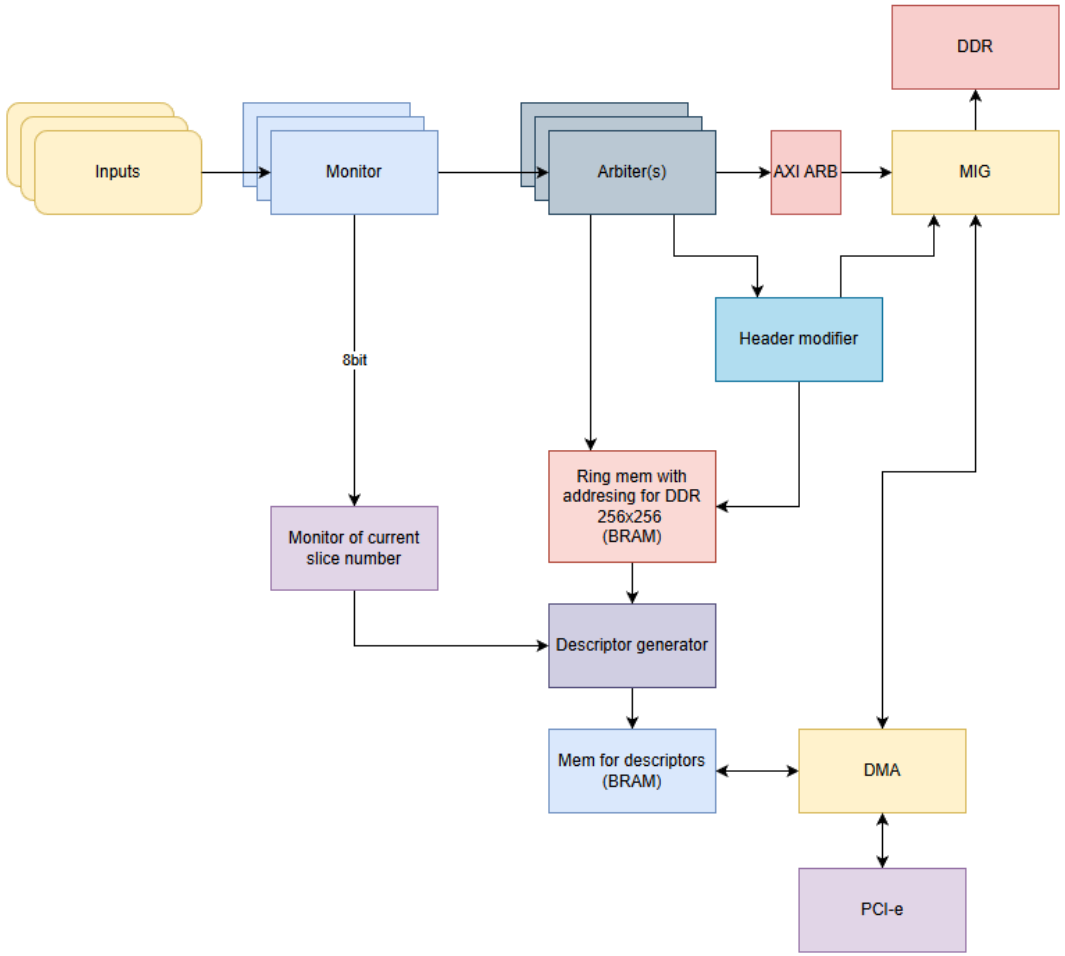
DDR test’s

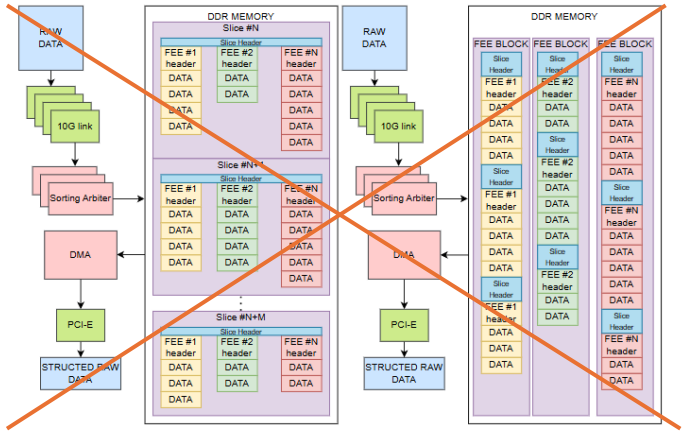

Сравнение пропускной способности AXI-интерфейса
64-бит vs 256-бит шина (100 МГц)
Пропускная способность (МБ/с)
Интервал измерения (тактов)
3500
3000
2500
2000
1500
1000
500
0
4K
64K
1M
16M
64-битная шина, 100 МГц (измерено)
256-битная шина, 100 МГц (измерено)
Пик 64-бит (800 МБ/с)
Пик 256-бит (3200 МБ/с)

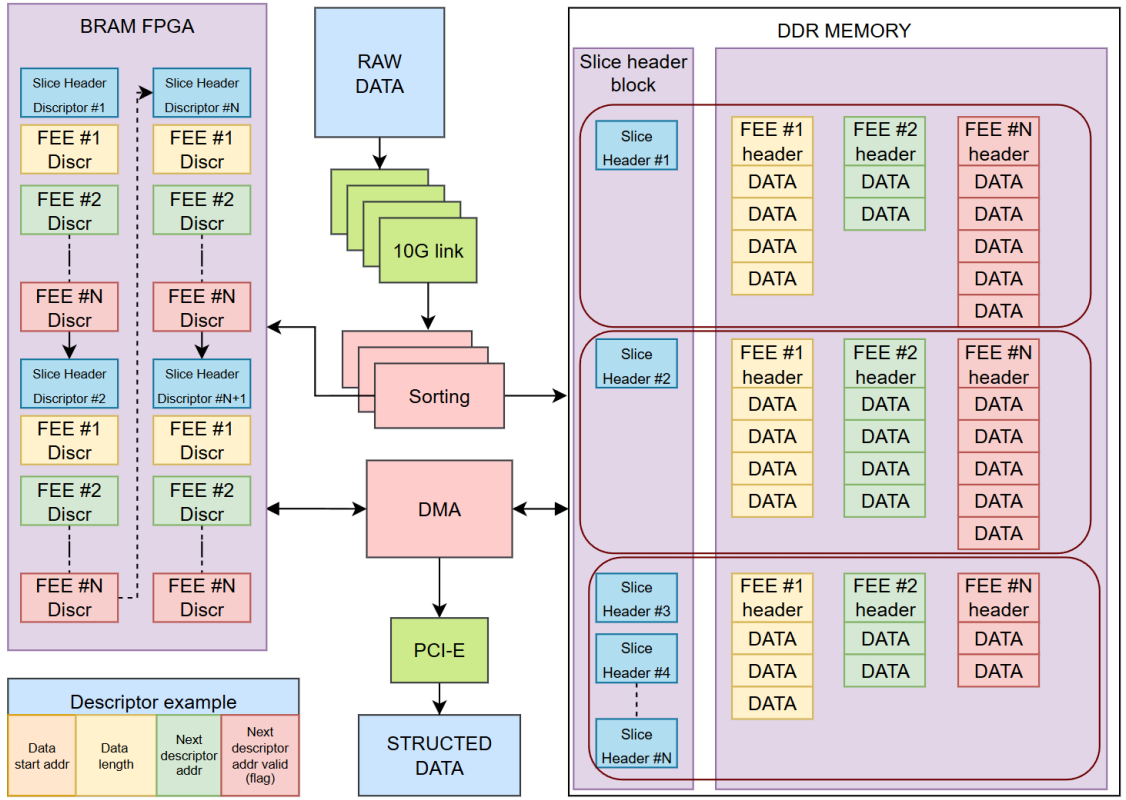

PCIe Bandwidth. CPU Intel i7-8700K, x16 lines
Bandwidth (MB/s)
Size of packet (Bytes)
10000
8000
6000
4000
2000
0
512B
1KB
2KB
4KB
8KB
16KB
32KB
64KB
128KB
256KB
512KB
1MB
Poll Mode (Static Size)
MSI (Random Size)
Poll Mode (Random Size)

New data clustering concept

Use *DMA Scatter Gather* mechanism for data sorting







Long Mini SAS cable test

Test setup

- 2x MiniSAS 1.5 m cable
- 1x SAS 2m cable
- MiniSAS to SAS converter (passive PCB)
- Two test boards with E-link



A stable connection with a speed of 1250 Mbps without 8b10b encoding and 1 Gbps with 8b10b encoding in CDR mode on the L1 hub was achieved.





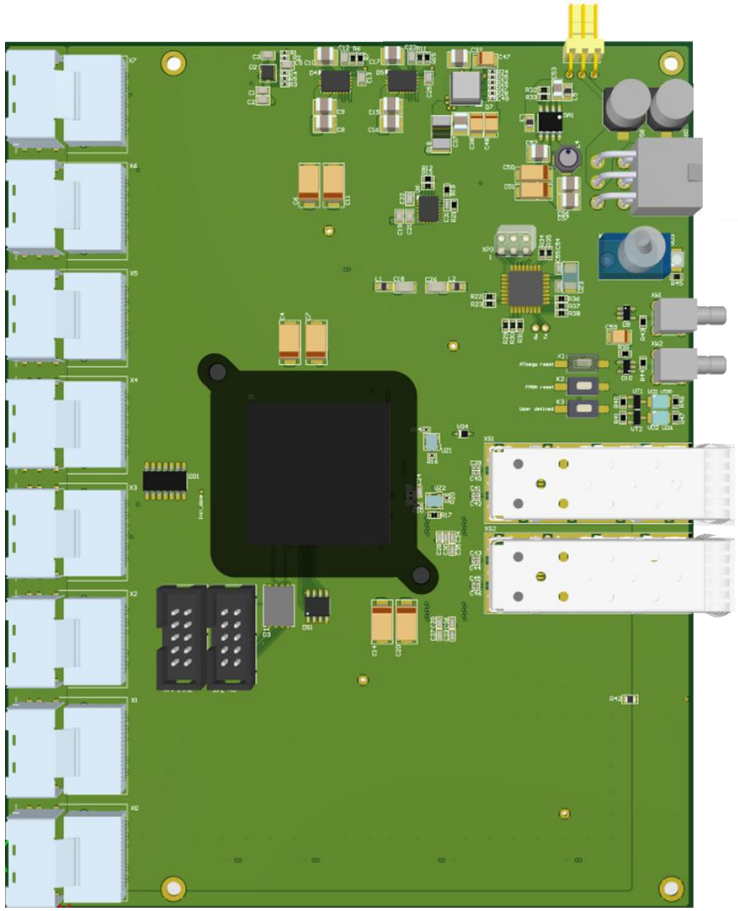
Mini SAS



Pin function	Side B Pin	Side A Pin	Pin function
GND	B1	A1	GND
Tx0+	B2	A2	Rx0+
Tx0-	B3	A3	Rx0-
GND	B4	A4	GND
Tx1+	B5	A5	Rx1+
Tx1-	B6	A6	Rx1-
GND	B7	A7	GND
Unipolar 0	B8	A8	Unipolar 7
Unipolar 1	B9	A9	Unipolar 3
Unipolar 2	B10	A10	Unipolar 4
Unipolar 6	B11	A11	Unipolar 5
GND	B12	A12	GND
Tx2+	B13	A13	Rx2+
Tx2-	B14	A14	Rx2-
GND	B15	A15	GND
Tx3+	B16	A16	Rx3+
Tx3-	B17	A17	Rx3-
GND	B18	A18	GND

Additional

The final technical information for the White Rabbit L1 node is expected to be released soon to complete the development.☺



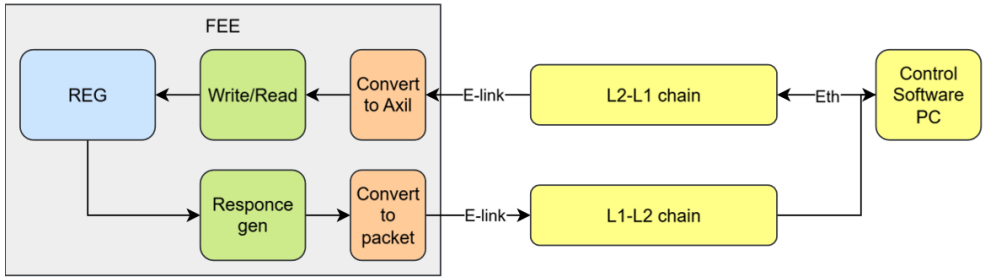
P **pkt-to-axil**

main · pkt-to-axil · + · Find file · Code

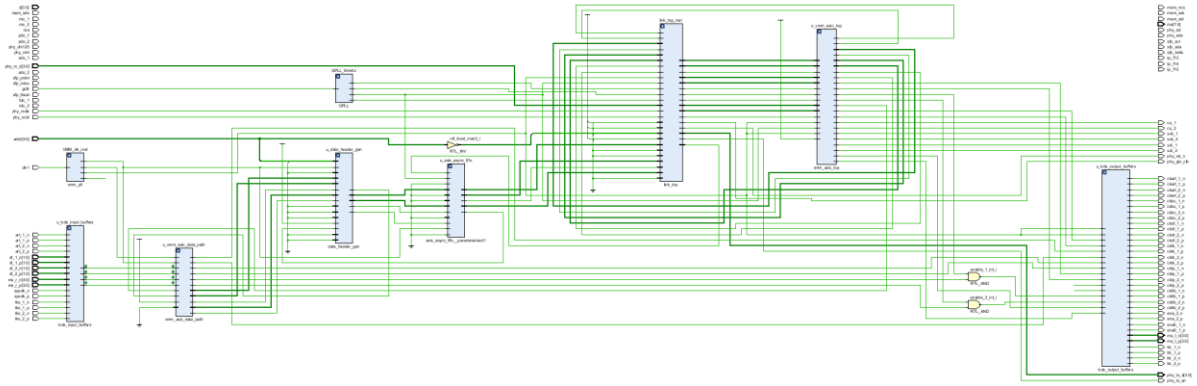
add manifest
Aleksandr Boikov authored 2 weeks ago · 1bdb5fa0 · History

Name	Last commit	Last update
RDL_regmap	fix valid signal	1 month ago
rtl	fix valid signal	1 month ago
test_regmap	fix resp generation in testreg and binder	1 month ago
tests	fix valid signal	1 month ago
Manifest.py	add manifest	2 weeks ago
README.md	all type transaction is supported. No erro...	1 month ago

```
89990.02ns INFO     cocotb
90990.02ns INFO     cocotb.regression
90990.02ns INFO     cocotb.regression
                    Reset completed - все сигналы сброшены
                    test_mixed_combinations_size_10 passed
                    ********************************************************************************************************************
                    ** TEST                                                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                    ********************************************************************************************************************
                    ** pkt2axil_test.test_write_response                             PASS         610.00           0.02     38949.73  **
                    ** pkt2axil_test.test_multiple_packets_with_varying_write_transactions  PASS       17180.00           0.13    131558.03  **
                    ** pkt2axil_test.test_four_writes_then_four_reads                PASS        1060.00           0.01     79380.92  **
                    ** pkt2axil_test.test_write_then_read_after_delay               PASS         900.00           0.01    149897.86  **
                    ** pkt2axil_test.test_multiple_writes_then_reads                PASS        1600.00           0.01    131870.52  **
                    ** pkt2axil_test.test_multiple_write_read_cycles                PASS        2550.00           0.02    121824.72  **
                    ** pkt2axil_test.test_ten_writes_then_ten_reads                 PASS        2020.00           0.02    100694.05  **
                    ** pkt2axil_test.test_write_ten_then_read_varying_sizes         PASS       18010.00           0.13    136958.18  **
                    ** pkt2axil_test.test_mixed_read_write_combinations             PASS        5110.00           0.05    101753.73  **
                    ** pkt2axil_test.test_mixed_combinations_size_2                 PASS        2220.00           0.02    124313.89  **
                    ** pkt2axil_test.test_mixed_combinations_size_3                 PASS        3700.00           0.03    117969.81  **
                    ** pkt2axil_test.test_mixed_combinations_size_4                 PASS        6460.00           0.05    117802.18  **
                    ** pkt2axil_test.test_mixed_combinations_size_5                 PASS        4600.00           0.04    115742.44  **
                    ** pkt2axil_test.test_mixed_combinations_size_6                 PASS        4370.00           0.04    117223.05  **
                    ** pkt2axil_test.test_mixed_combinations_size_7                 PASS        4670.00           0.04    107440.10  **
                    ** pkt2axil_test.test_mixed_combinations_size_8                 PASS        4980.00           0.04    110041.50  **
                    ** pkt2axil_test.test_mixed_combinations_size_9                 PASS        5320.00           0.05    103851.32  **
                    ** pkt2axil_test.test_mixed_combinations_size_10                PASS        5630.00           0.06    100846.16  **
                    ********************************************************************************************************************
                    ** TESTS=18 PASS=18 FAIL=0 SKIP=0                                    90990.02           0.90    101269.72  **
                    ********************************************************************************************************************
make[1]: Leaving directory '/mnt/g/SPD/Micromegas/micromegas-fee-firmware/core/pkt-to-axil/tests'
(venv) boikov@WORKBOIKOV:/mnt/g/SPD/Micromegas/micromegas-fee-firmware/core/pkt-to-axil/tests$
```



MM FEE



Change FPGA: Pangomicro Logios 2 → XILINX ARTIX 7

Thanks V.Bautin !!



