MPD & BM@N Data Acquisition Systems

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MPD & BM@N DAQ Collaboration

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The second Collaboration meeting of the MPD and BM@N
experiments at the NICA Facility

Outline

- DAQ Intro
- DAQ Architecture
- Readout Electronics
- DAQ Technical Network
- IT Infrastructure

For more details please proceed to >>> MPD DAQ TDR

MPD Data Acquisition System

Properties

Reliable data transfer. Pipeline operation with synch and async stages.
Extensive diagnostics in hardware and software. Monitoring, logging.
Data integrity check on all levels. CRC, sequence numbers, FEC.
Fault tolerant, Highly available. Fast self recovery after SEU events.
Distributed, scalable, extendable. Based on open and industry standards.
Flexible architecture. Partitioning for independent subsystem operation.

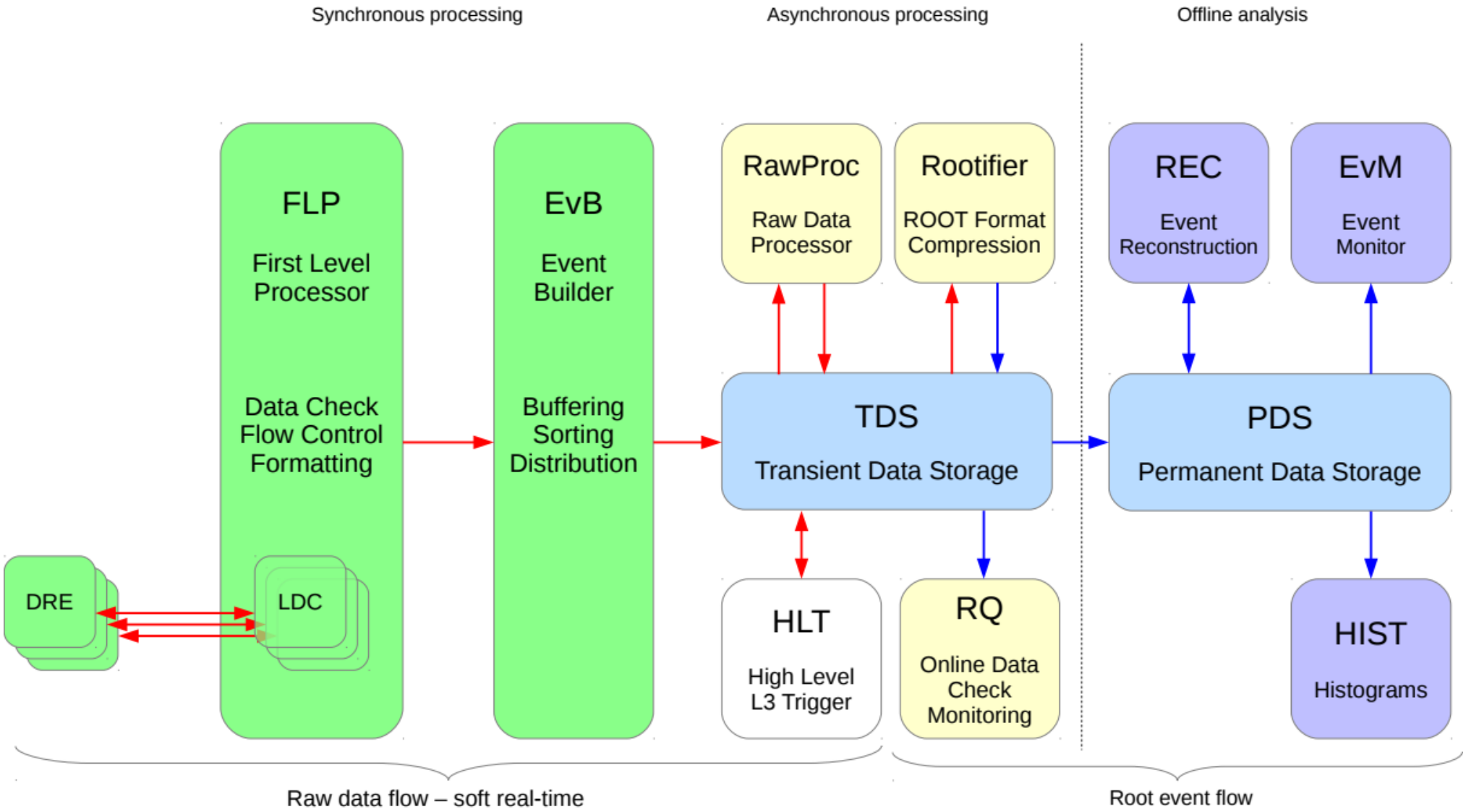
Operation Modes

Multiple hardware trigger classes
Uncompressed, full raw data during MPD commissioning
Large calibration data events at low trigger rate
High multiplicity events from central collisions at planned trigger rate

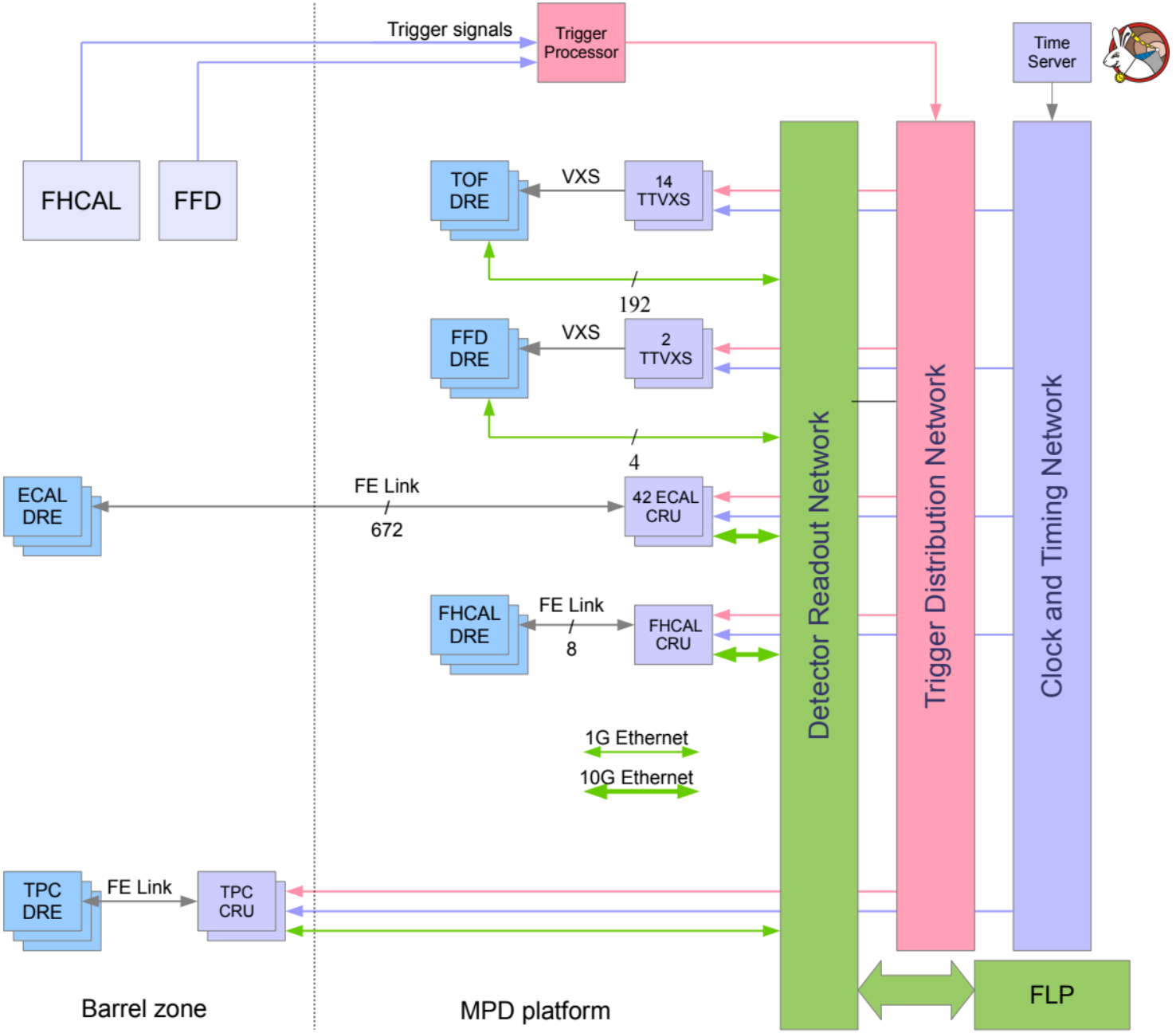
DAQ in numbers

Up to 7 kHz trigger rate, over 1 MB compressed event size to storage device
From 5 to 30 GB/s uncompressed raw data rate from readout cards to FLP
Approx. 200 TB in 2020 to 20 PB in 2023 annual stored data size

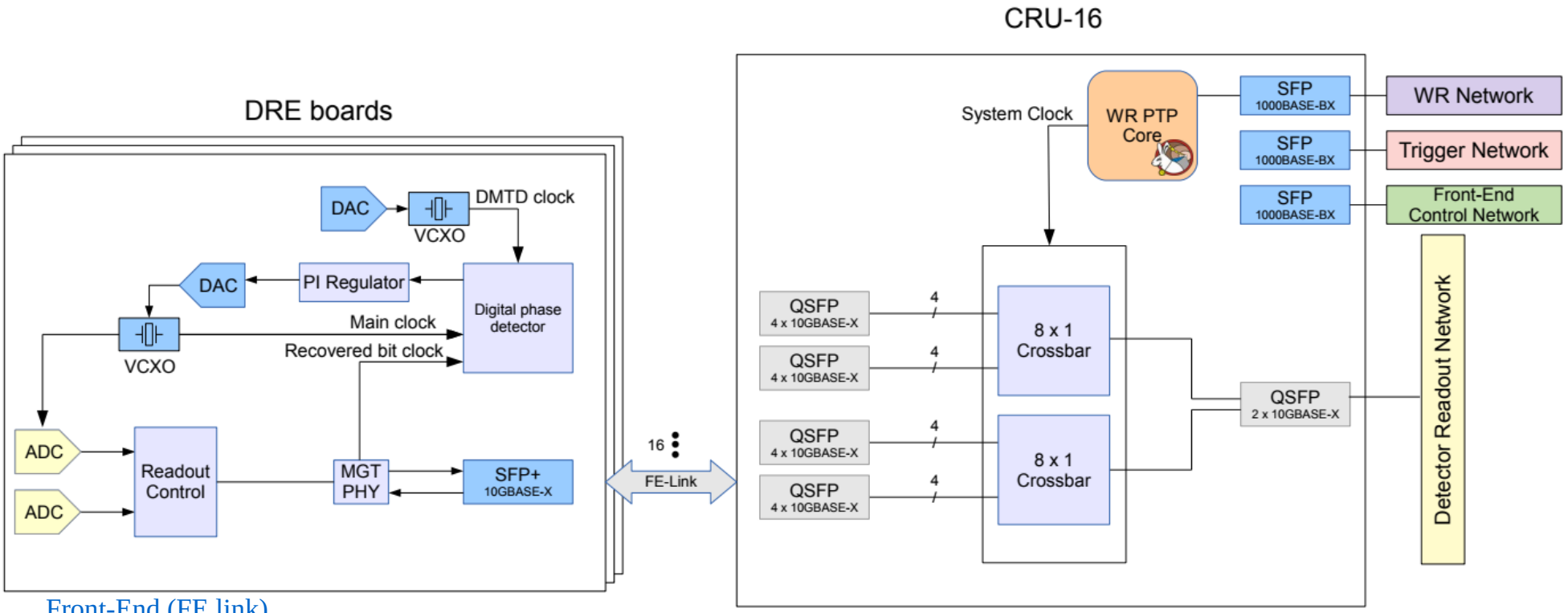
MPD Data Flow



MPD DAQ Hardware



Common Readout (and everything else) Unit



Front-End (FE link)

"Variable-speed Synchronous Ethernet". Byte-oriented, 8b/10b Ethernet like encoding and framing

Maximum data rate: 2.5 Gb/s VXS backplane (TTVXS), 8 Gb/s (CRU-16) with commercial QSFP fiber-optical transceivers.

DRE clock synchronized to CRU with digital PLL. Short fixed cables – one time delay calibration.

Timestamps, trigger, data readout, control over same link

No TCP-IP stack complexity in DRE. Simple FGPA code with fail-safe FSM and data pipelines to mitigate SEU events.

Aggregation *"switch"* (CRU-16 core)

Not an Ethernet switch. Fixed traffic directions: left-right or right-left only. Connects to DAQ network with 10G Ethernet, UDP-IP.

Large FPGA on board running White Rabbit and service CPUs

Extensive diagnostics: hardware histograms, RAM-based multichannel counters

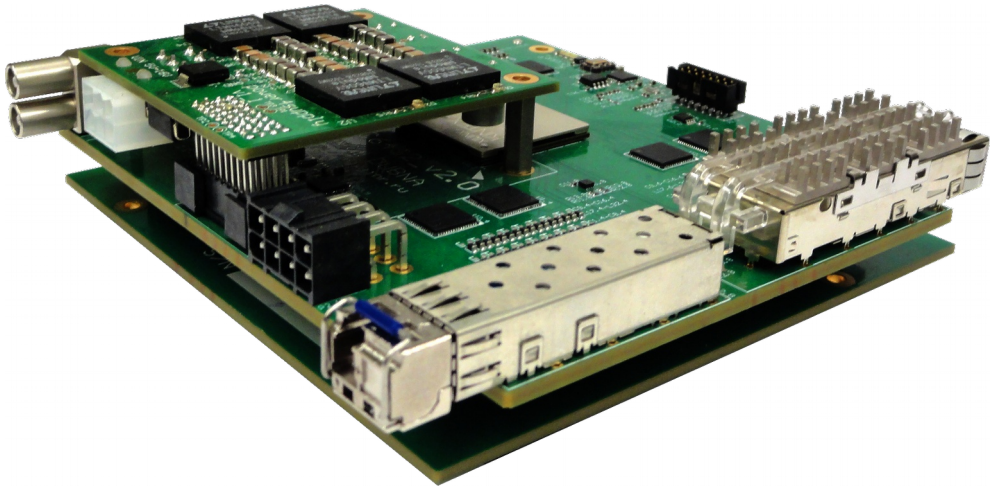
Use speed translation FIFOs. Arbitrated crossbars. Option for large DRAM buffer on board

Future: hardware event merging for connected DRE boards

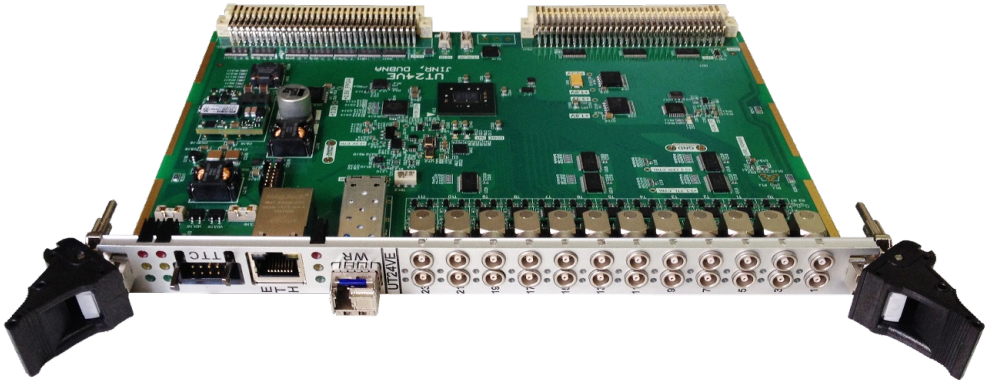
DAQ Electronics – made in Dubna

Timestamping TDC – TOF, FFD, T0

PCI-Express Fiber-optical Interface

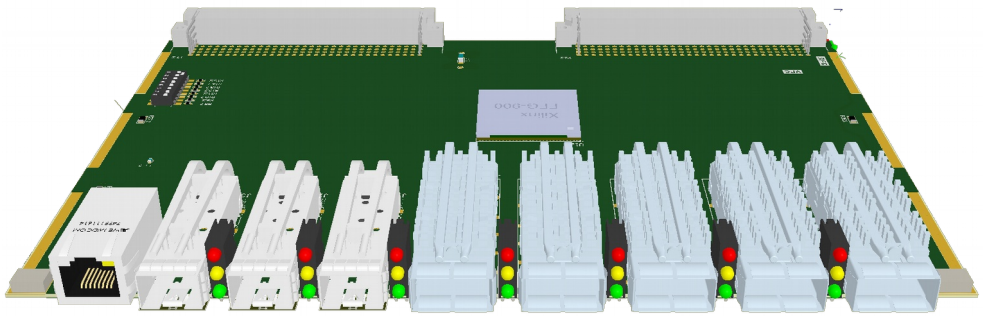


Waveform Digitizer – ECal, ZDC



Trigger Distribution and Control

New! DAQ Electronics – designed in Dubna

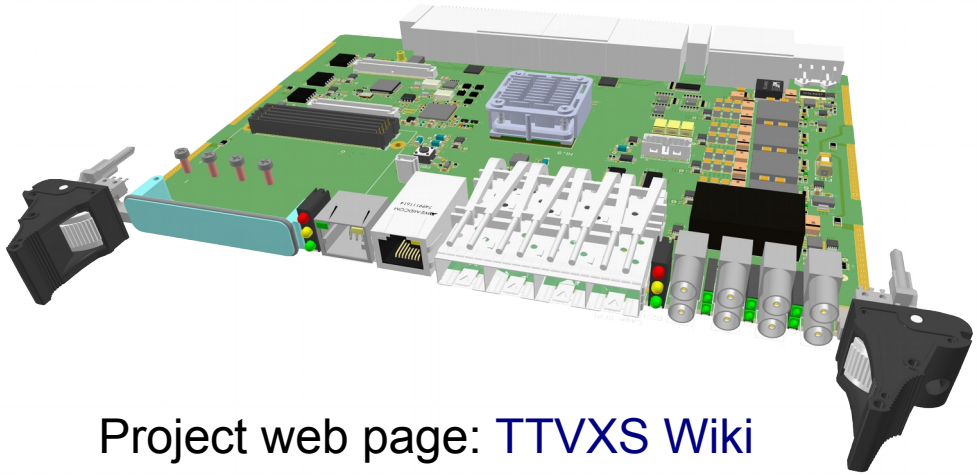


CRU-16 – Common Readout Unit

- 16 FE links to readout boards (QSFP breakout)
- 10 Gb/s Ethernet link to FLP (up to 4•10G)
- Trigger, Timing (WR), Management ports

Status: PCB, FPGA, software design phase

Usage at MPD: ECal, FHCal, ...



Project web page: TTVXS Wiki

TTVXS – Trigger, Timing, RC

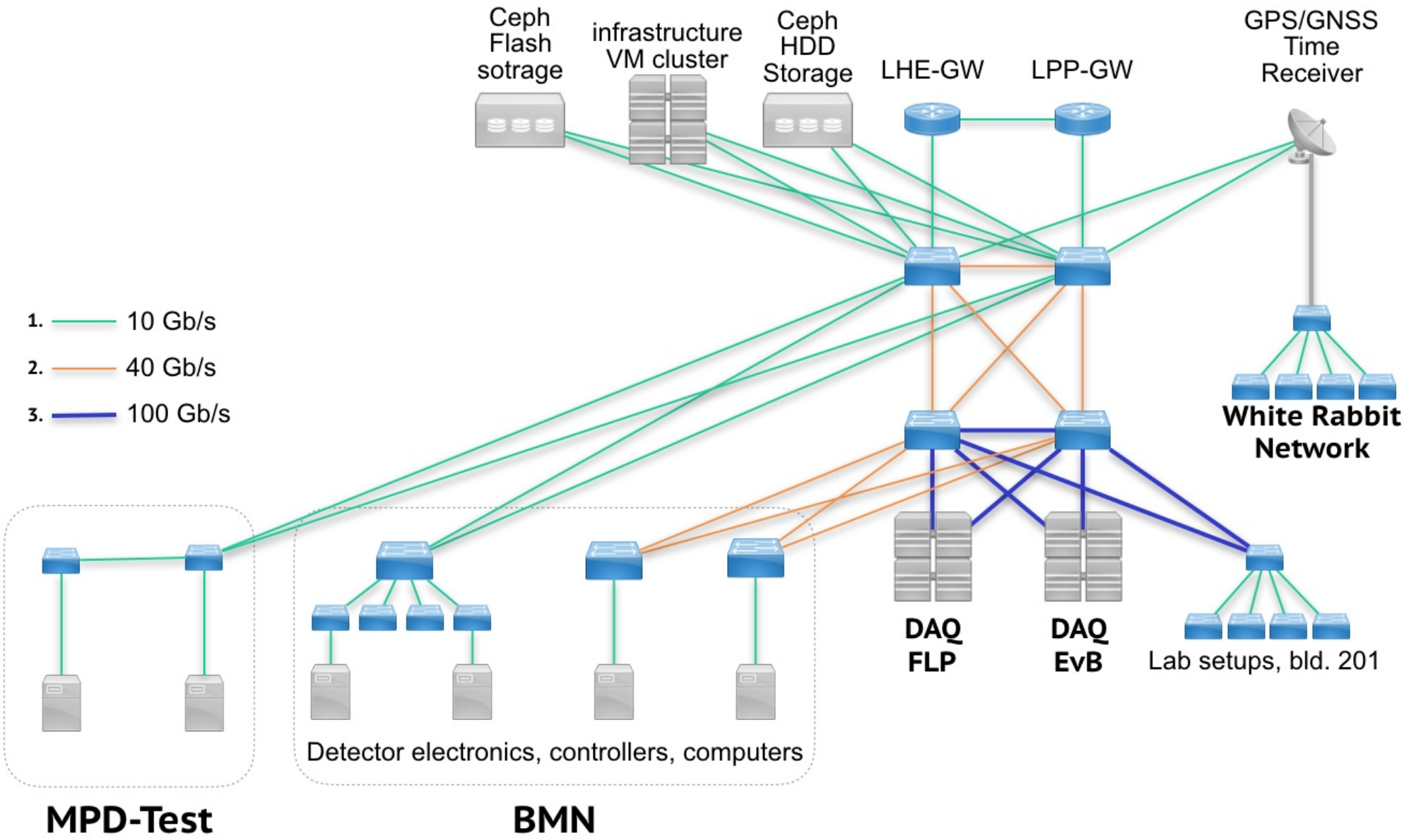
- Supports 18 VXS payload boards
- Trigger, Timing (WR), Management ports
- System monitoring for VXS boards

Replaces FVME2TMWR+UT24VE-RC, eliminates front-panel TTC bus.

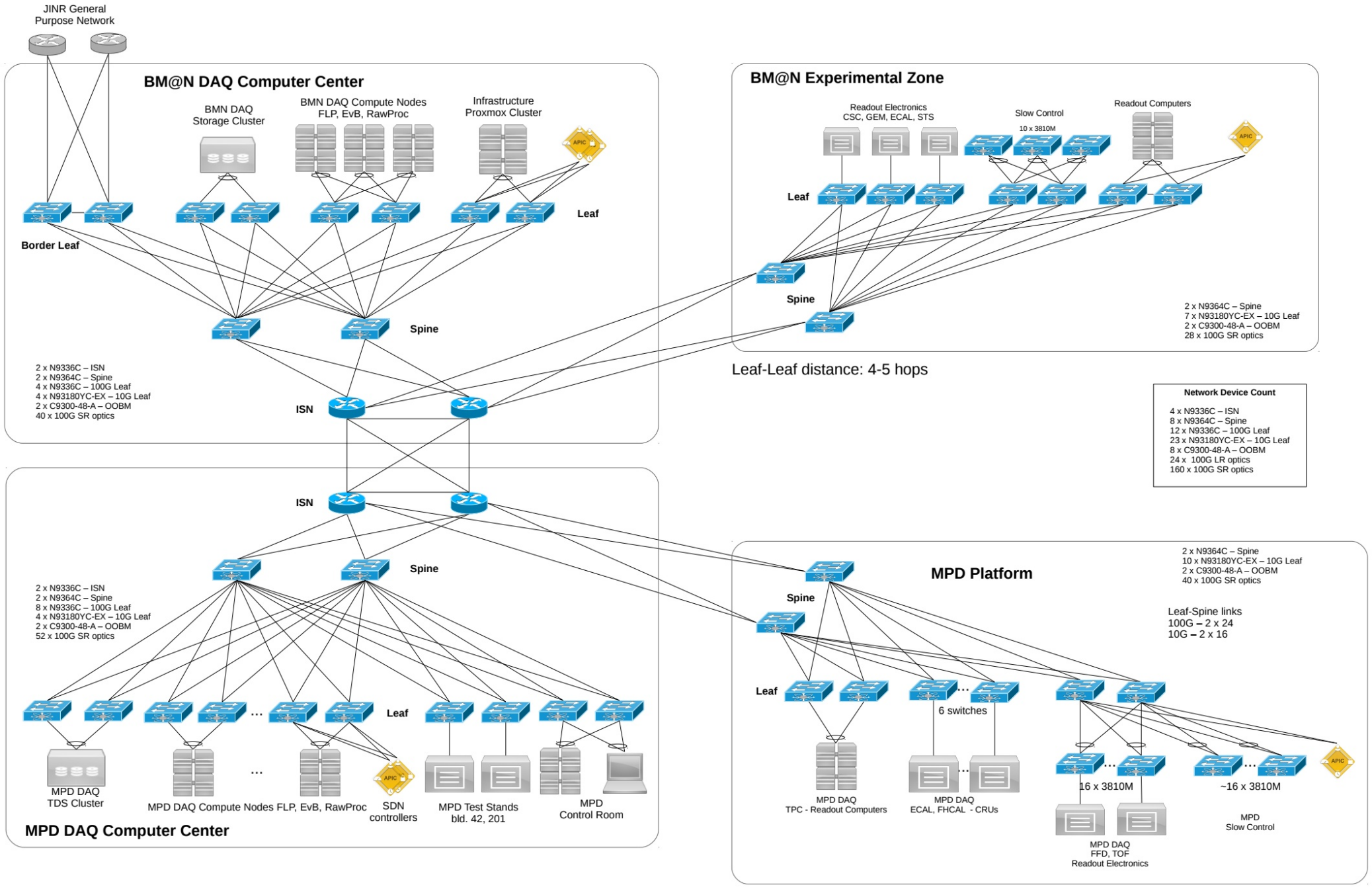
Status: PCB assembled, FPGA and software design. Add-on CPU board design.

Usage at MPD: TOF, FFD

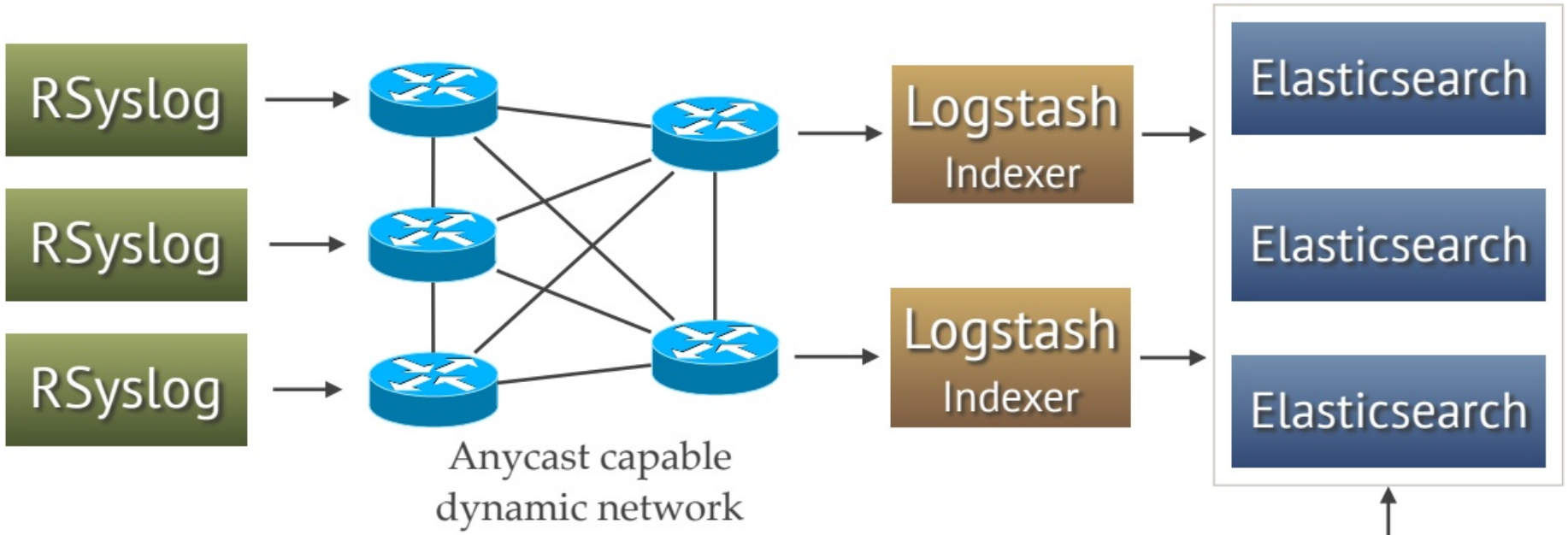
DAQ Technical Network in 2018



DAQ Technical Network – MPD & BM@N



Message Logging and Search



Any input

RFC 5424
RFC 3164
JSON
custom

Structured data

```
@timestamp = …
host = control-01
severity = notice
program = MainControl
message = “Starting Run”
```

DAQ IT Hardware, 2018

FLP, event builder nodes

16 nodes, each equipped with:

- Two 16-core CPUs (Intel Xeon 2.6 GHz Broadwell)
- 512 GB RAM (16 GB/core)
- 2 x 100 Gb/s network

Network

- Cisco Nexus 5000 / 9000 switches
- Fault tolerant, redundant topology
- Bidirectional multicast capable (DAQ software requirement)

Ceph Flash storage

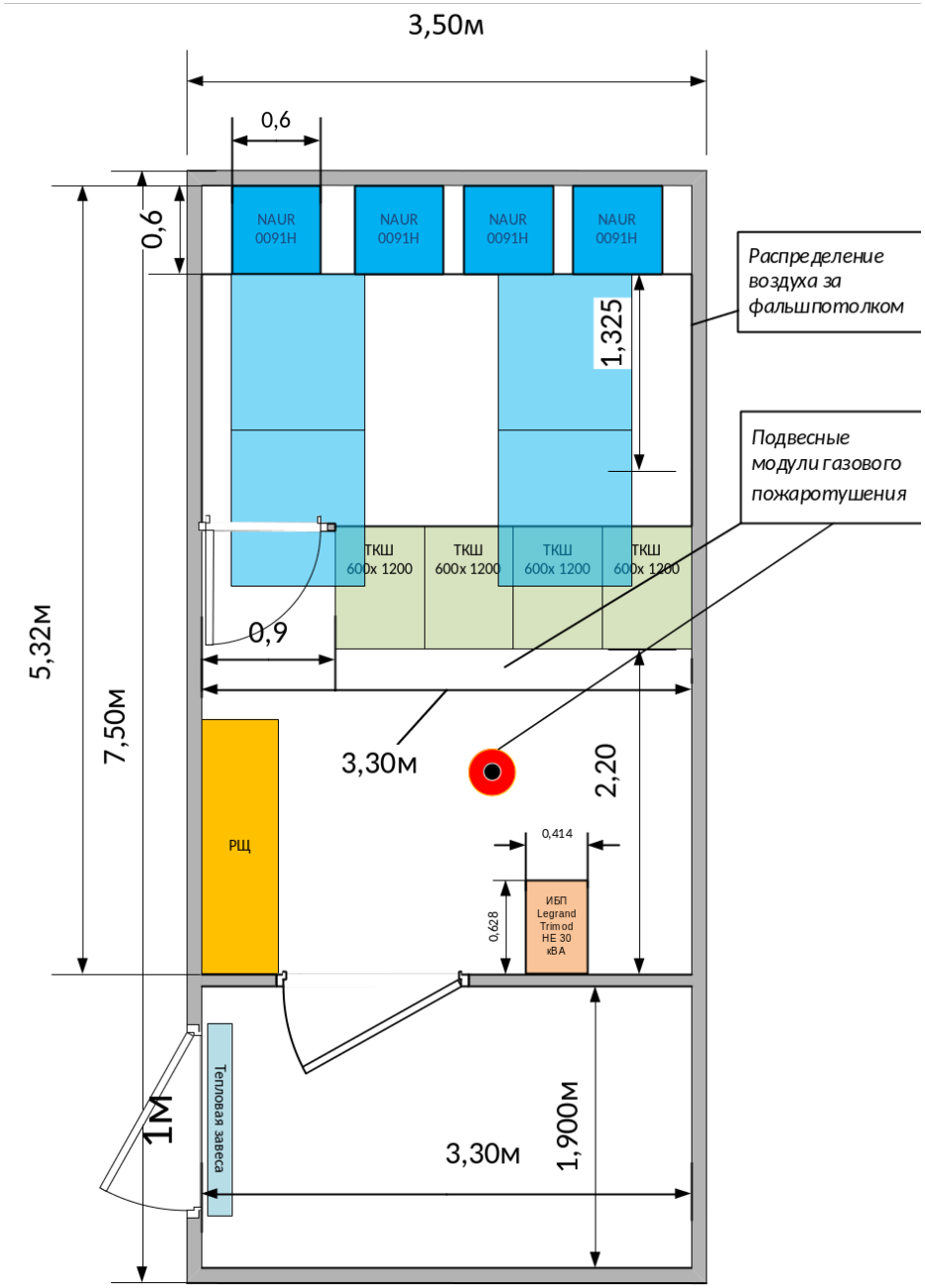
Two clusters with 8 nodes each

- SATA: 6.5 TB useable space
- NVMe: 20 TB useable space
- Houses all virtual machine disks

Ceph HDD storage

- 140 • 4 TB disks in 4 nodes
- 180 TB useable space (3x replicated)
- 4 GB/s read/write aggr. throughput
- Fault tolerant. ~12 HDDs failed in 4 years with no service interruption

BMN DAQ – Mini Data Centre



Specifications	
Input power	50 kW
IT power	24 kW (N+1) / 30 kW max
Rack count	4 racks
Redundancy	N+1 (UPS, HVAC)
Battery backup	8 minutes
Rack size	600 x 1200 x 42U

Equipment	Rack Units
Passive network	16
Active network (switches, controllers)	12
VMEDAQ nodes	16
FLP, Event Builder nodes	20
Transient Flash Storage	13
Persistent Disk Storage	35
Message Logging and Search	5
Reserve	51

Thank you!

Extra slides

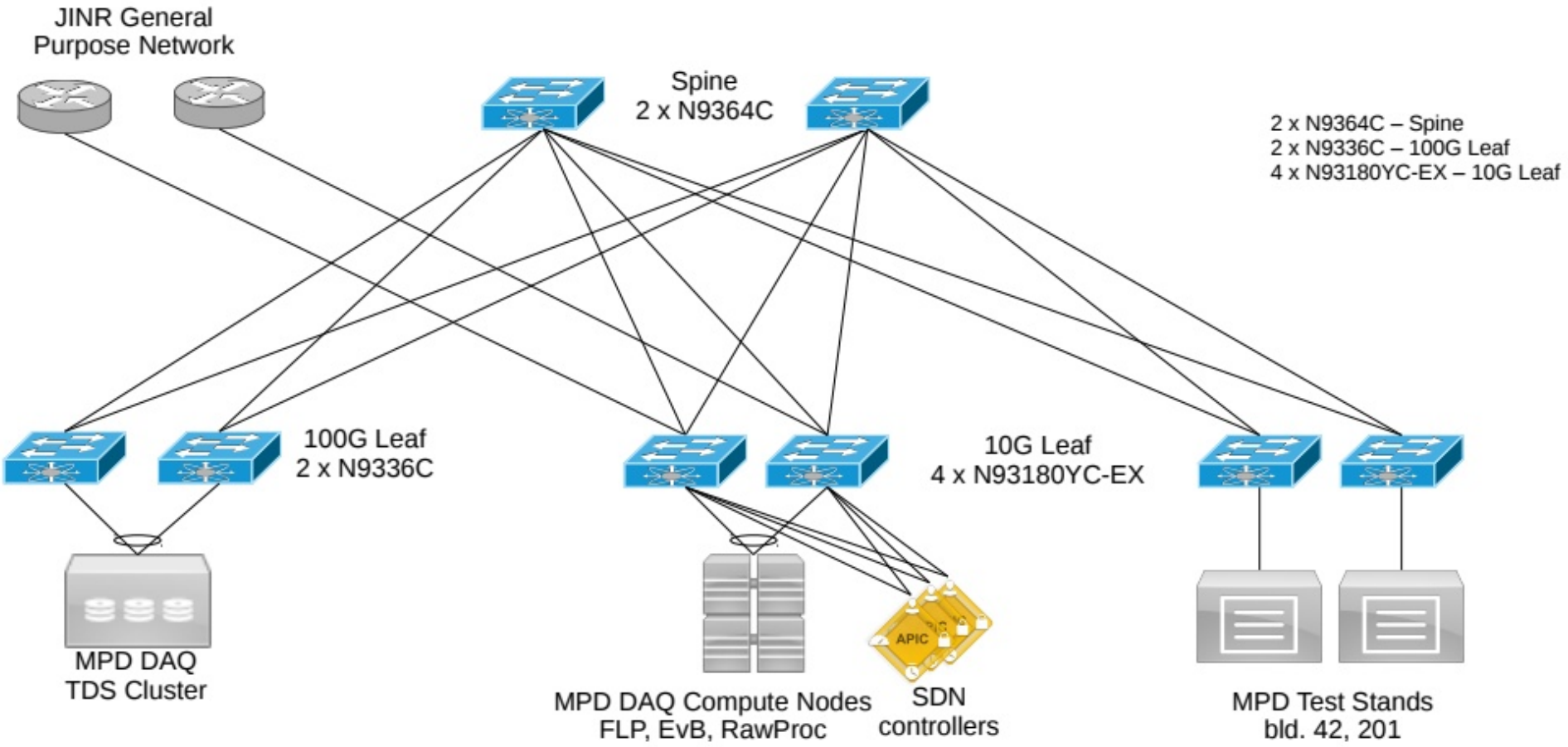
BMN DAQ parameters

	March 2017	Mar–Apr 2018	2020 – 2021
Raw event size, Bytes	120 000	225 000	~ 300 000
Trigger rate	5k	10k	20k / 50k
Before / After Protection	none	3 μs / 0.5 μs	
DAQ missed triggers	> 50 %	< 15%	
GEM / STS / CSC zero suppression	none (Off-line)	none (Off-line)	On-line
Event readout time	100 – 300 μs	35 μs	15 μs
Total raw data volume	7.6 TiB	66.4 TiB	150 – 500 TiB
DAQ FLP network bandwidth	20 Gb/s	90 Gb/s	800 Gb/s

Readout and Control Electronics

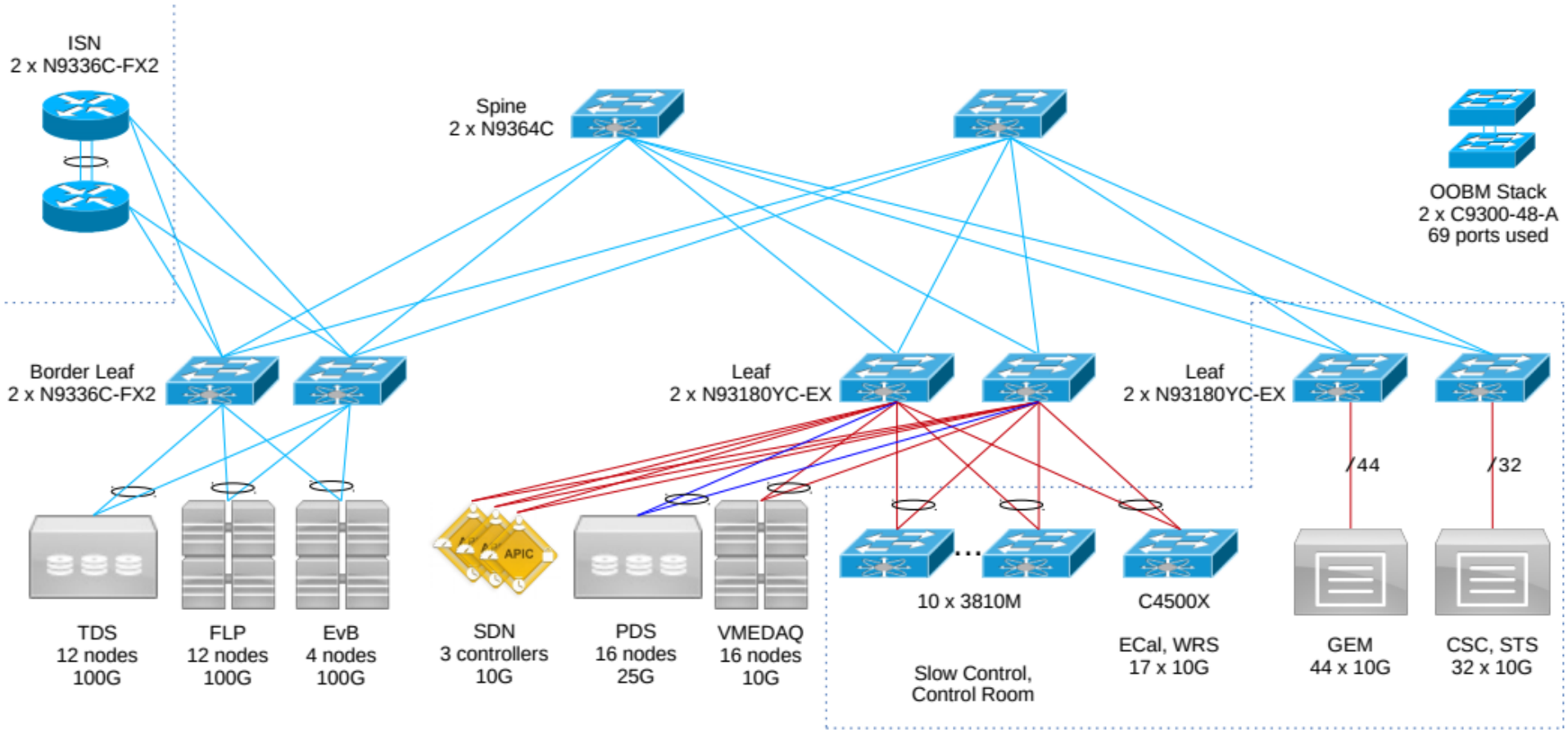
Detector	DAQ Function	Readout card	Standard	Readout
BMN GEM, CSC, STS (prototype)	Charge, 32 or 128 channel multiplexed readout + waveform digitizer	VME ADC64VE-10GE	VME64x	Ethernet 10G
BMN TOF-400, T0 — MPD TOF	Two-edge Pulse Timestamping	VXS TDC72VHE – 25 ps TDC	VXS	VME64 — Ethernet
BMN TOF-700	Two-edge Pulse Timestamping	TDC64VHLE – 25 ps TDC	VXS	VME64
BMN DCH	Pulse Timestamping	TDC64VL – 100 ps TDC	VME64x	VME64
BMN ECal, ZDC — MPD ECal	Charge, waveform digitizer with DSP	ADC64S2 v5.0	standalone	Ethernet
Time Synchronization	WR Time receiver, VME clock distribution	FVME2-TMWR	VXS	Ethernet
Control and Monitoring	UT24VE-RC	UT24VE-RC	VME64	Ethernet
Interfaces	VME control and readout	FVME2, PEXML-4	VME64, PCIe	PCI-Express

MPD DAQ Network, 2019



Status: Design complete. Equipment delivery expected Q1-2019.

BMN DAQ Network, 2019–2020



Status: Design complete. Equipment delivery expected Q1-2019.

BMN DAQ setup in March 2018