

Laboratory
of High Energy Physics
Data Analysis

Tomsk
State
University

Status of the L2 hub development

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The study was carried out within the framework of the state assignment of the Ministry of Science and Higher Education of the Russian Federation (project No. FSWM-2025-0023).

Reminder: L2 hub positioning in the DAQ

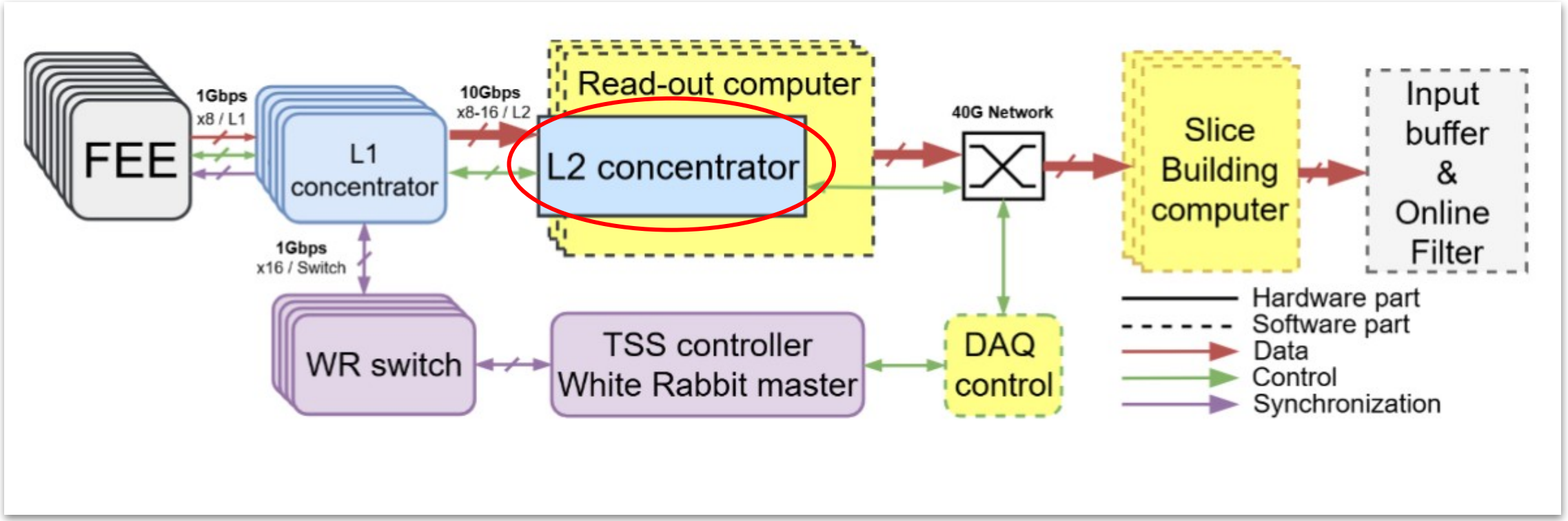


Fig. 1 Position of the L2 hub in the DAQ.

L2 hub: Current architecture

Tasks:

1. Combine 8-16 data streams into one
2. Perform data sorting
3. Send and receive control and monitoring commands

Since about 2024, the L2 hub has been developed on this architecture to fulfill the assigned tasks. We are now moving to a slightly different architecture.

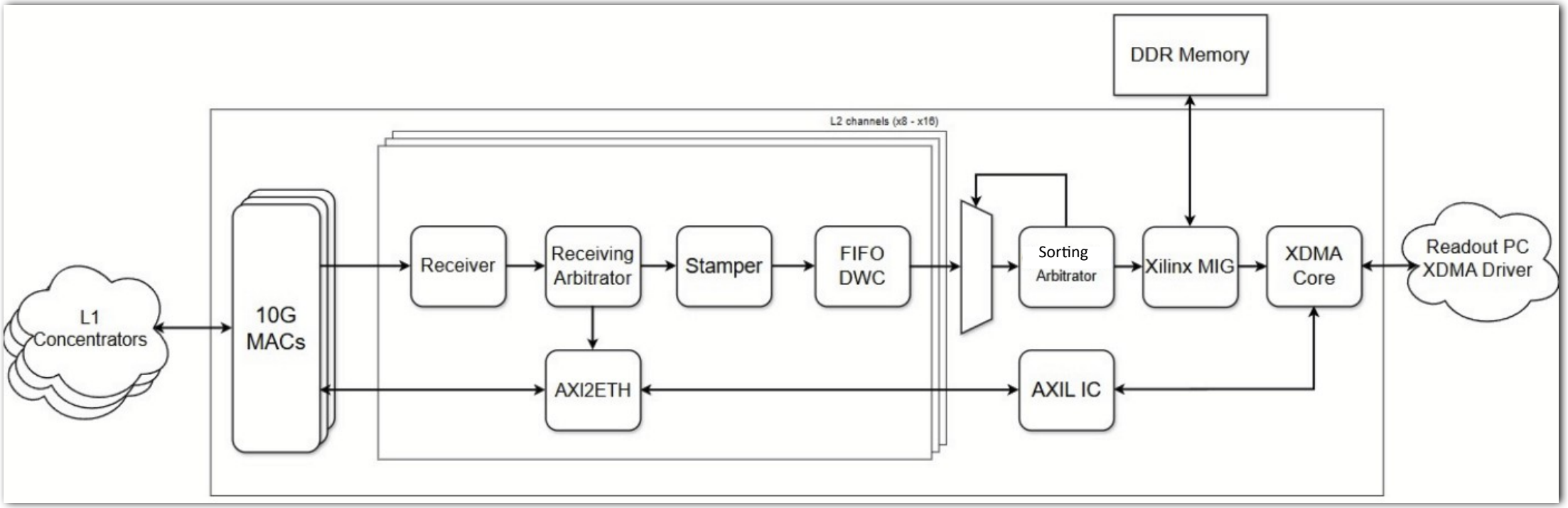


Fig. 2 Current architecture of the L2 hub (FPGA firmware)

L2 hub: New architecture

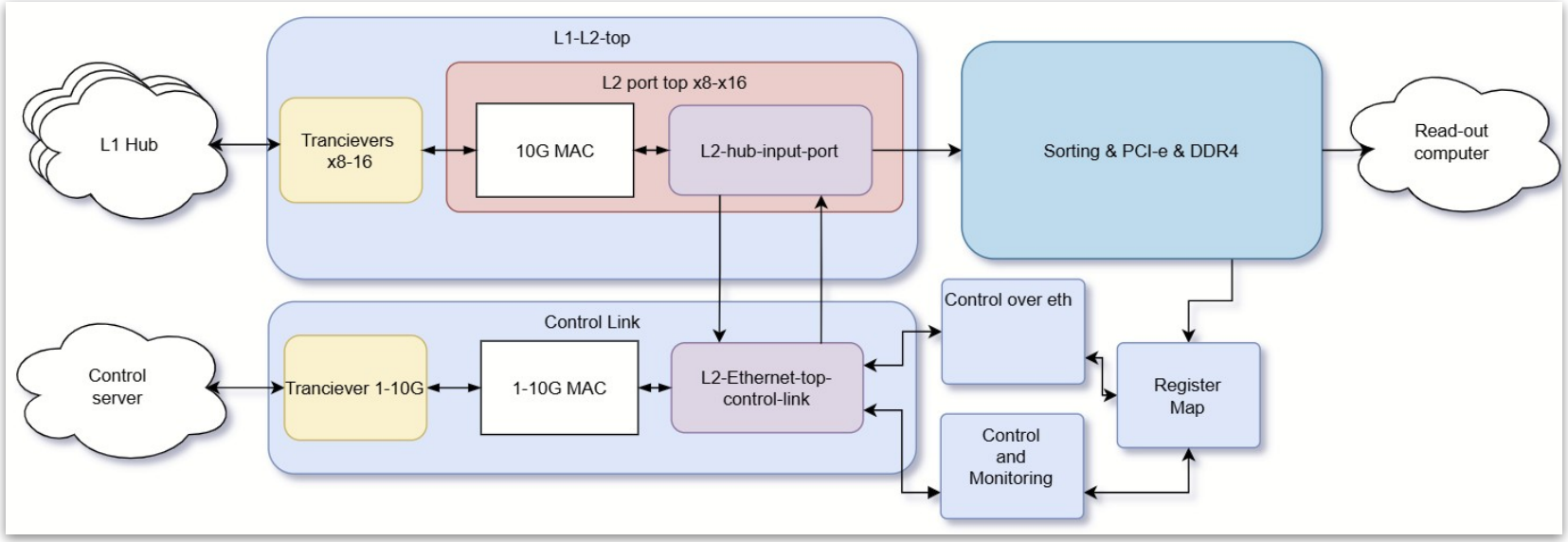


Fig. 3 New architecture of the L2 hub (under development)

The migration to the new architecture is already underway. In the new architecture:

1) New clocking (more PLLs and CDC, to meet timing requirements).
2) A shared Control & Monitoring module.
3) A dedicated Ethernet channel for receiving commands from the server.
3) Support for ARP and UDP (primitives from SPD Firmware Library)
4) New address space.
5) No PS dependances.
6) etc.

L2 hub: Sorting

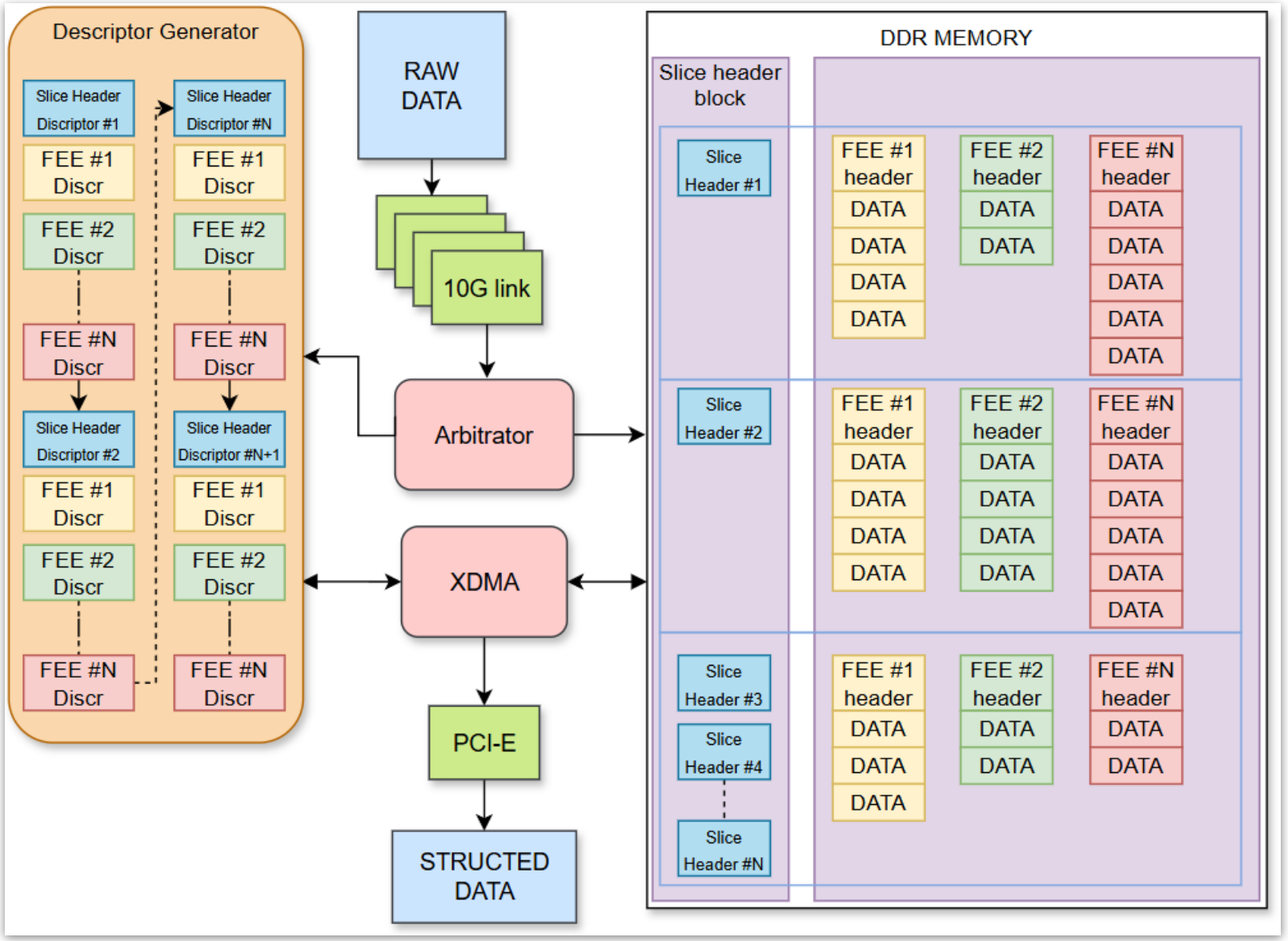


Fig. 4 Simplified sorting architecture

The main challenge is the empty spaces between FEE columns. To solve this, we use a descriptor generator in our design.

Arbitrator is the main sorting module.

The XDMA module sends sorted data from DDR4 to the computer. Descriptors help the XDMA module to send this data in strict order and without any empty spaces.

L2 hub: Sorting

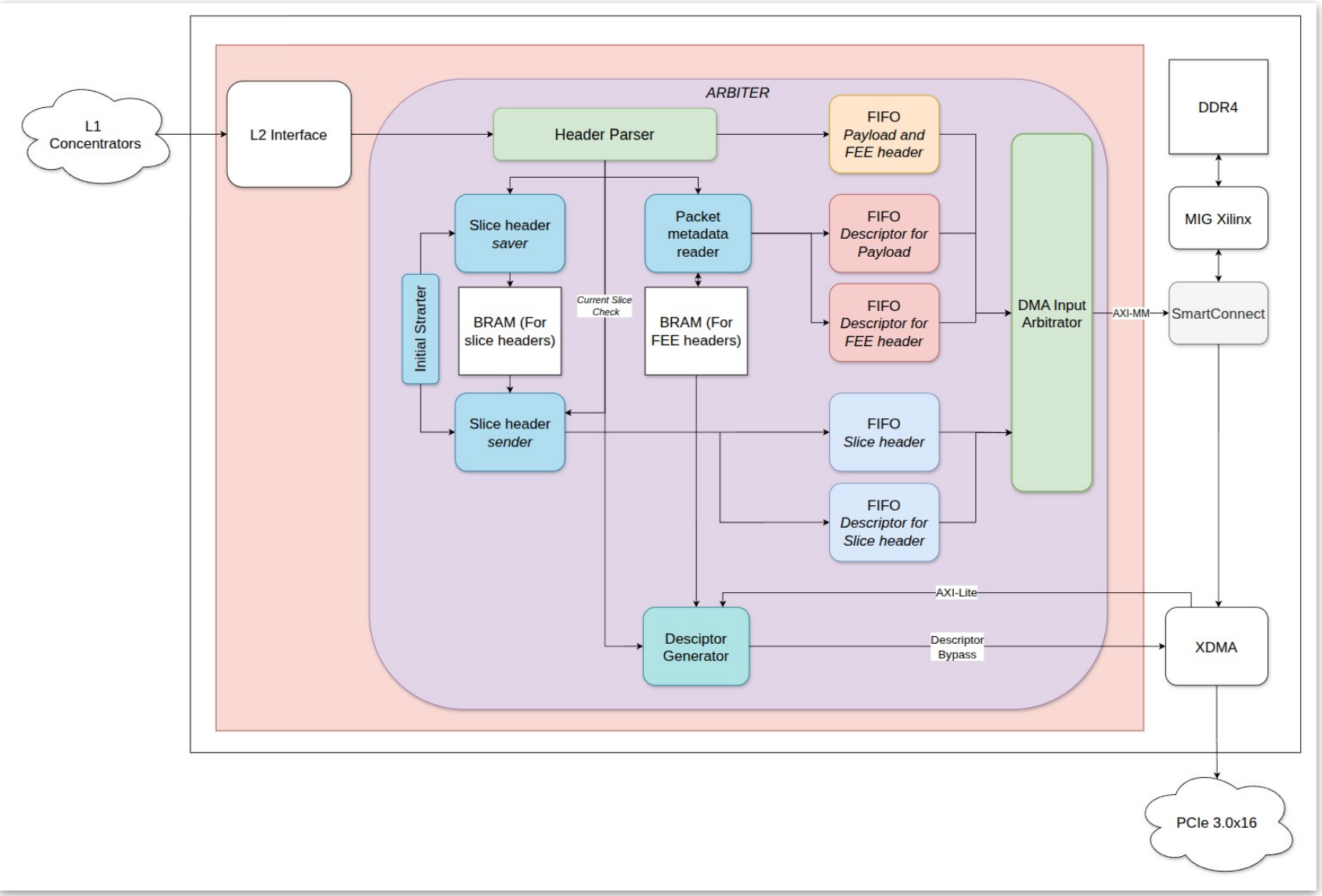


Fig. 4 Arbitrator architecture

Arbitrator:

1. It parses package headers.
2. It stores and sends metadata from headers to descriptor generator.
3. It sorts packages to DDR4 also using this metadata

Results and Plans

- The sorting design is nearly complete. Its prototype was tested in Dubna this September.
- Now, we need to finalize the design, perform bandwidth tests, and complete the verification process.
- Finish the transition to the architecture and to the new hardware platform.
- Begin working on the “Control and monitoring” modules.

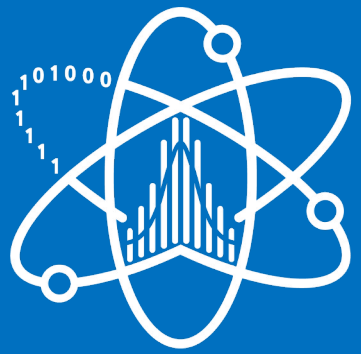
Thank you!

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