

DAQ hardware status report

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SPD CM October 2026

SPD DAQ Struct

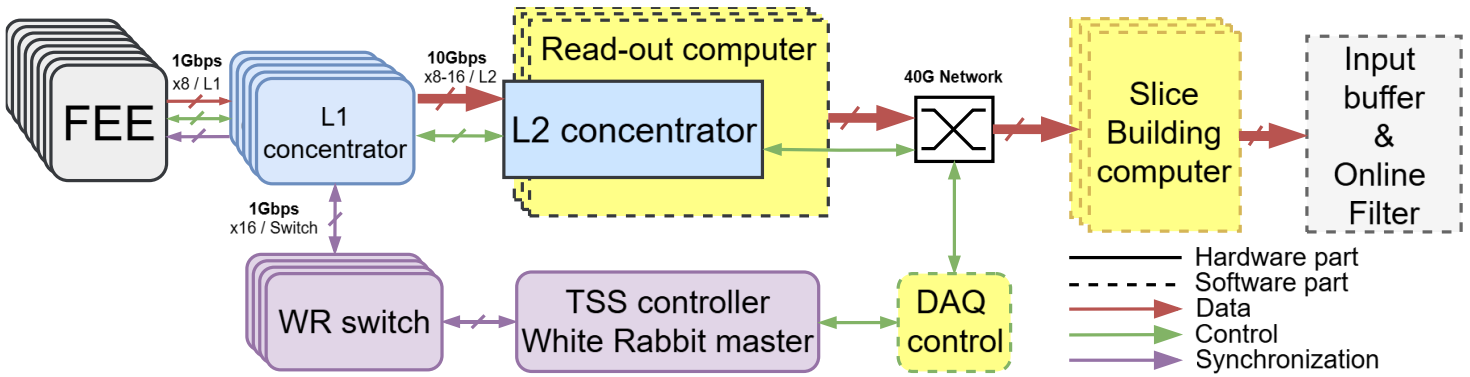
Elements of DAQ:

- Read-out chain
  - L1 – Level 1 concentrator
  - L2 – Level 2 concentrator
  - Read-out computer
- **Time Synchronization System**
- **Slice building system**

SPD Stage	FEE Outputs	L1 (8 ports)	L2 (16 ports)	Read-out PC	Slice Builders
First	~1292	>165	>12	>6-12	>5
Second	~5800	>730	>50	>25-50	>40

Bandwidth per one link:

- FEE-L1: **1.25 Gbps**
- L1-L2: **10 Gbps**
- Read-out computer – Slice building system: **40 Gbps**



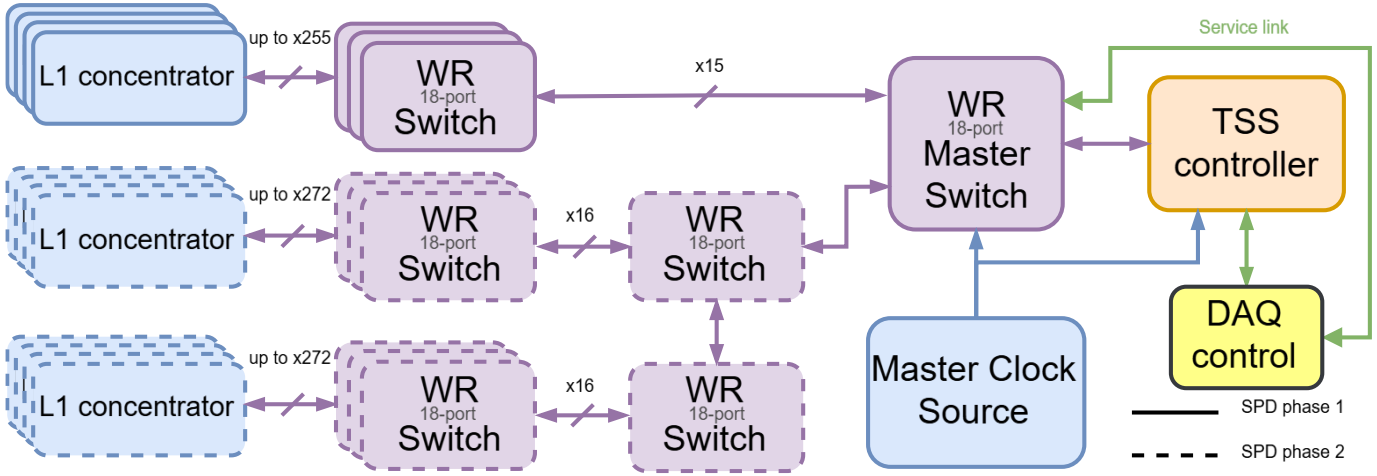
Synchronization

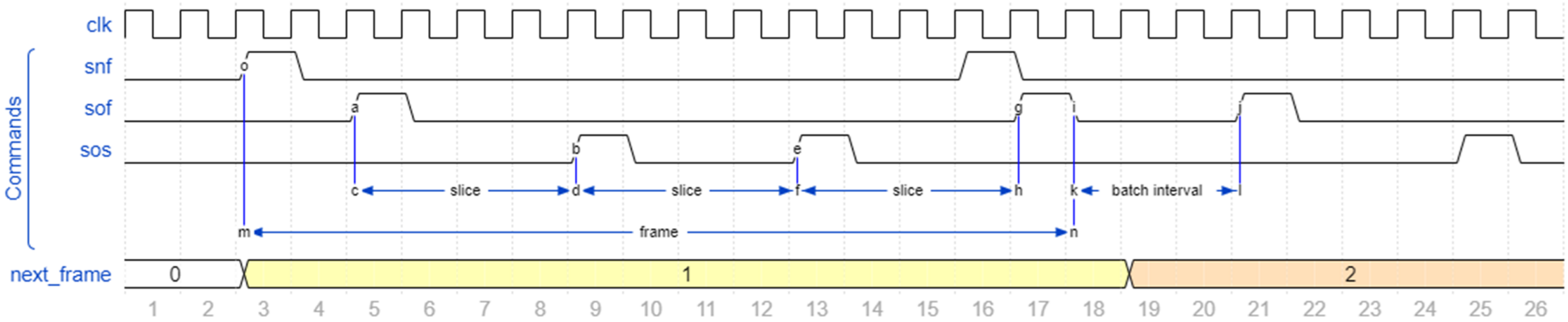
Time synchronization system tasks:

- Generation and distribution of a 125 MHz clock frequency with an accuracy of better than 1 ns and a jitter of better than 50 ps
- Generation and distribution of synchronous commands to the detector

Components:

- TSS controller
- Ultra-stable clock source
- 18-port White Rabbit-enabled switches
- White Rabbit nodes integrated into L1 hubs





IP core for FEE control

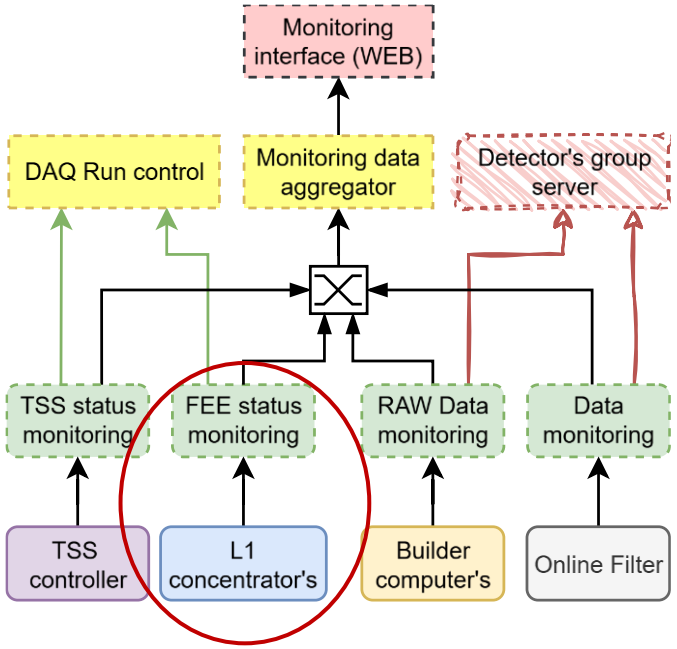
A mechanism has been implemented to provide access to the registers of all devices connected to the DAQ system. It is universal and compatible with all FPGA-based devices

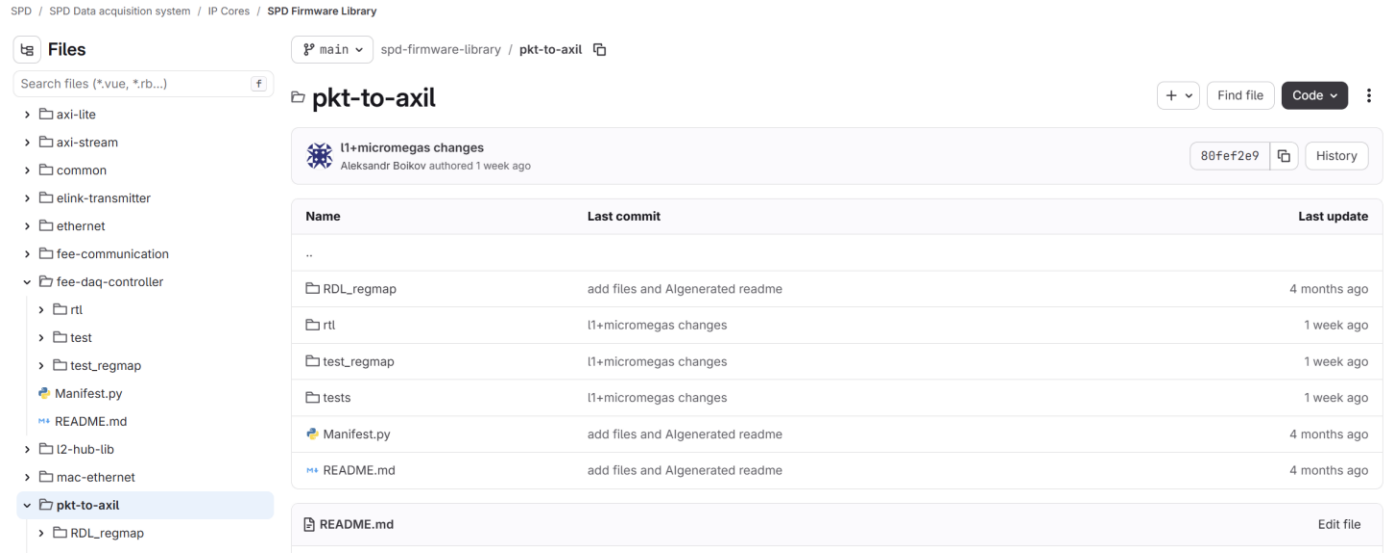
Each request generates a response indicating the operation status

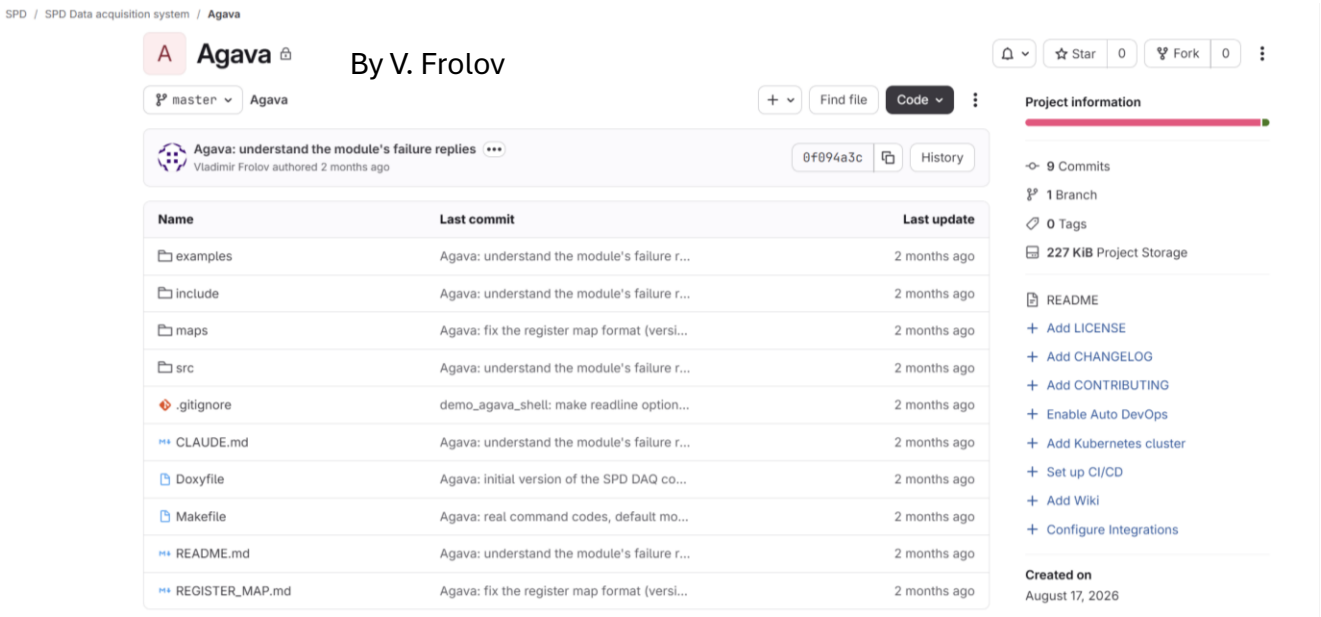
One request = 10 bytes (address, value, flags)

Supports up to approximately 140 register read/write requests in a single UDP packet

Includes timeout and error handlers







Tested on the following FPGA platforms: Altera, Xilinx, and PangoMicro.

IP core for remote access

Main module: FEE_DAQ_controller

Up to 15 channels for register control *(creation of instances of the **FEE_control_over_packet** module)*

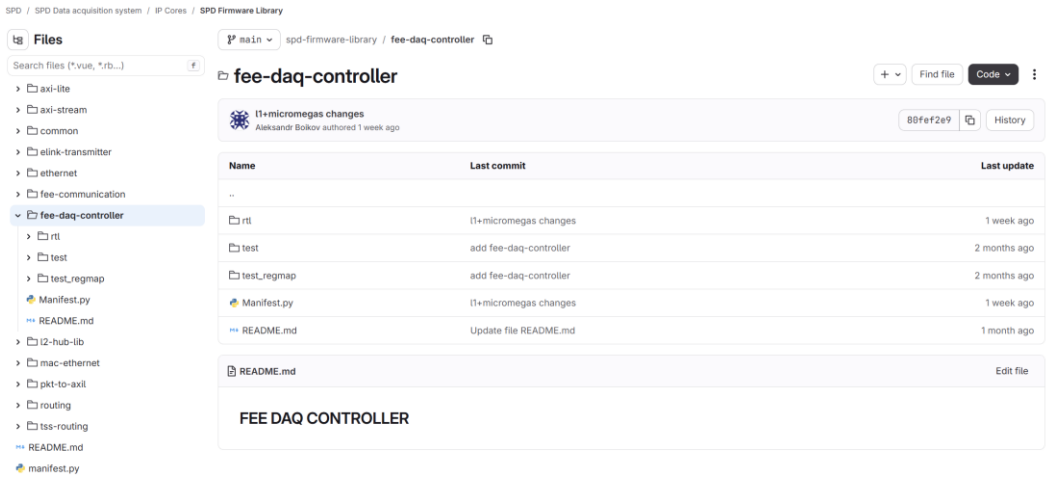
A dedicated access channel for FPGA firmware reconfiguration

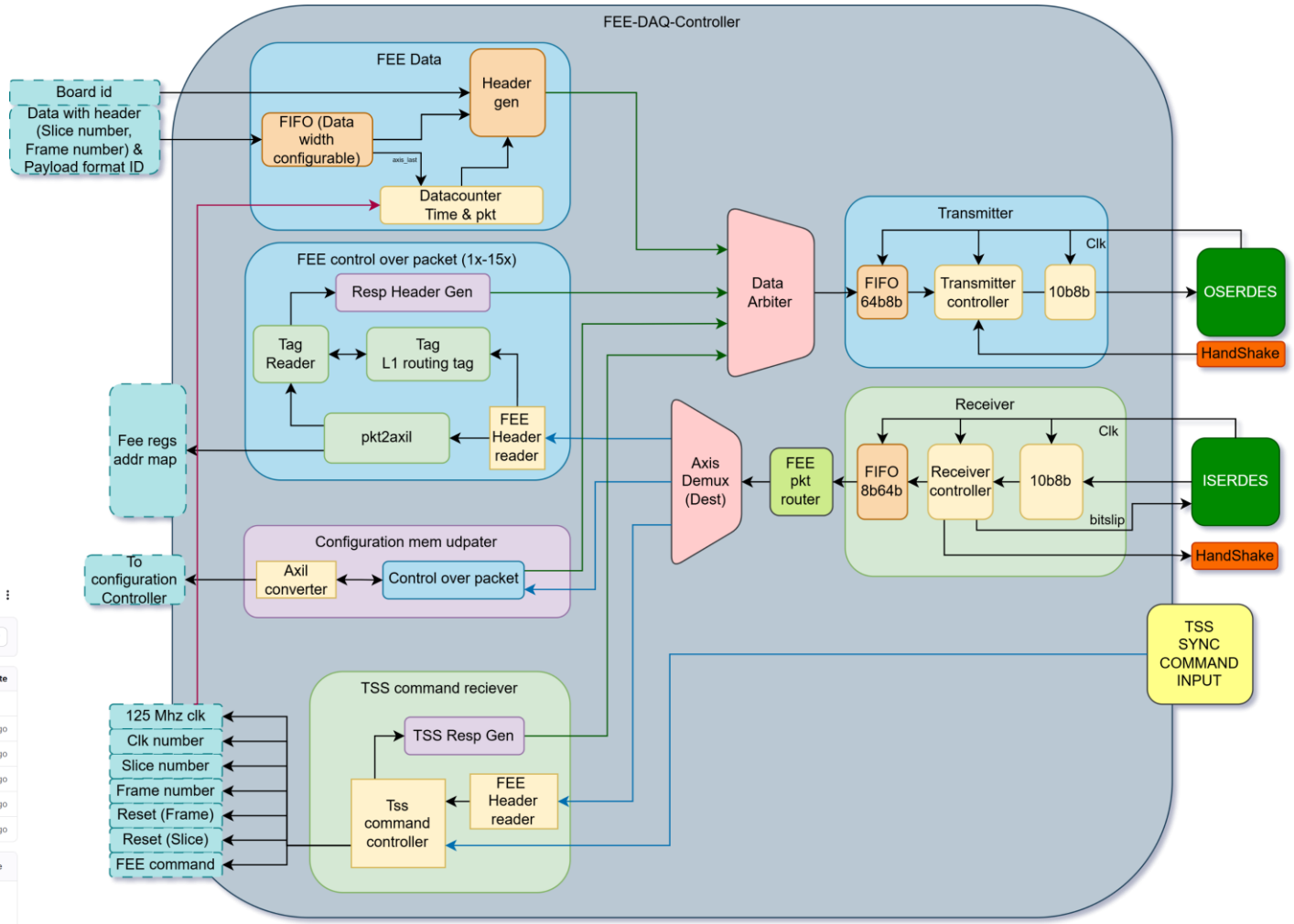
A module for decoding commands received from the synchronization system

A packet-generation module that formats data as required for transmission to L1

Available on git.jinr.ru

The README will be updated soon...





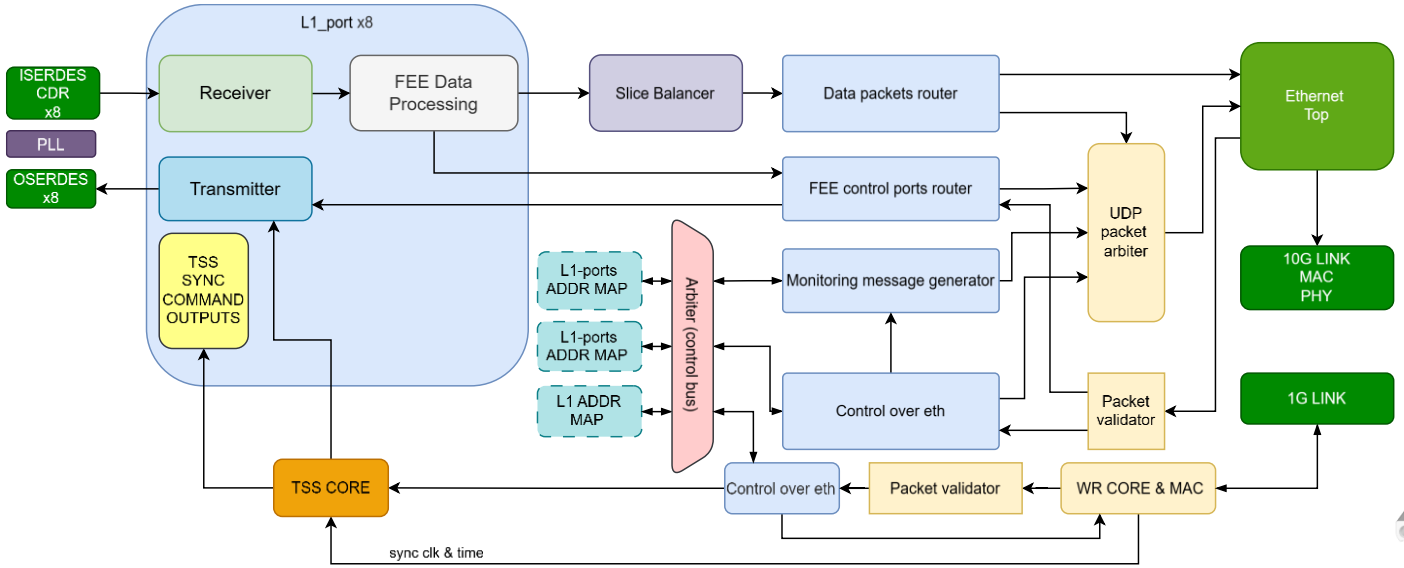
L1 concentrator (hub)

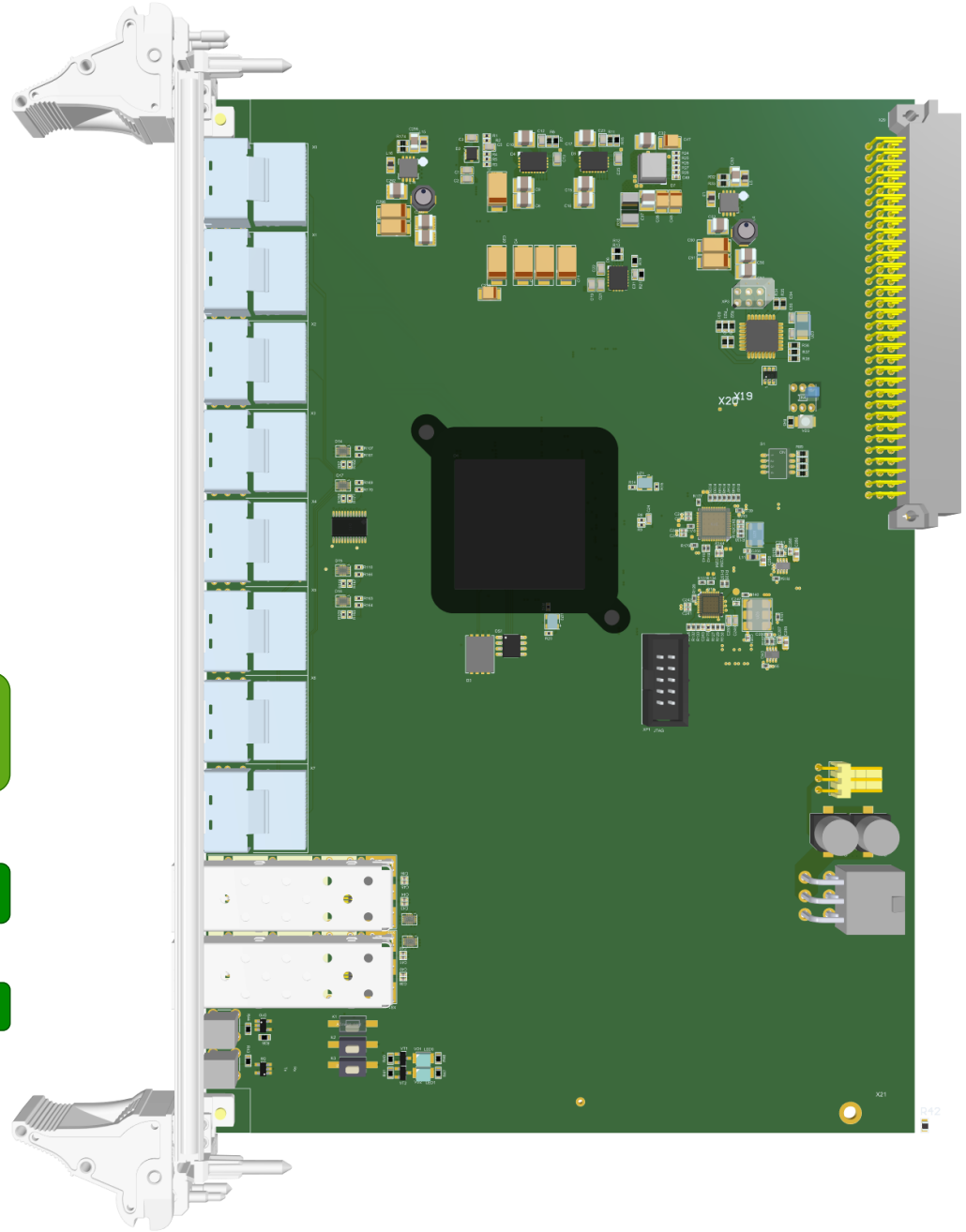
The firmware (excluding the White Rabbit core and TSS module) is ready and has been tested as extensively as possible on the current prototype

The implementation of the prototype for the RS system is still being refined. We plan to send the PCB design for manufacturing by the end of next week. All further testing will be carried out using this prototype

At this stage, we can work with the electronics prototypes for STRAW and Micromegas. We currently have 2 boards for Micromegas and 3+ boards for STRAW

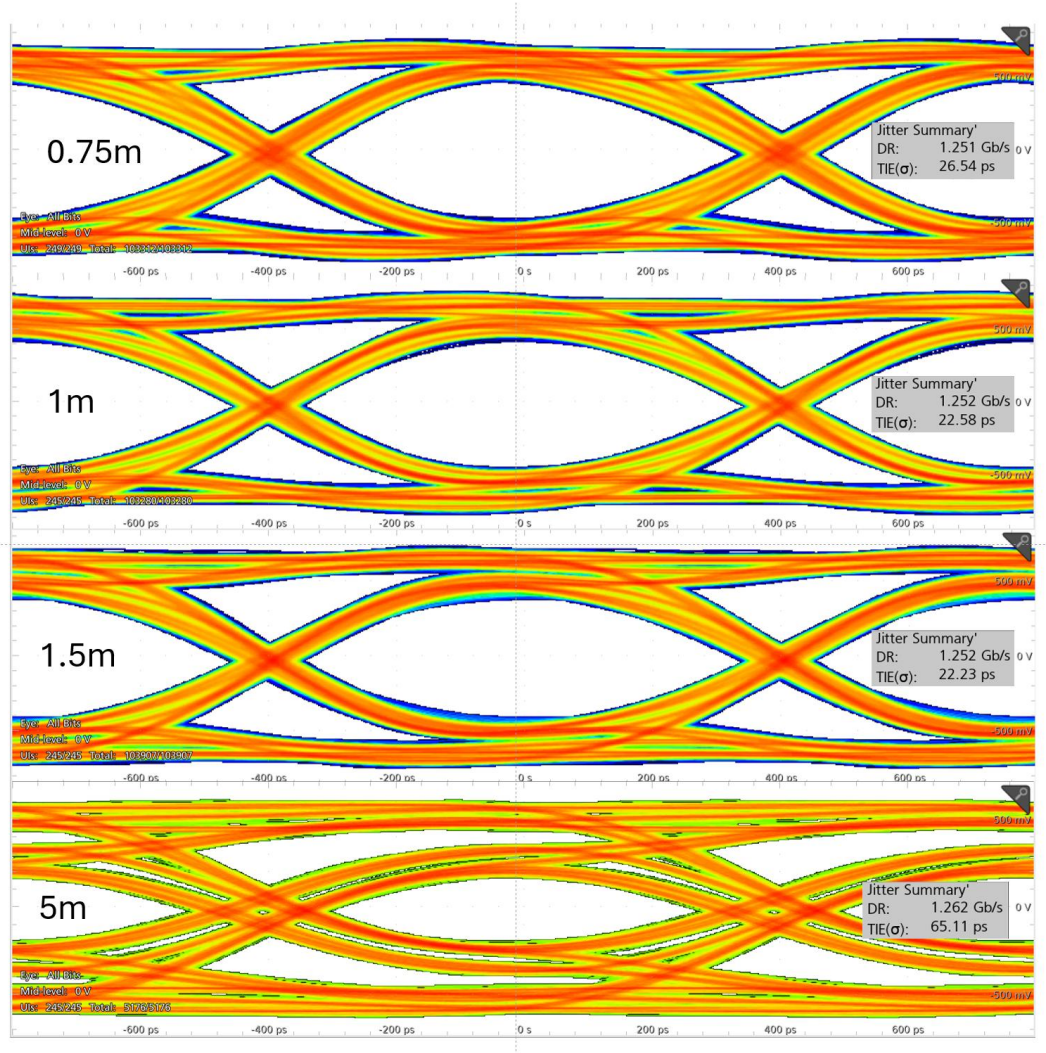
The prototype will be used to test FEE control and readout, as well as the operation of the synchronization system

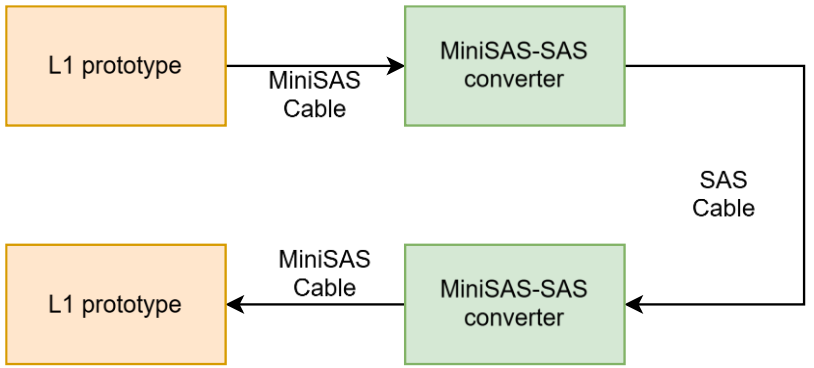


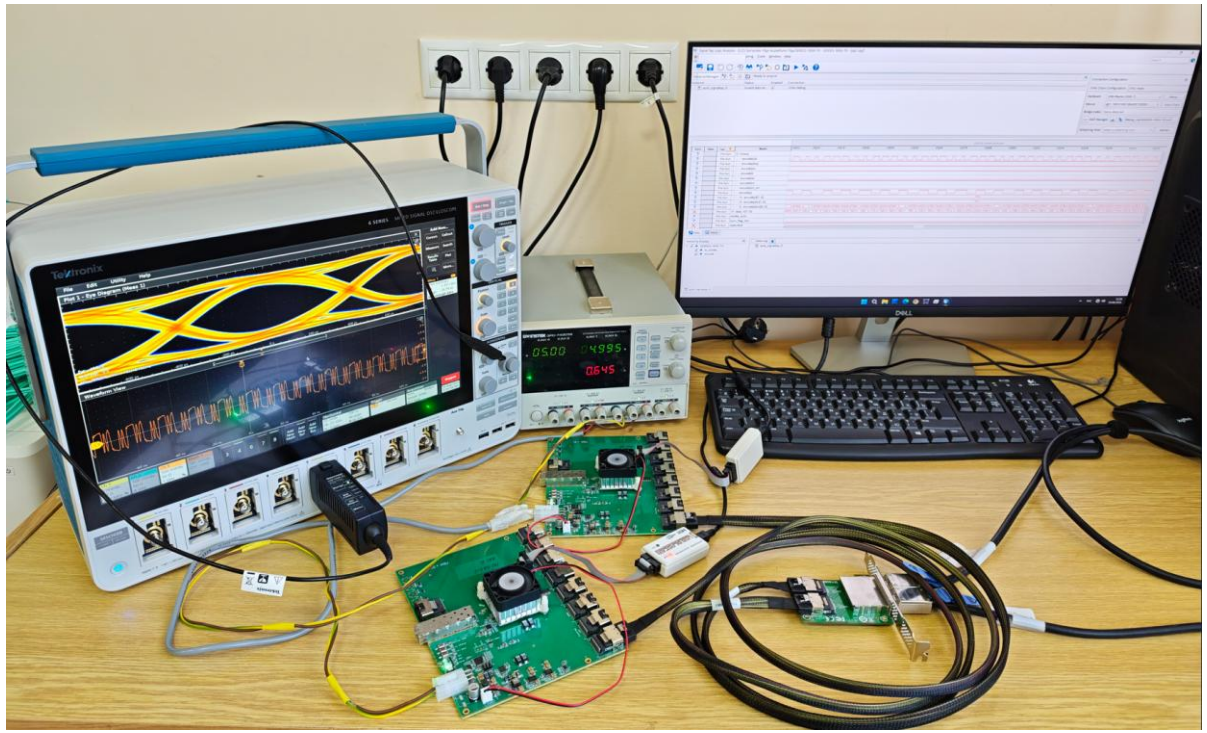


MiniSAS cable test’s

The tests have shown that a realistic connection via MiniSAS over a 5-meter cable will work. For further testing, we need to have the corresponding cables manufactured at the factory.







L2 concentrator (hub)

A prototype of the hub for the new platform has been assembled

All hardware functions are operational

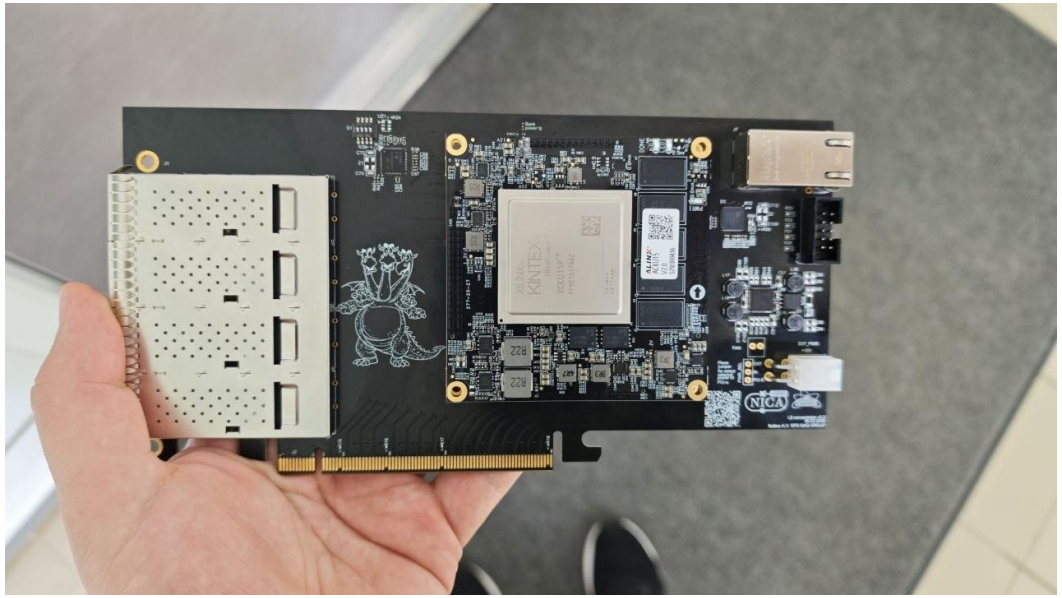
Project migration, including firmware migration, is required (is currently being handled by the Tomsk team)

Another iteration is planned (components was be founded)

For the 1 Stage, 12–14 hubs will be required, depending on the number of FEE units

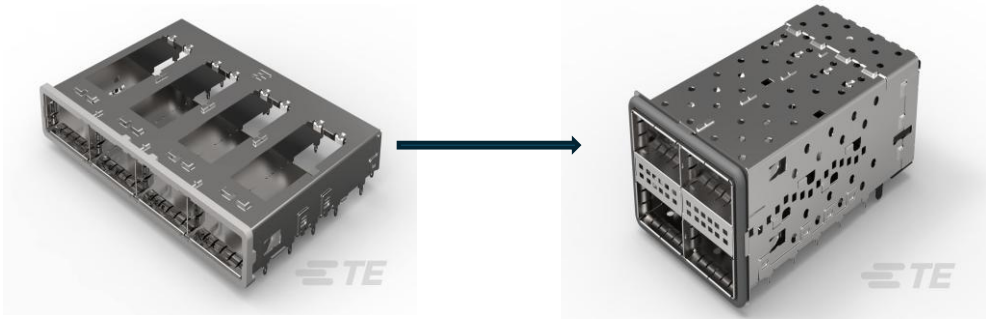
- ACKU15 FPGA SoM with AMD Kintex Ultrascale+™ XCKU15P
- 10 GByte (80-bit) DDR4 SDRAM
- 2 x 64MB QSPI Flash
- 1 x PCIe® Gen3 ×16
- 12V single supply
- Dimension: 80 x 80mm form factor
- Gigabit transceivers
  - 32 x GTH, up to 16.3 Gbps
  - 24 x GTY, up to 28.21 Gbps





Next Step

Change type of QSFP cage



Will use an SFP module instead of standard RG-45. And place on the front panel



White Rabbit Switch manufacturing

16–18 units required for the 1 Stage.

Commercial unit cost: over $10,000.

Estimated cost of components and assembly: $3,000–4,000 (preliminary estimate).

Last hardware update: 2014. Firmware and software were last updated in 2025.

Only minimal design modifications are needed to proceed with manufacturing. One chip for current iteration.

More components for future cost optimization.

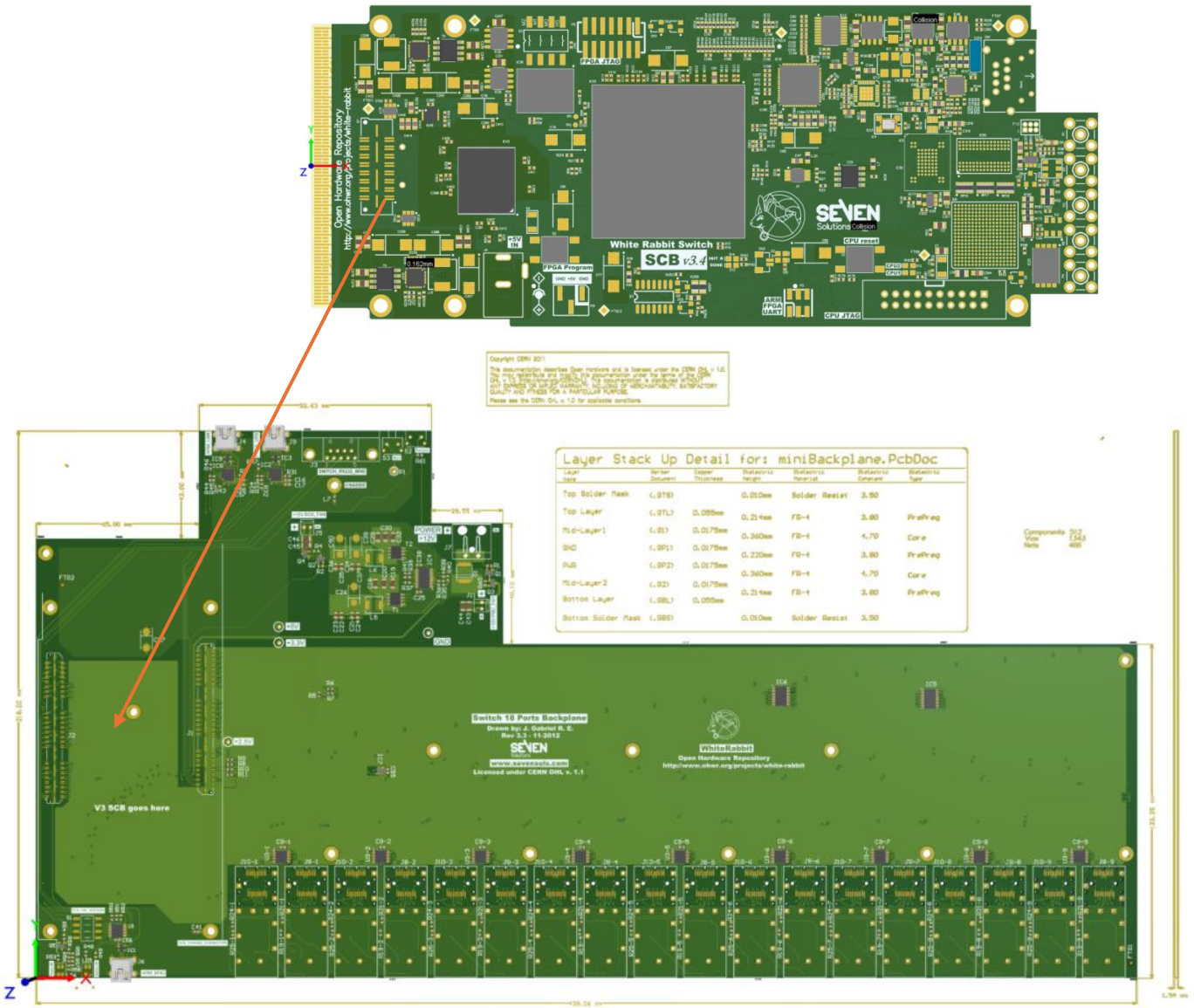
master wr-switch-hw / circuit_board / **wrs_v3**

wrs_v3

Find file | Code

scb: add pdf file of schematics for v3.4
Benoit Rat authored Sep 25, 2014 — 7c3334c8 | History

Name	Last commit	Last update
..		
Docs_PDF	scb: add pdf file of schematics for v3.4	12 years ago
LIBS	Updated PCB and schematics. Changes are in th...	14 years ago
SCB_SAM9G45	scb: add partlist file 3.4.1 for SCB v3.4	12 years ago
mini_backplane_18SFP	misc: clean up mini-backplane folders	12 years ago
mini_backplane_simple	PCB: production docs for V3 simple mini-backpla...	15 years ago
mini_backplane_test	misc: clean up mini-backplane folders	12 years ago
LICENSE.txt	wrs3: improve license and README	12 years ago
README.md	wrs3: improve license and README	12 years ago



White rabbit testbench

Oscilloscope: Tektronix MSO68B 6-BW-6000 (50 Gb/s, 2 channels)

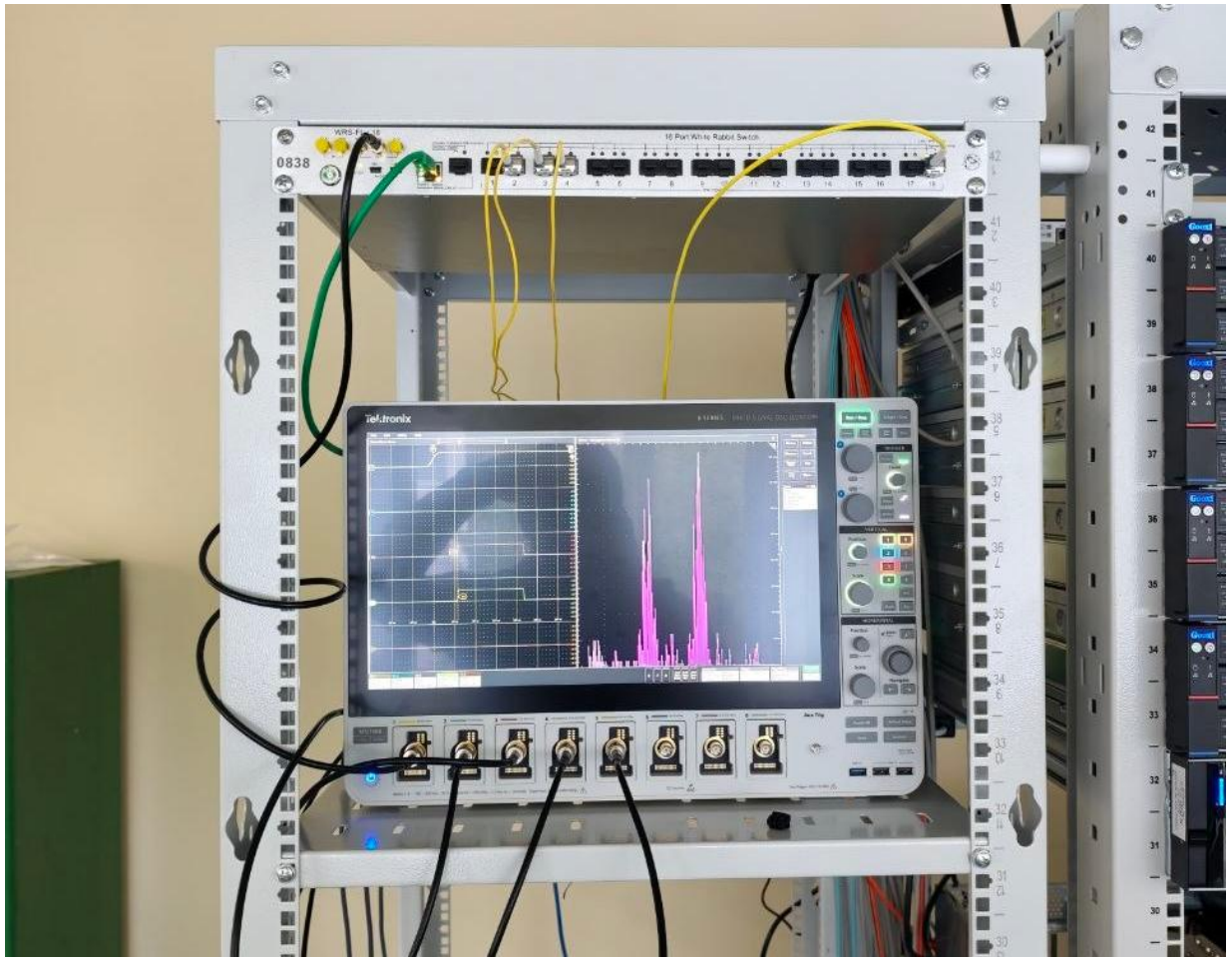
Network switch: White Rabbit (SyncTech)

Nodes: White Rabbit (SyncTech)

Server, cabling, etc.

Ready for future L1 test’s





FEE emulator

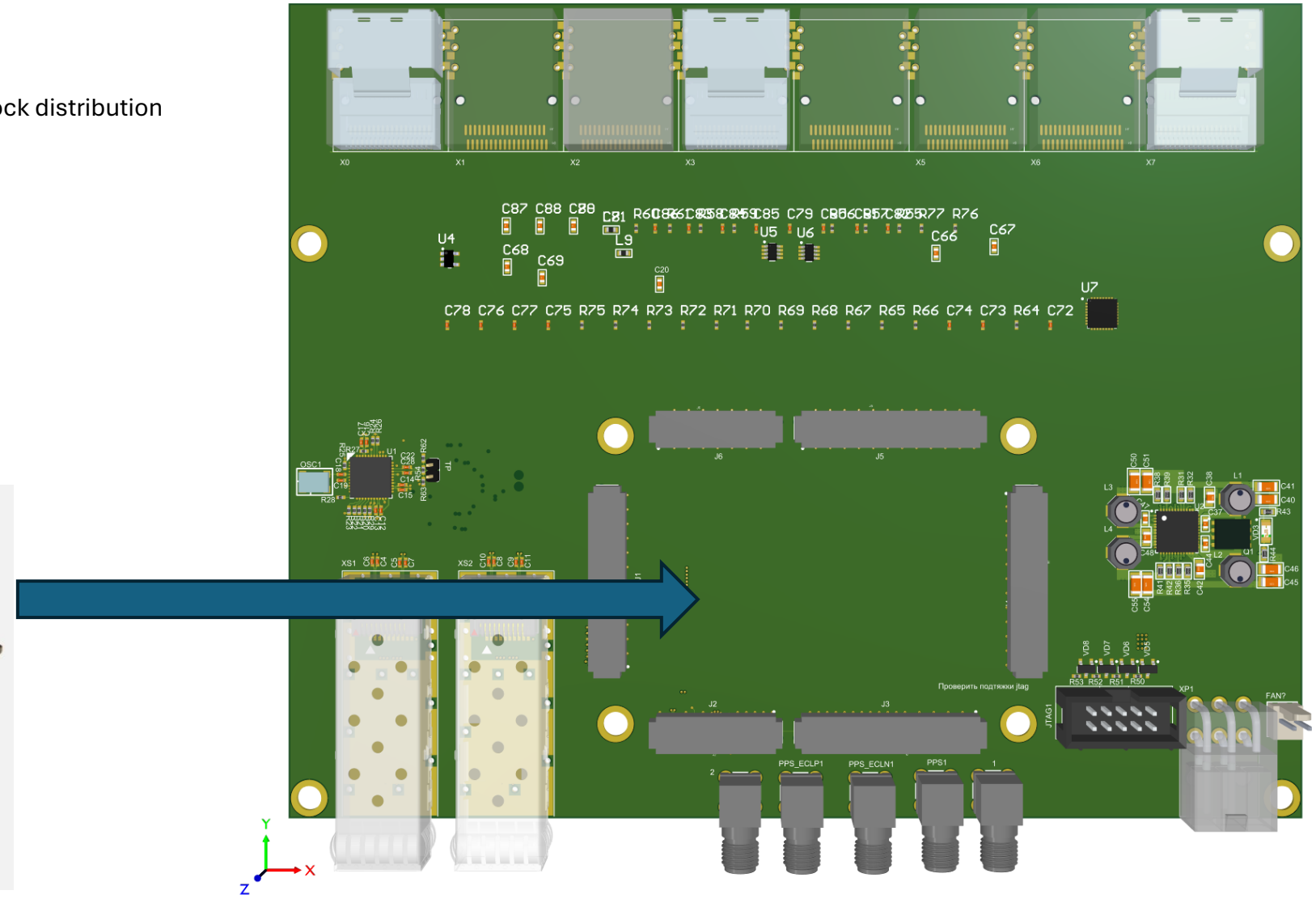
Custom PCB for Kintex SoM:

- 8 MiniSAS for test E-Link
- SFP+ for 10G link (Software data generator)
- SFP+ for 1G link for White Rabbit test’s
- Test points for diff line (TSS part) for verification clock distribution from L1
- SMA connectors

Test cases:

- PC-> ETH -> MiniSAS data sender
- TSS command reader
- Register configuration procedure L1-FEE
- Test Firmware update procedure
- …



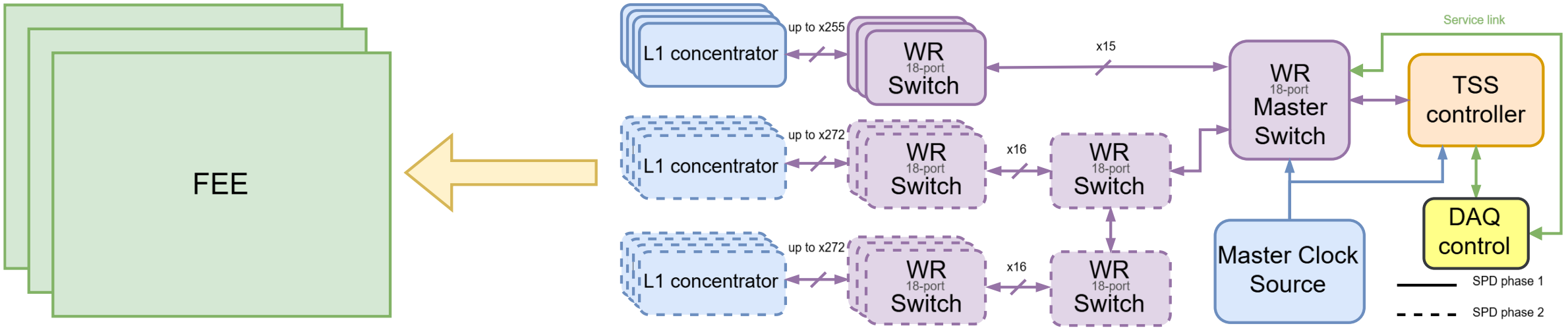


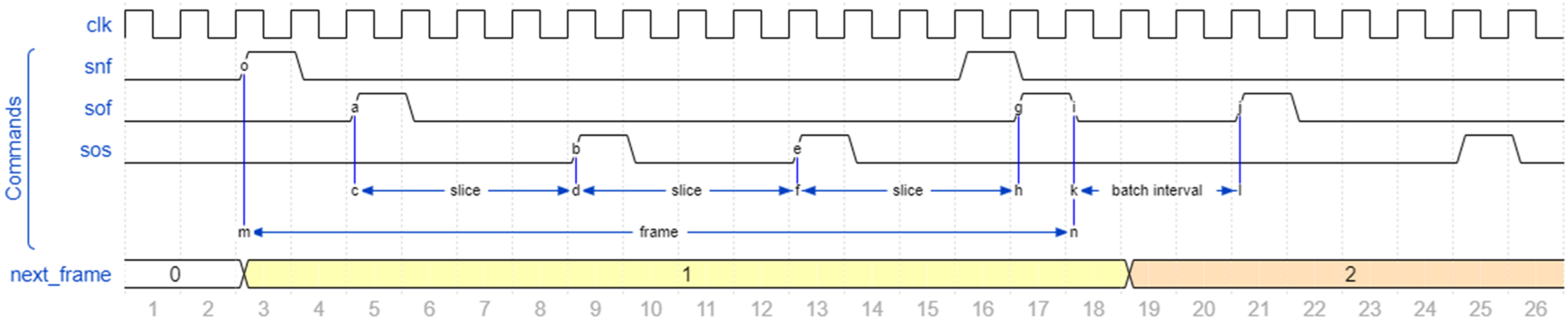


Thanks for your attention

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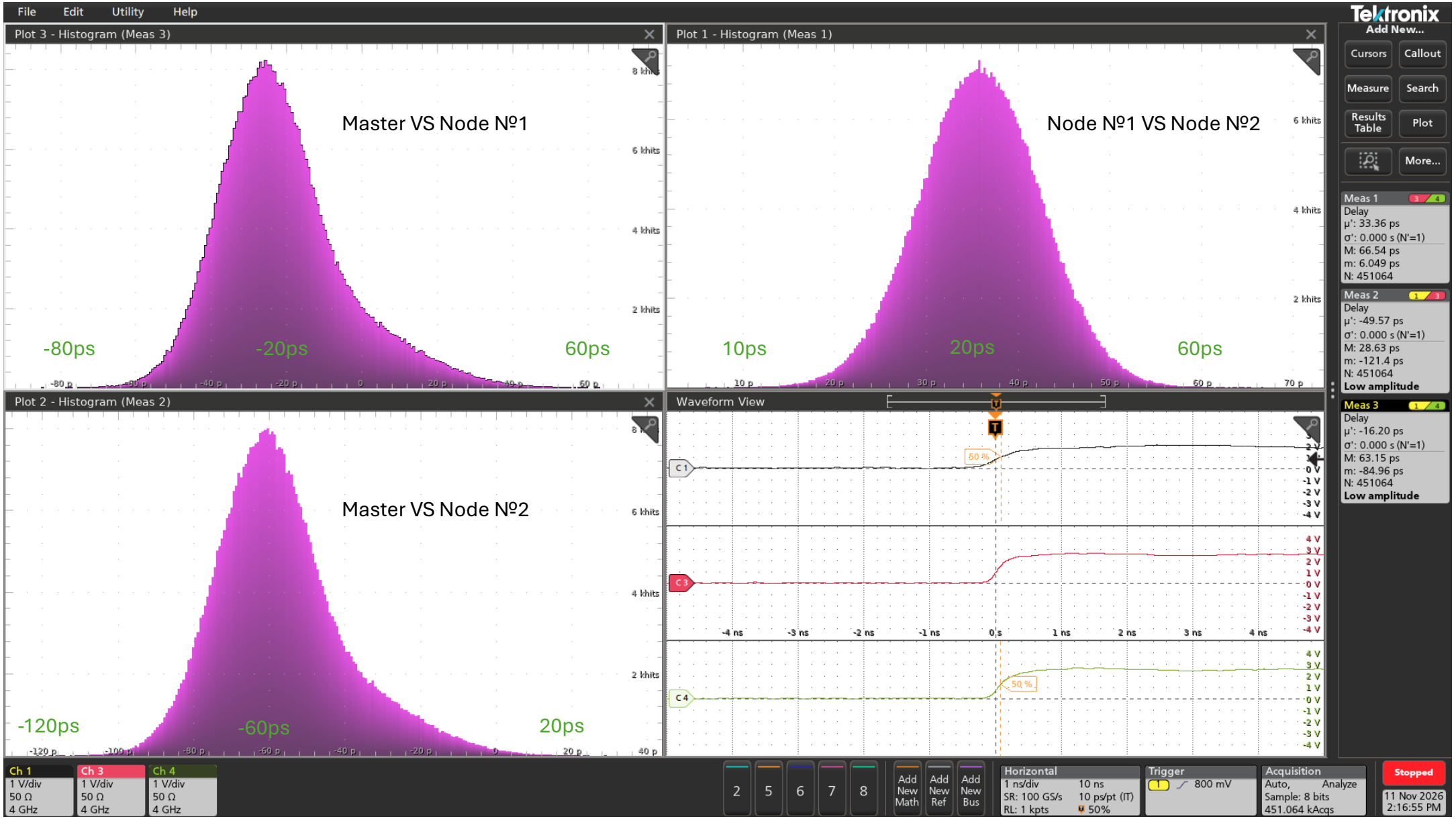
Remarks before next session (1)





Remarks before next session (2)

4-week test. Stable temperature conditions. MLIT 421 room



Remarks before next session (3)

4-week test. Unstable temperature conditions. MLIT 421 room

