Status of TOF development



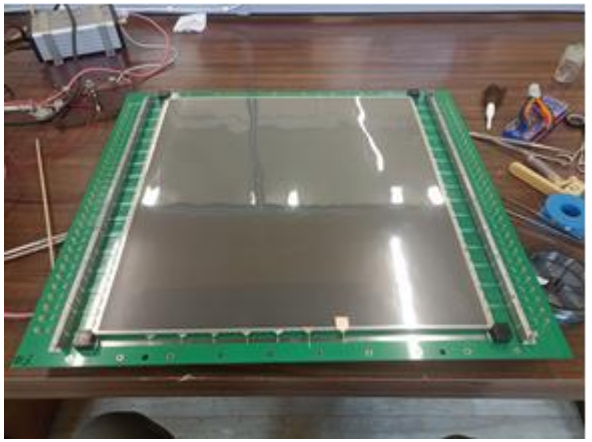
Valery Chmill

SPD NICA

Progress Report on MRPC Activities at FIAN (LPI)

Федеральное государственное бюджетное учреждение науки
Физический институт имени П.Н. Лебедева Российской академии наук

- 4 время-пролетные камеры с униполярным съемом сигнала (2 - закаленное стекло, 2 - незакаленное) были сделаны и переданы в Протвино группе Е.А. Ладыгина;
- В настоящий момент идет набор данных (см. фото.). По первым предварительным результатам есть отличия в характеристиках камер в зависимости от типа стекла.
- После получения и обработки необходимого объема данных будет сделан подробный доклад об изготовлении камер и полученных результатах тестов.
- Работы по изготовлению камер с дифференциальным съемом сигнала движутся. Материнские платы получены, сейчас находятся в процессе установки пассивных компонентов, начато нанесение высоко-резистивного покрытия на стекла.
- Оценка срока готовности камер — ноябрь-декабрь текущего года.





Status of DATA analysis

Valery Chmill

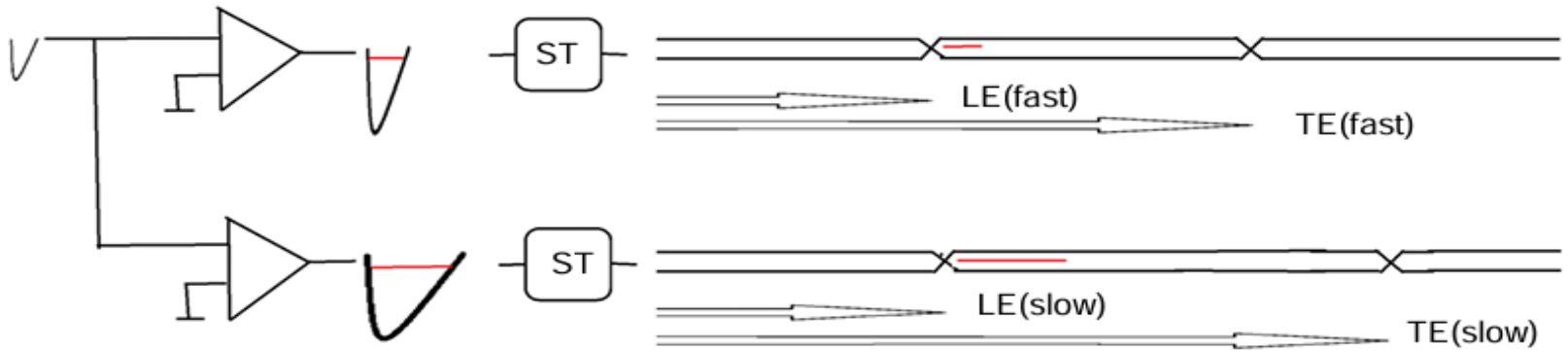


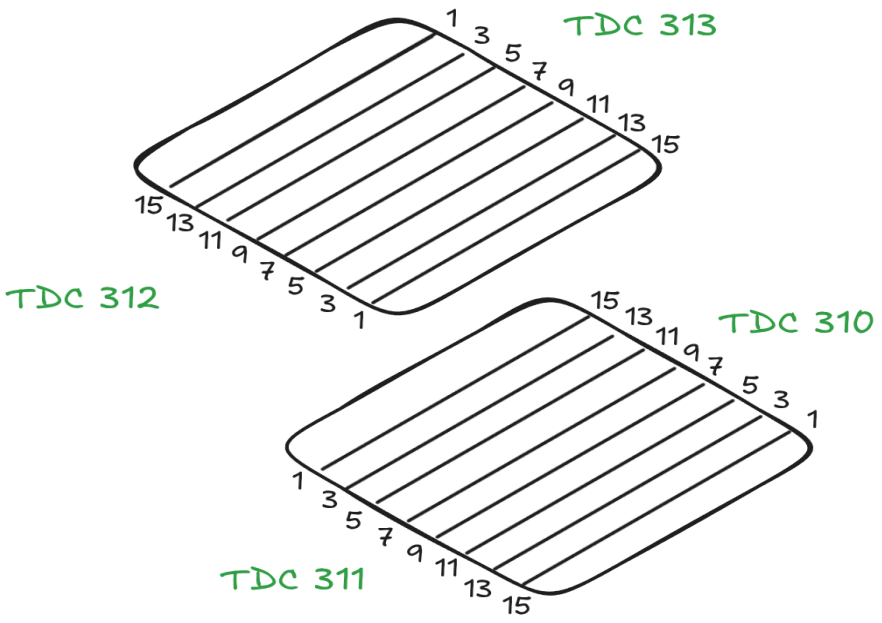
TDC-Readout-Board, Triggered/Triggerless-Readout-Board

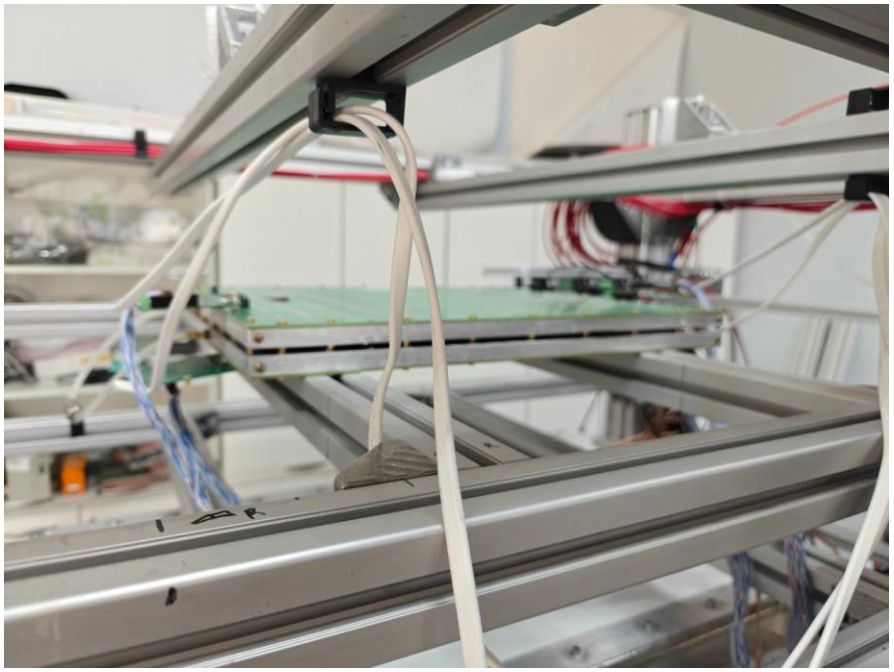
Item	Value
Supply Voltage	48 V (40-50V), galvanically isolated on board
Power Supply Current	0.5A minimum without AddOns
GbE-connectivity	max. 95 MBytes/s transfer per link
GbE-slow-control	up to 400 registers/transfer, speed depends on GbE latency
Connectivity	Max. 8 SFPs, each 2GBit/s on board. With hub-addon: max. 32 SFP
	4 AddONs on top (208 pin), 1 AddOn on bottom
Max Readout Trigger Rate	about 300 kHz (depending on configuration and network size)
Max Hit Rate	50 MHz (burst of 63 hits)
TDC Channels	260 (Single edge detection)
Time Precision	<20 ps
Minimum pulse width	<500 ps

TRBv3 FPGA-TDC Based Platforms 128ch in TDC mode

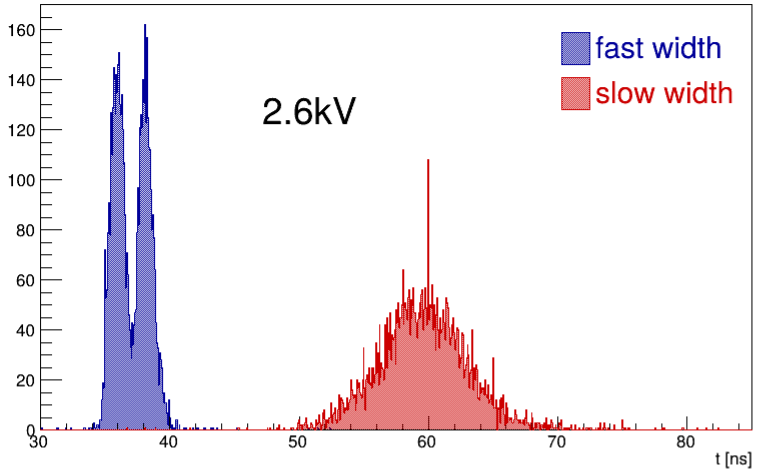
Schematic view of experimental setup

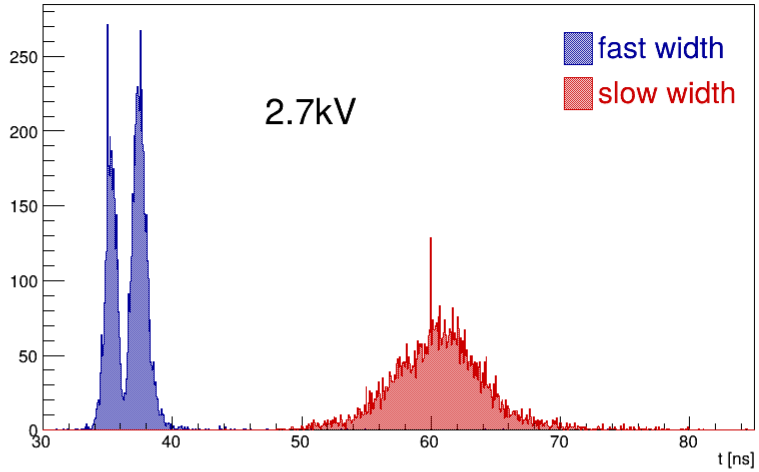


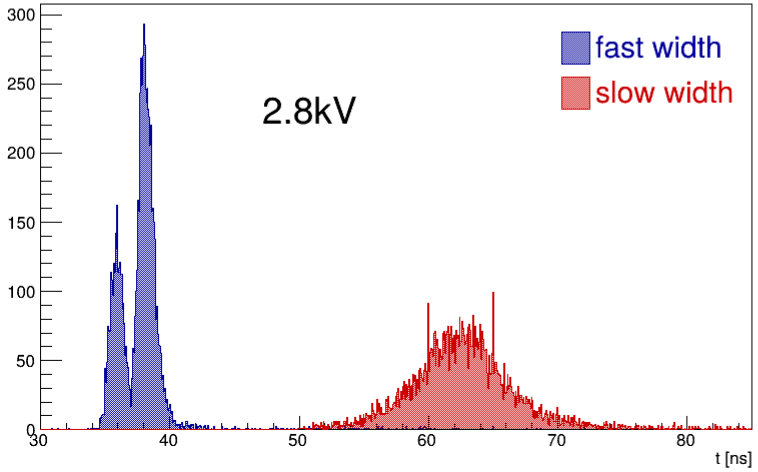


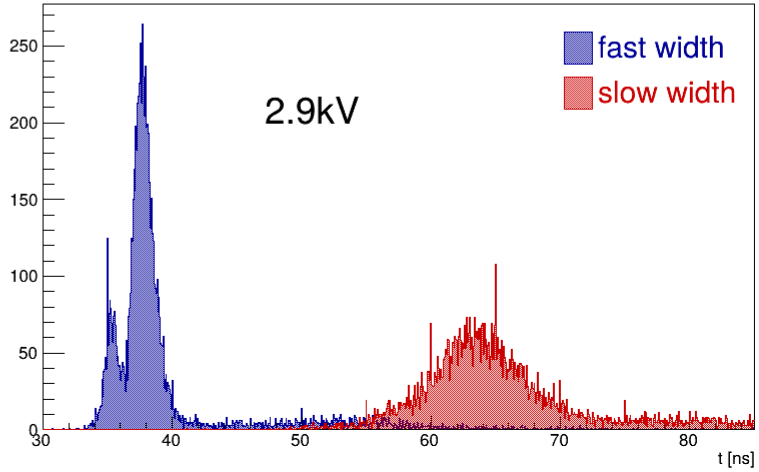


Width spectra for fast and slow channels

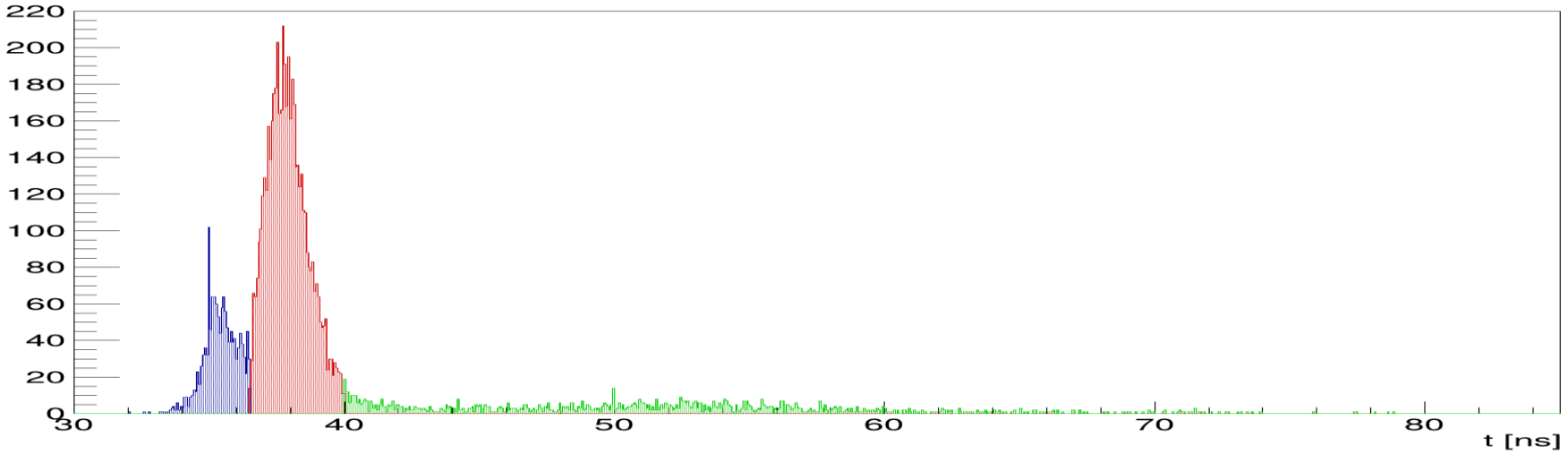


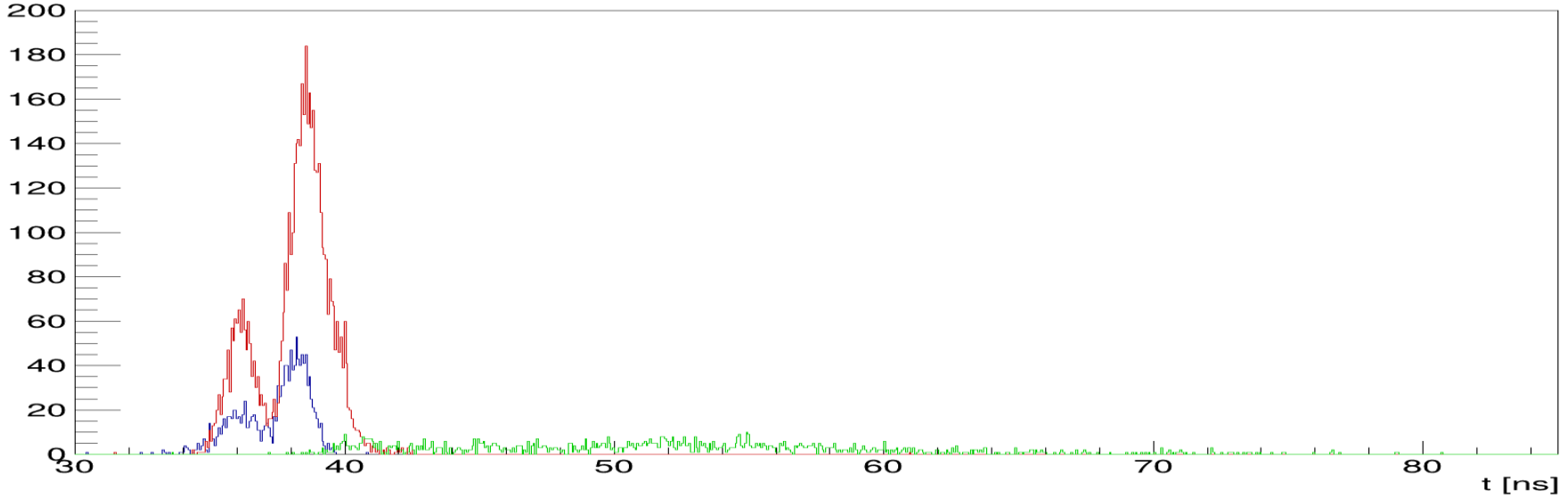




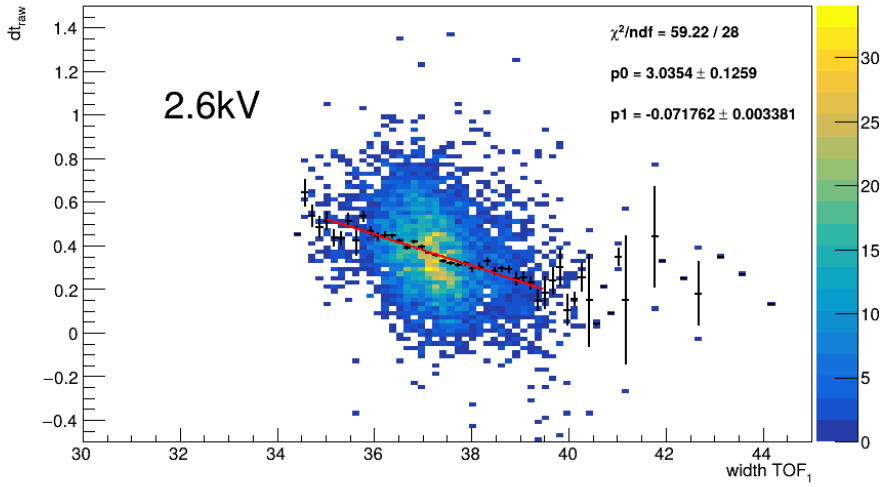


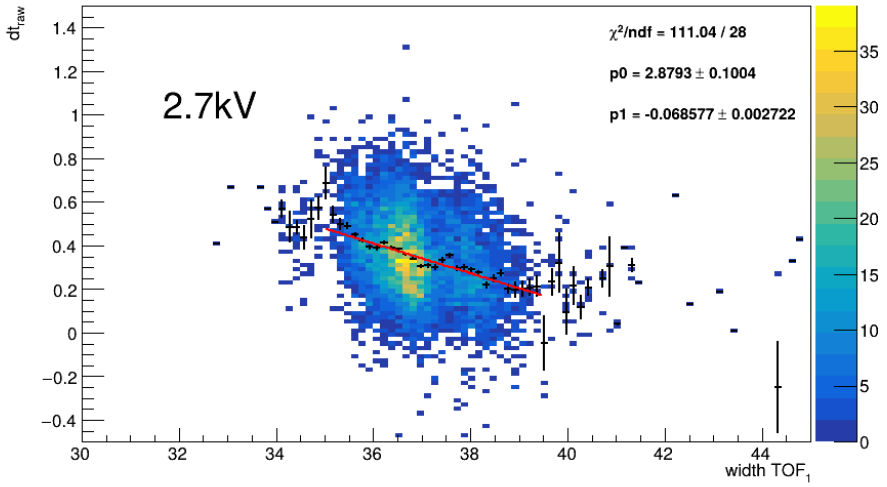
Time cuts to show who is who on fast

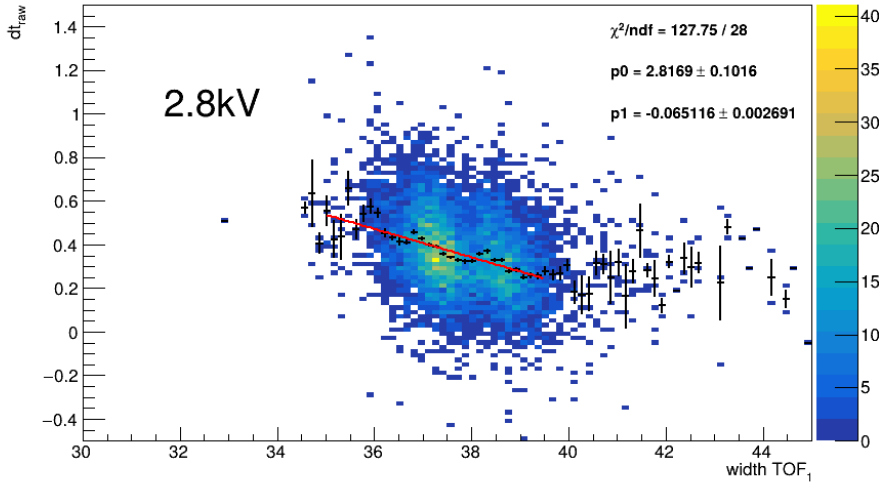


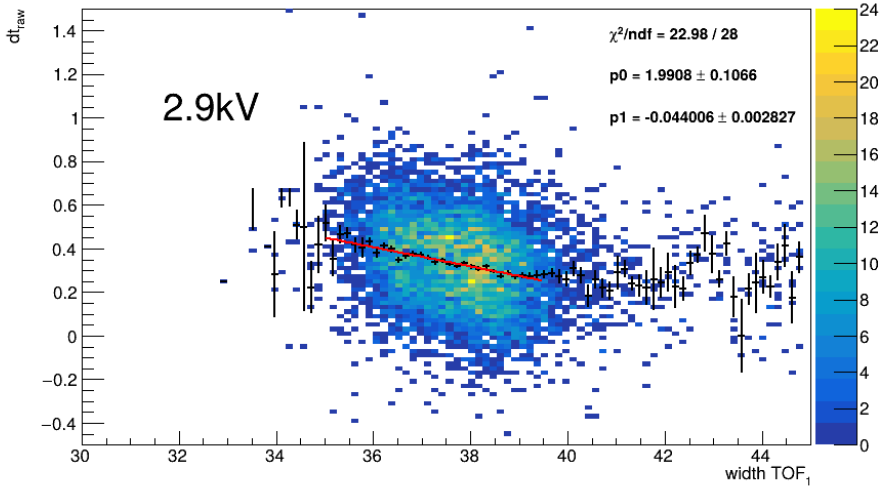


Walk through correction based on Fast signal

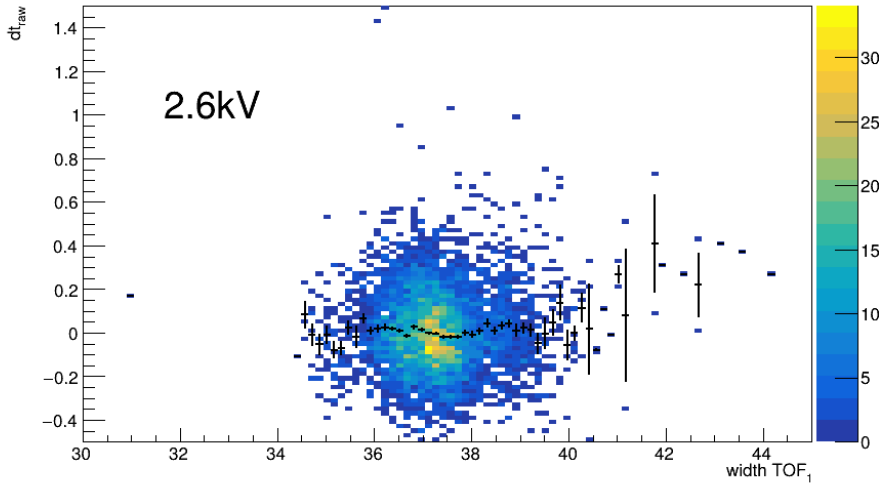


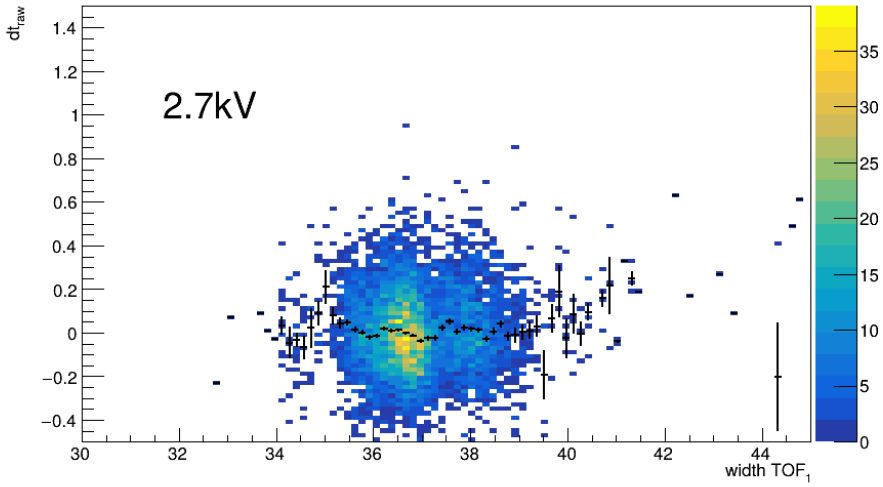


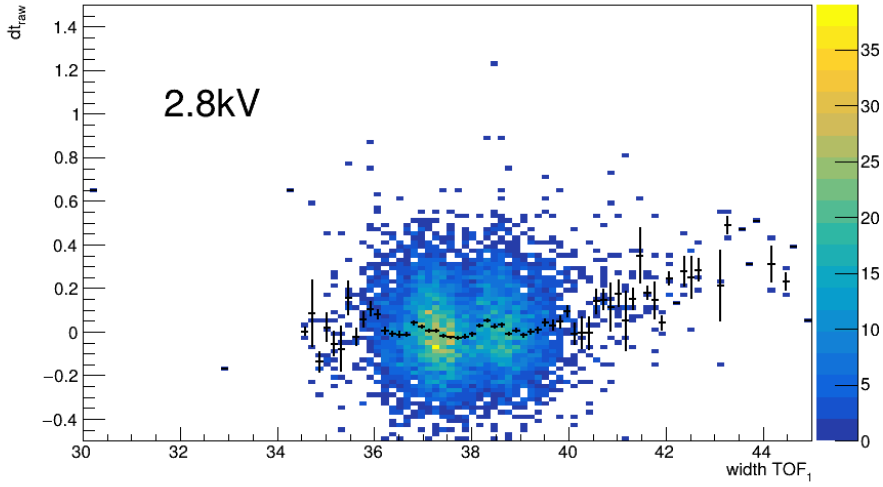


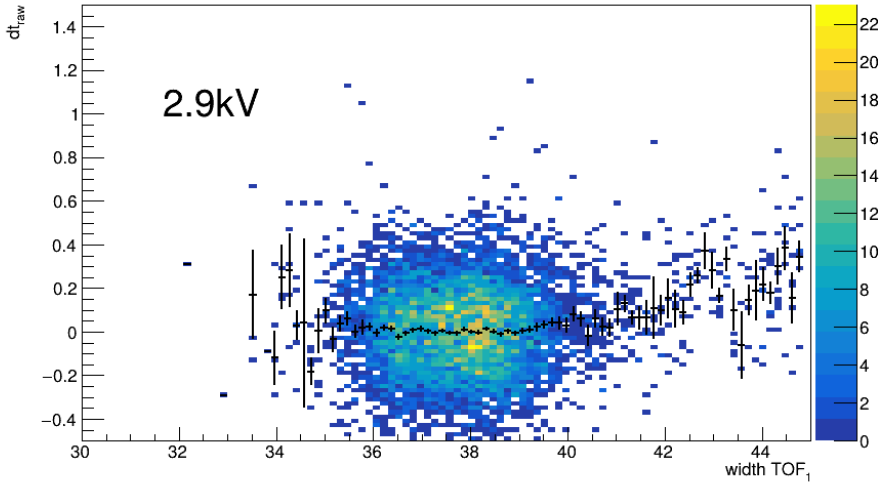


Walk through correction based on Fast signal

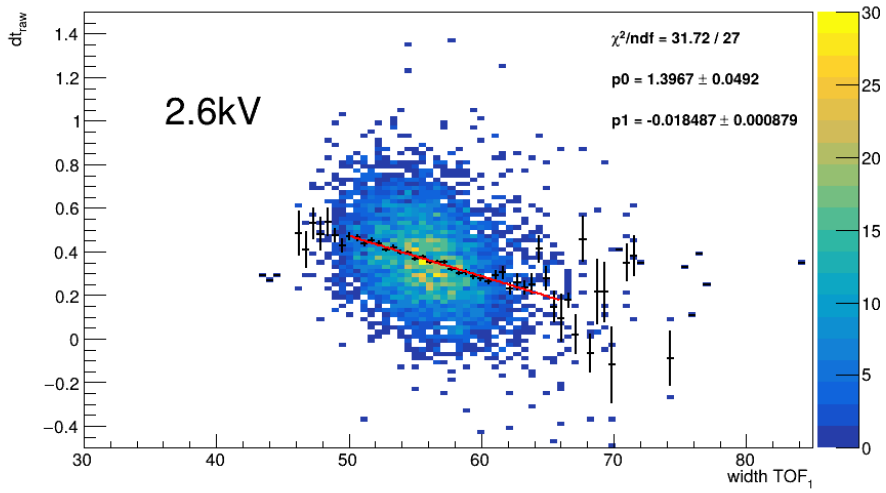


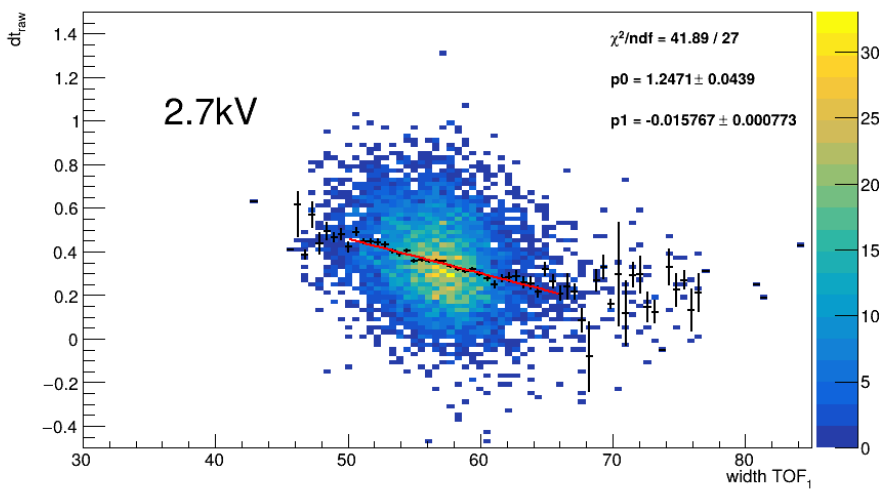


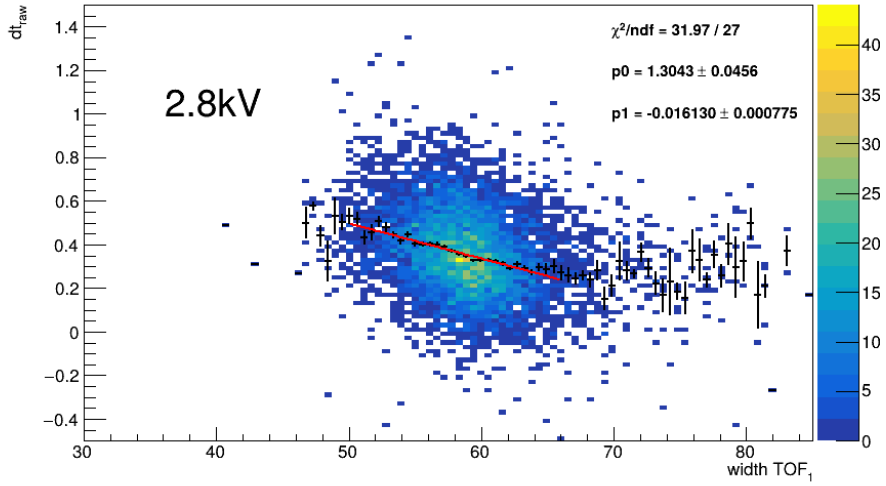


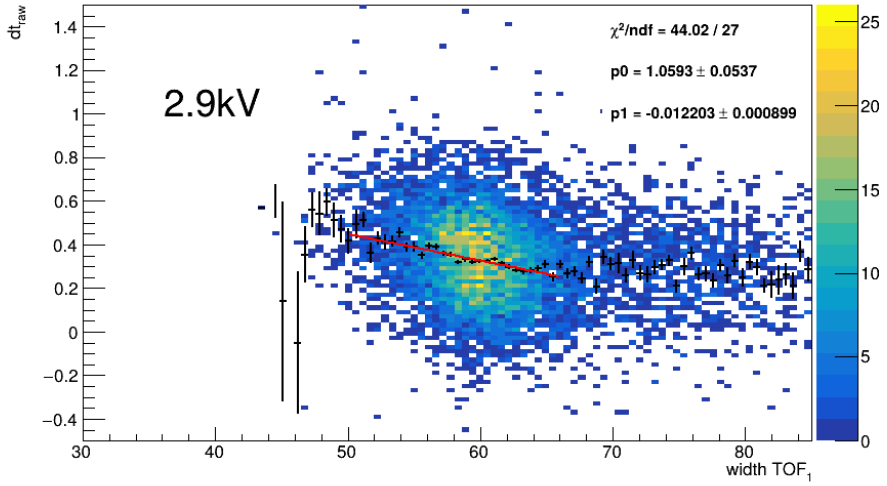


Walk through correction based on Slow signal

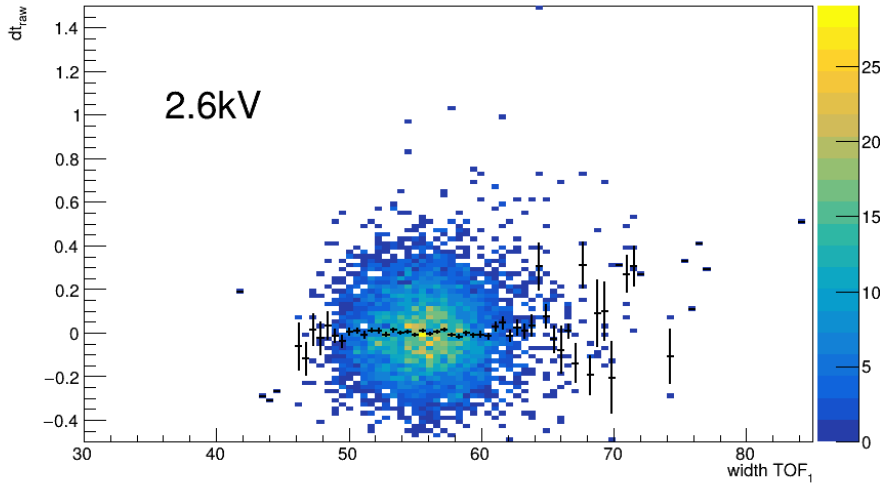


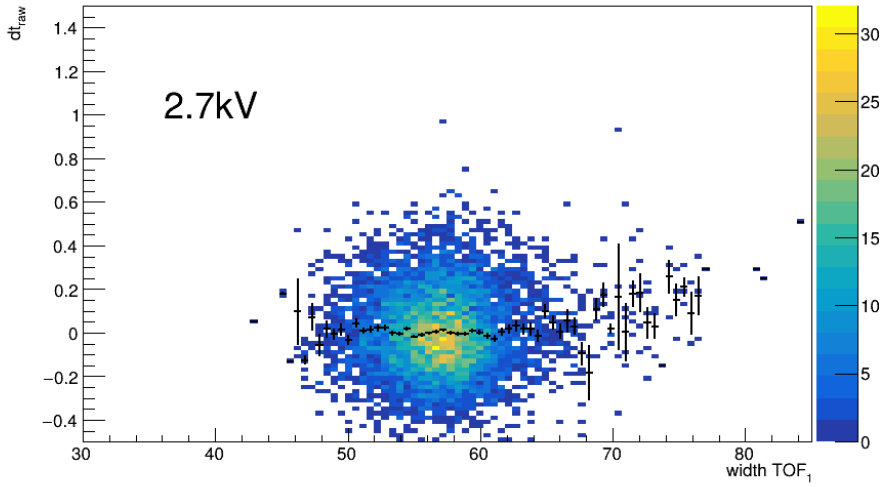


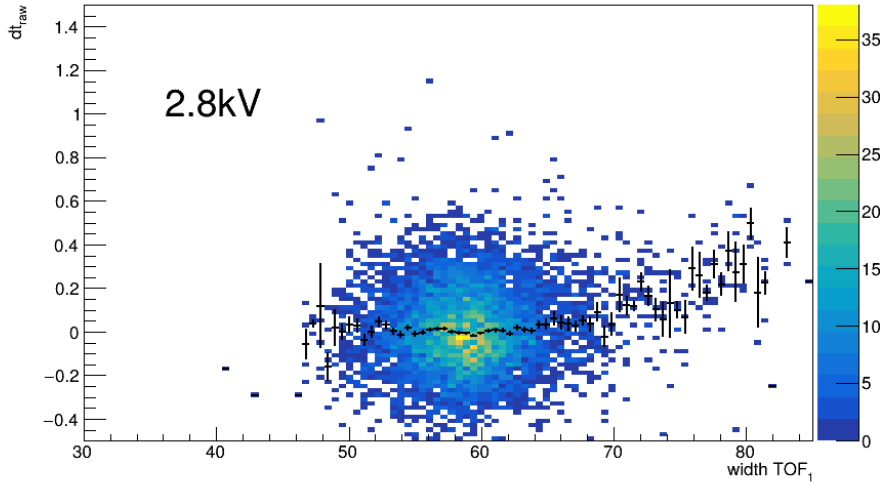


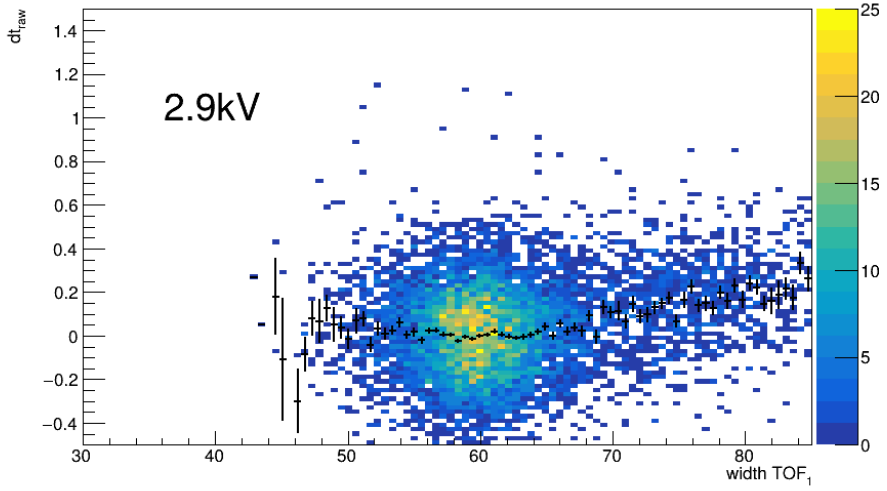


Walk through correction based on Slow signal

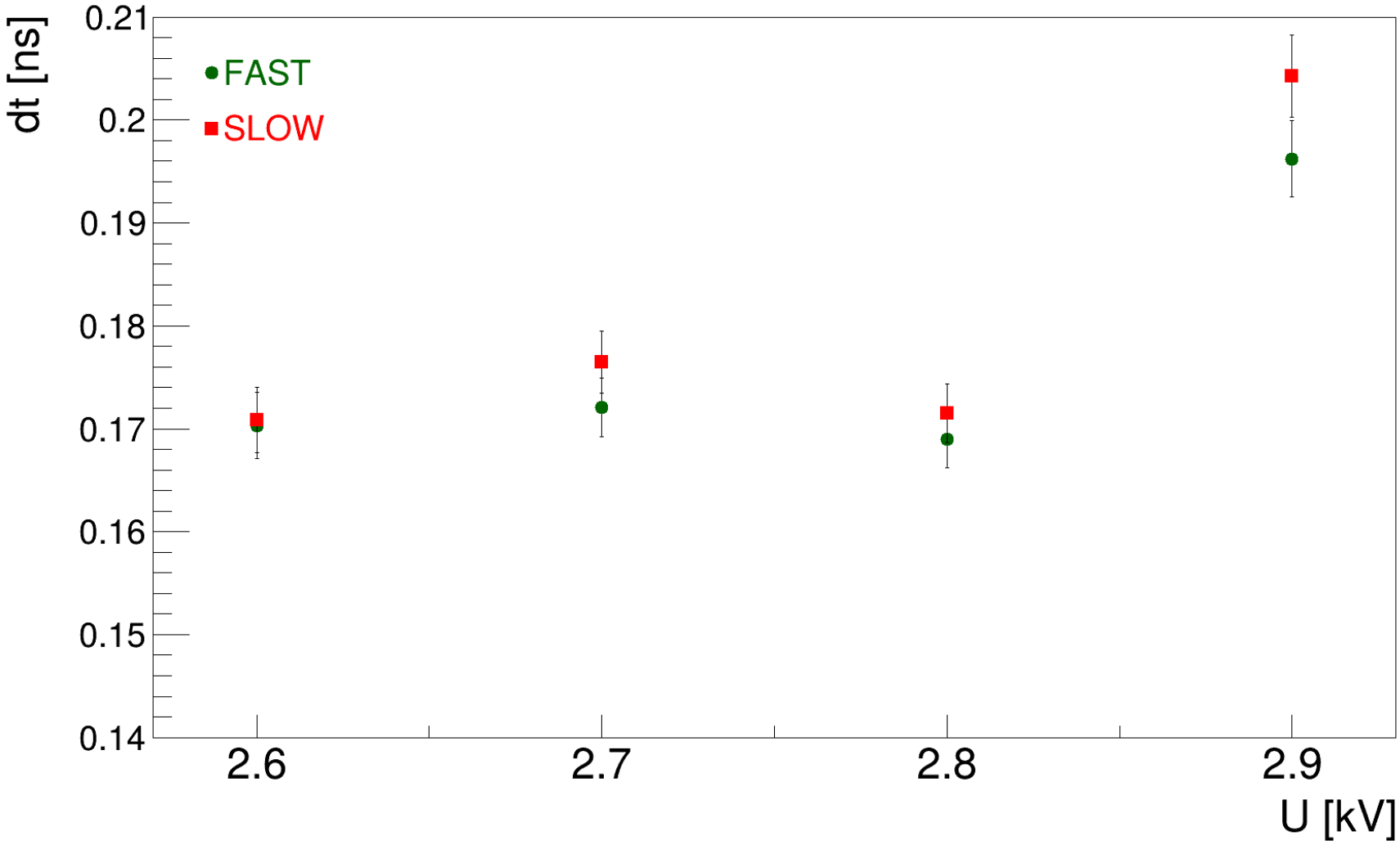






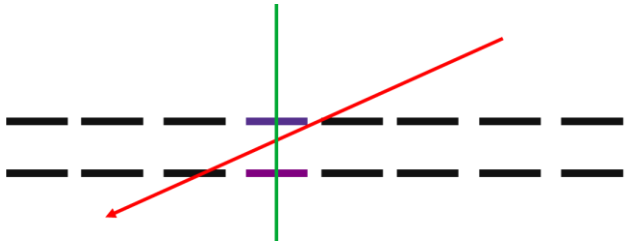


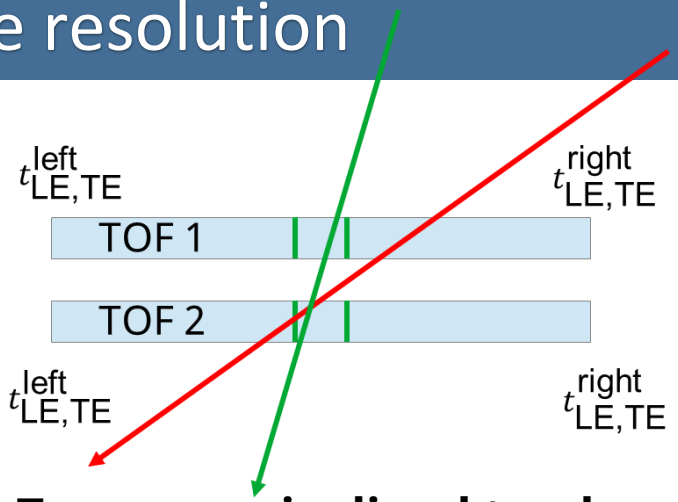
Time resolution after Walk through correction



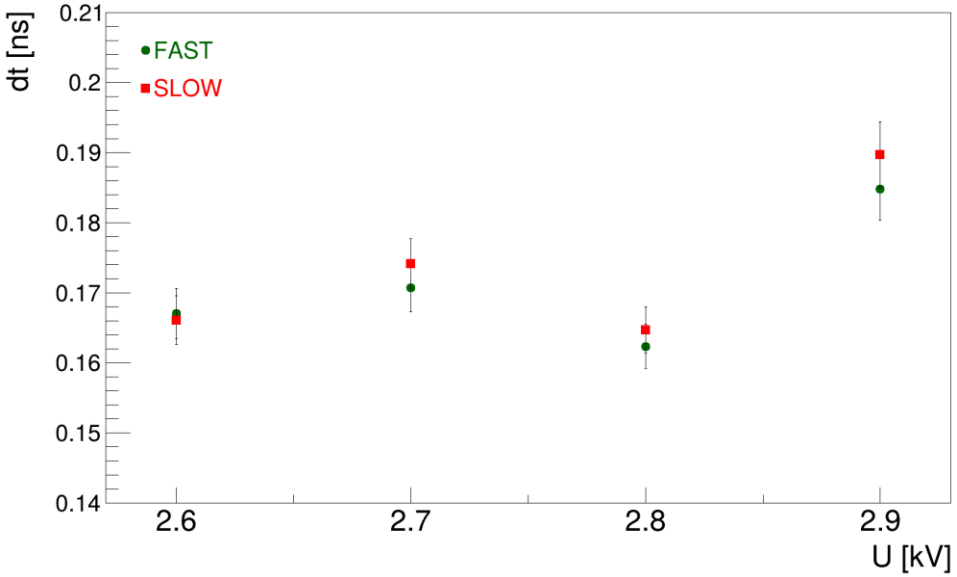
Track selection to improve time resolution

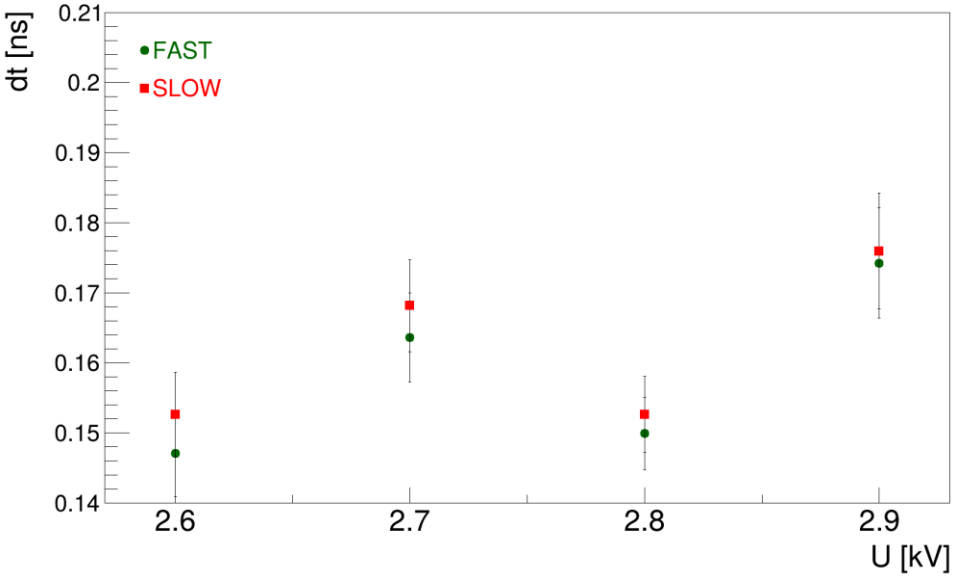
To remove inclined tracks



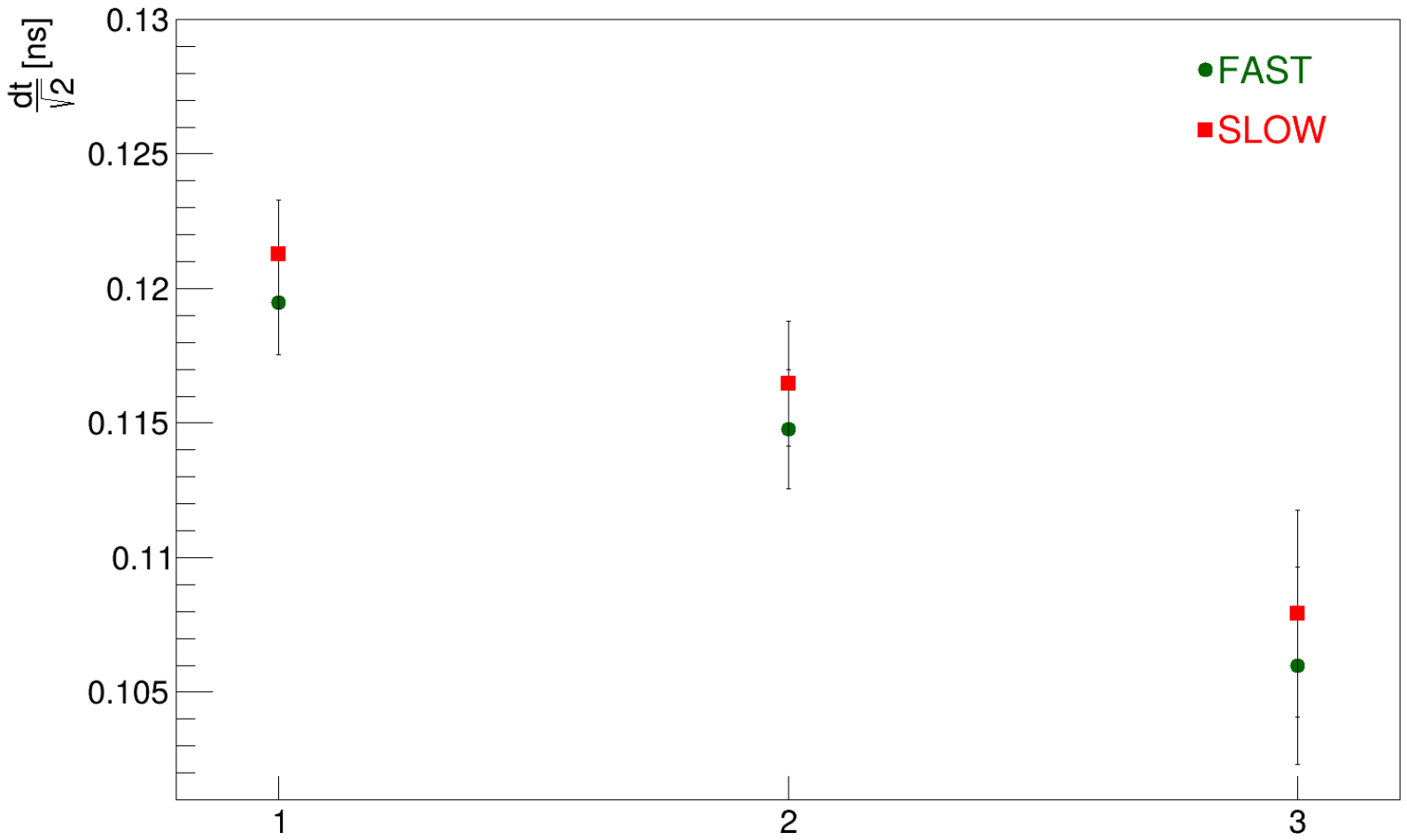


To remove inclined tracks along the strip

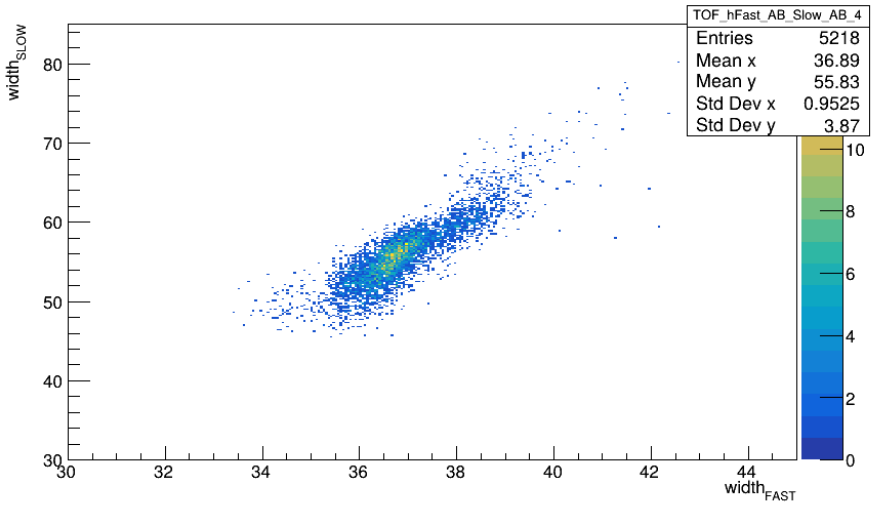


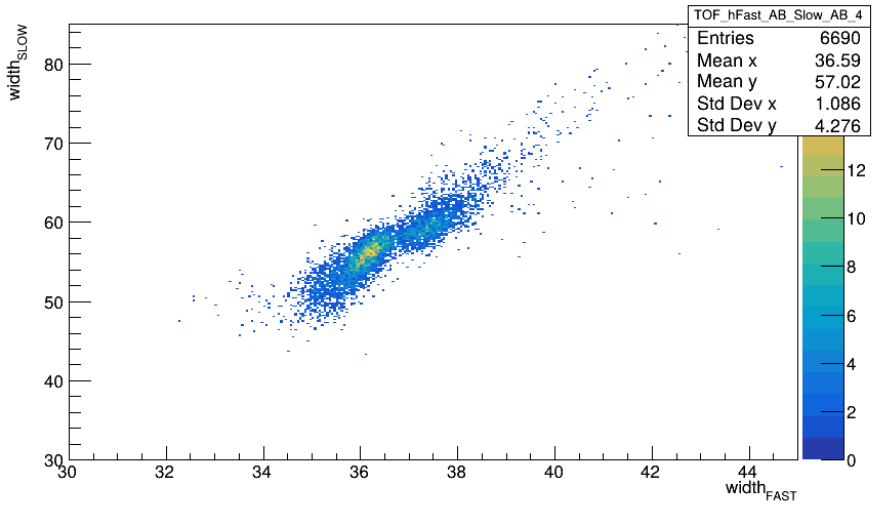


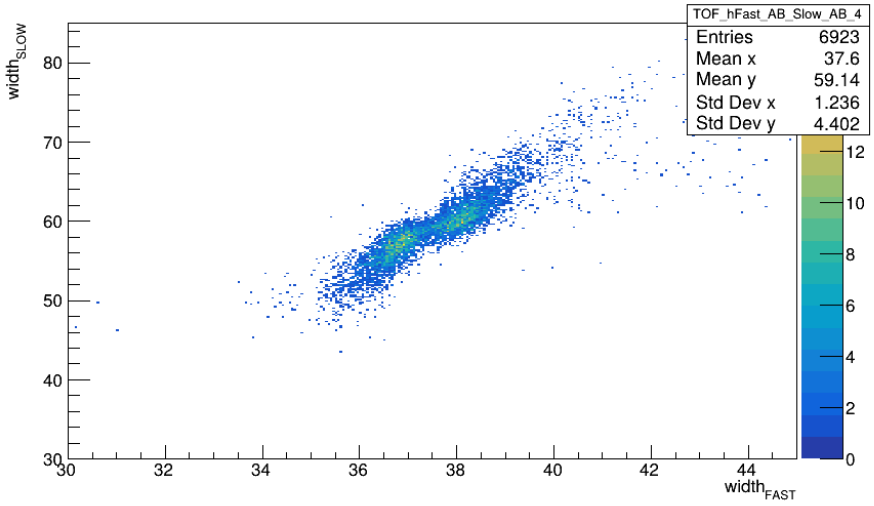
Time resolution by 3 steps of correction for 2.8kV

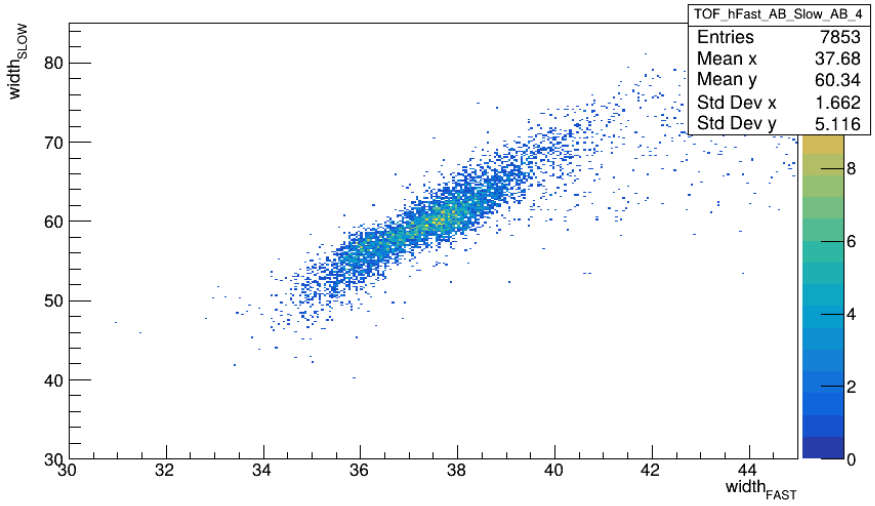


Fast vs. Slow to explain absence of improvement









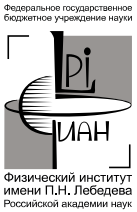
The only way to do great work is to love what you do. (S. Jobs)



- **Sergei Morozov, Evgeni Usenko**



- **Artem Ivanov**
- **Mikhail Rumyantsev**
- **Mikhail Buryakov**



- **Andrei Snesarev & Protvino team**



- **Lei Zhao, Jiajun Qin, Dongdong Hu**

I'm proud to work with such an amazing coworker.

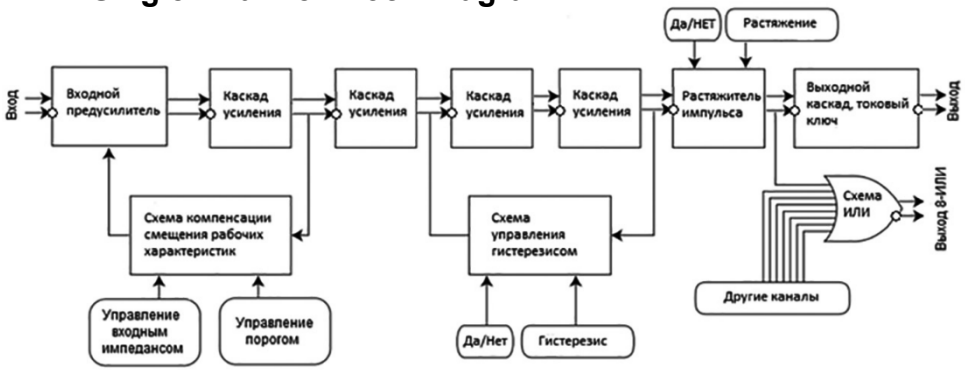
Status of RUNO development

Valery Chmill



Technical proposal for RUNO run#3

Single Channel Block Diagram



ALEXANDRE SOLIN, ALIAKSANDR SOLIN, INSTITUTE FOR NUCLEAR PROBLEMS, MINSK

Objective and Purpose of the Work

Development of the RUNOv1 IC prototype for the readout electronics of the RPC cameras of the NICA-SPD project.

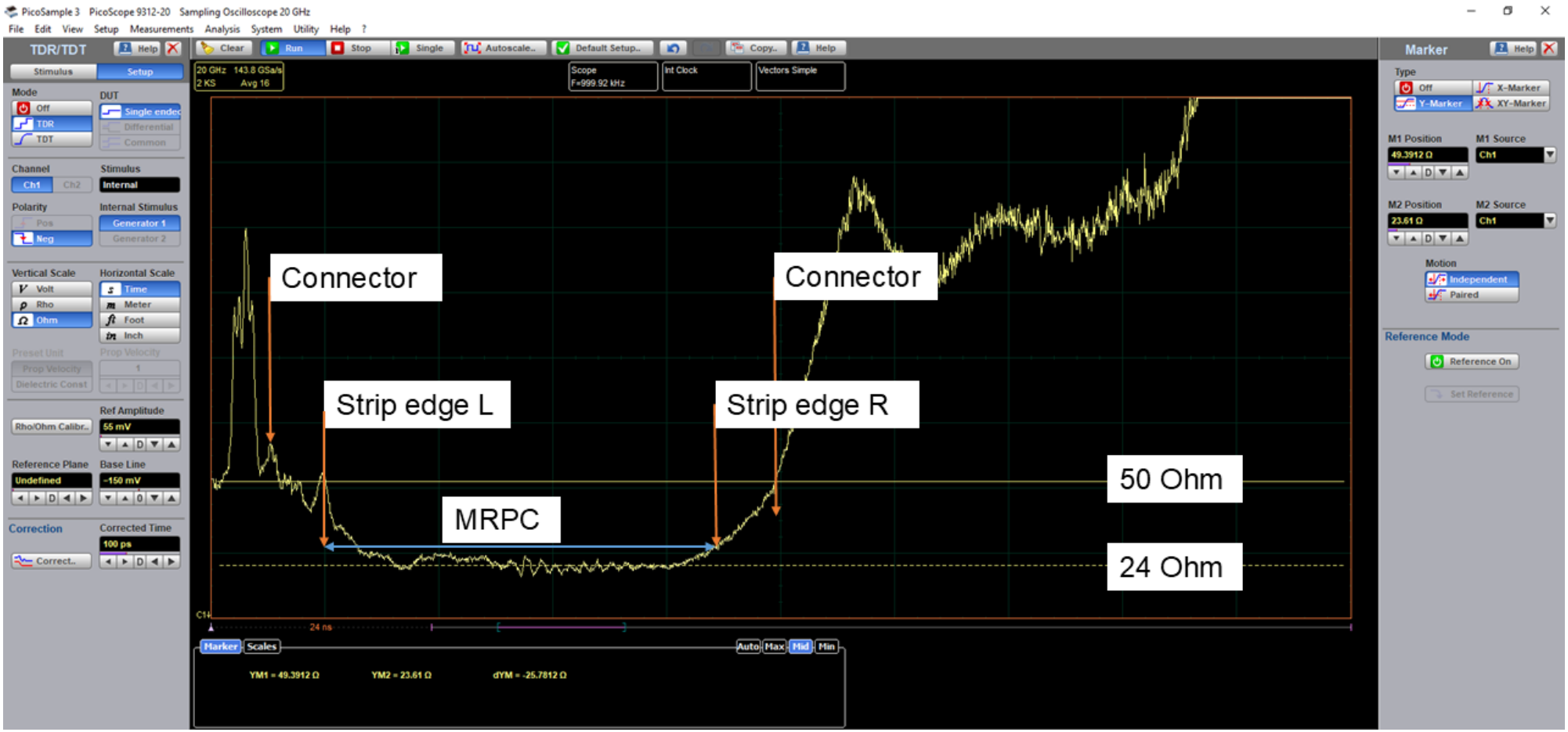
Work Content:

1. Development of the IC's schematic diagram and topology.
2. IC simulation and post-simulation.
3. Preparation for transferring the IC's GDS file to the semi-conductor foundry.

Параметры детектораи линии передачи	
Емкость детектора, пФ	10
Максимальный сигнал, пК	1.5
Фронт сигнала, пс	<200
Сопротивление линии передачи, Ом Две 110-омные параллельные линии	55
Длина линии передачи, см	<20
Загрузка канала, МГц	<10
Параметры ИС	
Технология	CMOS
Проектные нормы, нм	180
Напряжение питания, В	1.8
Количество каналов	8
Рассеиваемая мощность, мВт/канал 3-й приоритет	<30
Время формирования, нс 1-й приоритет	1
Линейный динамический диапазон предусилителя, фК	0÷100
Коэффициент преобразования для заряда, мВ/фК	>1000
Напряжение смещения по входу (дифференциальное), мВ	<3
Шум (RMS), е 2-й приоритет	<2500
Гистерезис, В	0÷0.9
Порог дискриминатора, фК Внешняя установка	10÷100
Коэффициент преобразования для порога, мВ/фК	4÷5
Джиттер, ps При входном сигнале	<15
Time walk, пс	<50
Входное сопротивление (дифференциальное), Ом Соответствует входному сопротивлению линии передачи	55
Уровни выходных сигналов (дифференциальные) Задаются внешними элементами	LVDS
Диапазон выходных токов, мА	1÷6
Диапазон растяжения импульса, нс	0÷100
Типовая длительность импульса, нс	15
Разброс длительности импульса, %	<15
Кросс-ток между каналами, дБ	-50

Impedance measurements for Protvino MRPC

Unipolar readout mode



Status of DISA Differential current(I) Saturation Amplifier development

Valery Chmill





To be continued (DREAMS or reality)

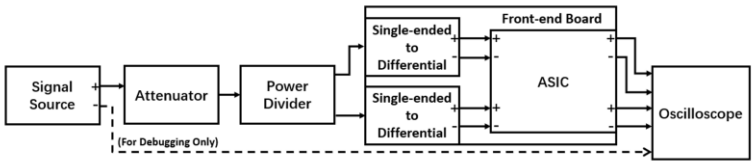
- Functionality verification and test of **DISAv2** design and prove of FEE.
- TDC implementation into **DISAv3** module
- Stand alone FPGA based TDC 64 ch module test and possible modification.

- ***A Fully Functional MRPC Readout Module:*** *A compact, high-density, low-power PCB providing 64 channels of readout, integrating DISA ASICs and an FPGA-TDC or TDC ASICs, optimized for the signal profile of MRPCs.*
- ***Publications:*** *Results will be presented at international conferences (e.g., IEEE NSS/MIC) and published in peer-reviewed journals (e.g., NIM A).*
- ***Strengthened Collaboration:*** *Establishment of a strong foundation for future joint projects in detector electronics for high-energy physics experiments between JINR and PRC institutions.*
- ***A Versatile Platform for Gaseous Detectors:*** *The developed system will serve as a key building block for future MRPC-based ToF systems in major experimental facilities.*

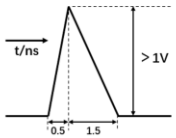
Spare parts (slides)



DISA evaluation Board description and test parameters

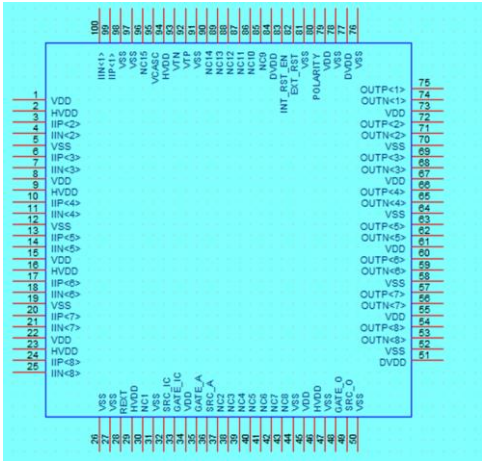


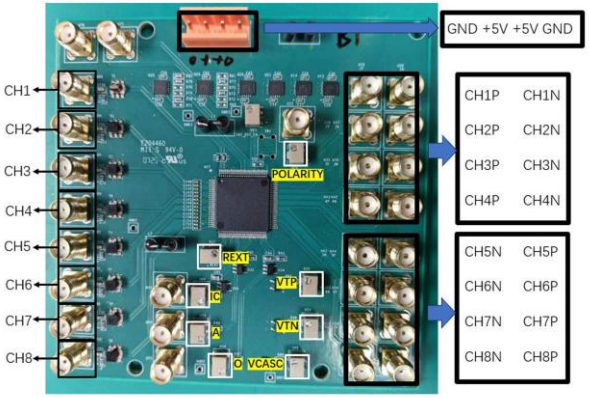
Test System Block Diagram



Test Waveform

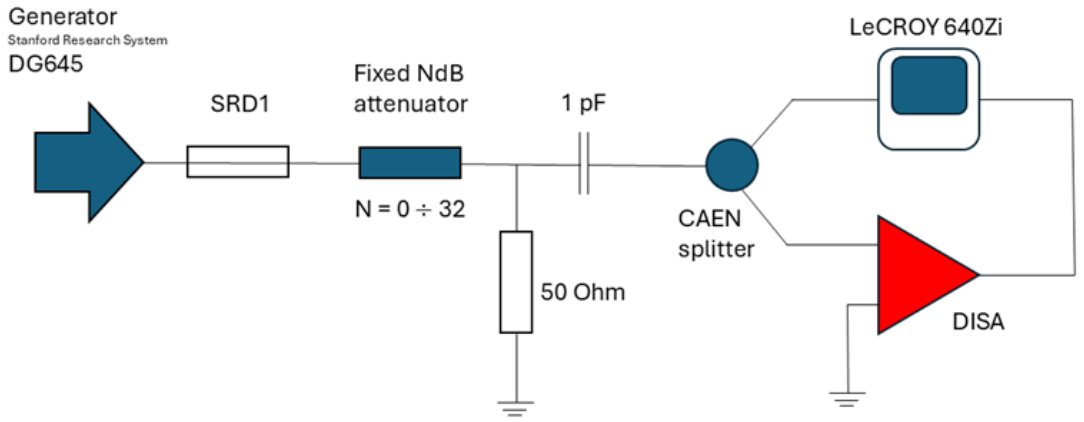


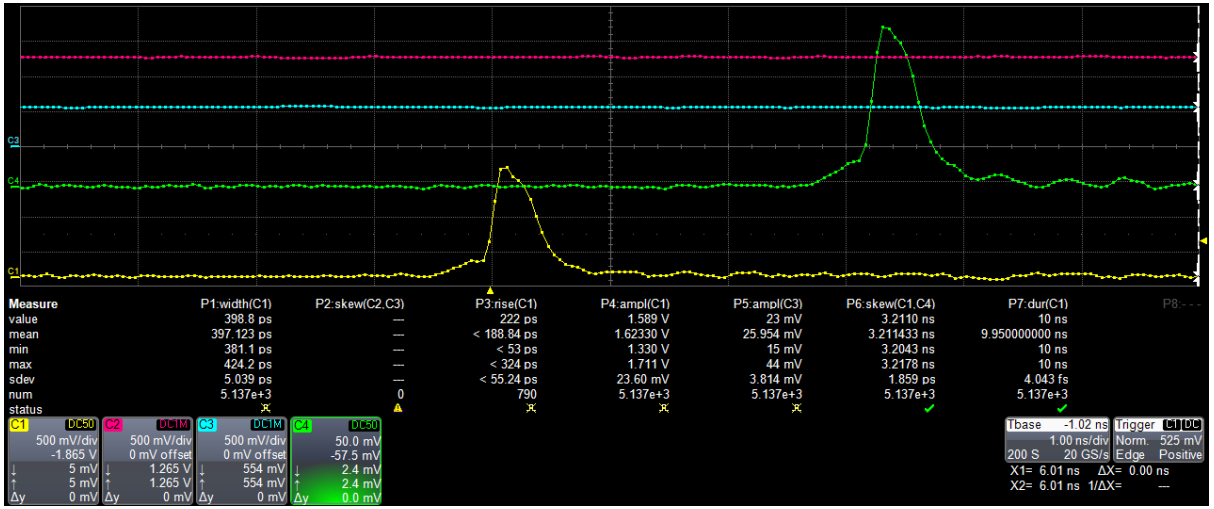




Bias Set	Recommend Value
REXT: External resistor for impedance matching	45Ω
VTP: Threshold Voltage at P Terminal (VTP is positive when polarity is 1, and negative otherwise)	0.697V
VTN: Threshold Voltage at N Terminal (VTP is negative when polarity is 1, and positive otherwise)	0.873V
VCASC: Input Stage MOSFET Common-Gate Voltage	1.352V
IC: Amplifier Stage Internal Current Compensation	0.806V
A: Internal Amplifier Circuit Current Setting	0.434V
O: LVDS Output Level Setting	1.092V
POLARITY: Signal Polarity Control, Set to "1" for Positive Signal on P Terminal(Output Pin), Set to "0" for Negative Signal on P Terminal. "0" Indicates High Level(1.8V).	1.8V (POLARITY=0)
Attention: Adjust VTP and VTN as needed. Note that too small differential voltage may cause noise-induced signal triggering.	Attention: The measurement of the recommended value is described in the illustration below.

Performance Characterization and Time Resolution Analysis





Self-jitter characterization of LeCroy Wave Runner 640Zi oscilloscope.

High-Performance Setup:

Pulse generator with <100 ps rise time.

LeCroy oscilloscope with 1.87 ps intrinsic jitter (4 GHz BW, 40 GS/s).

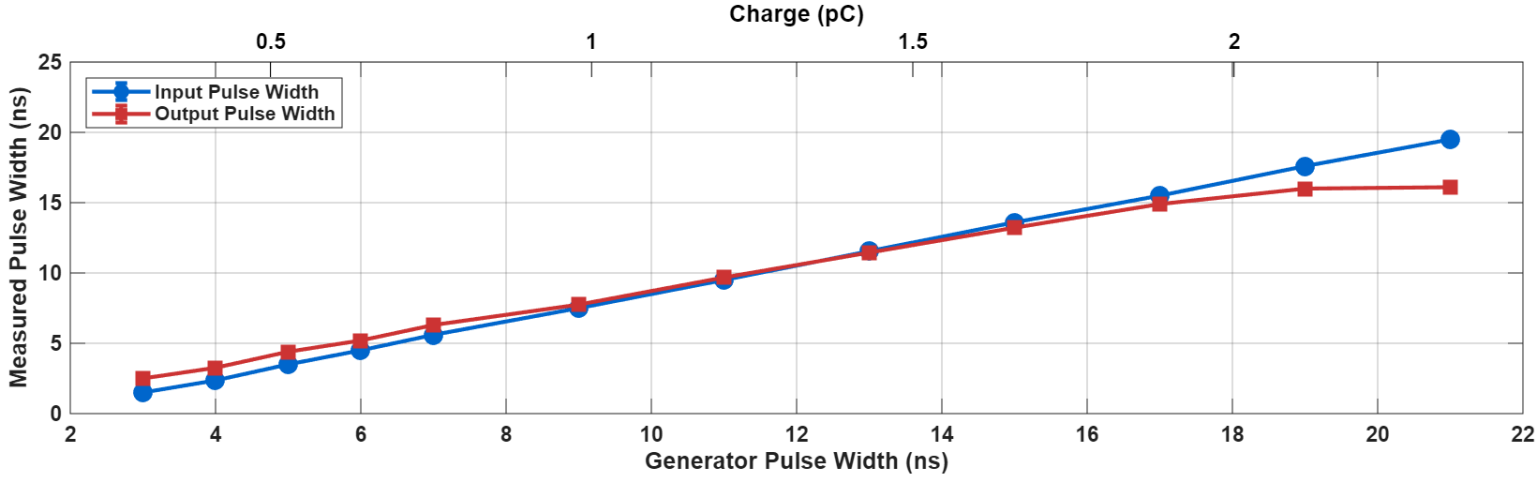
System Sensitivity:

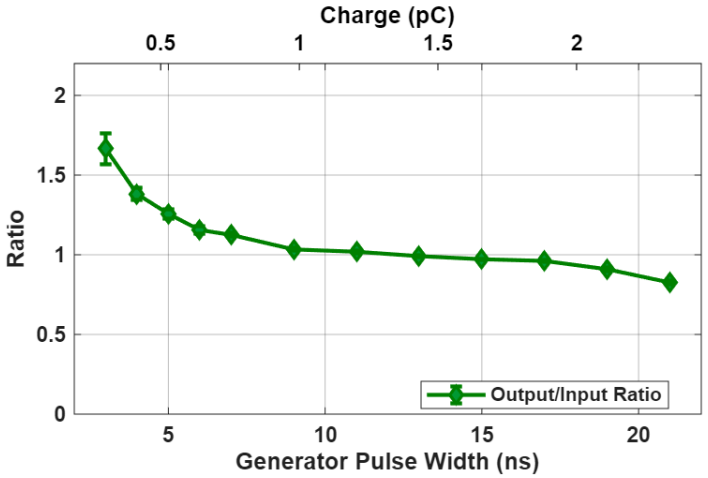
Minimum detectable charge: 86 fC ???

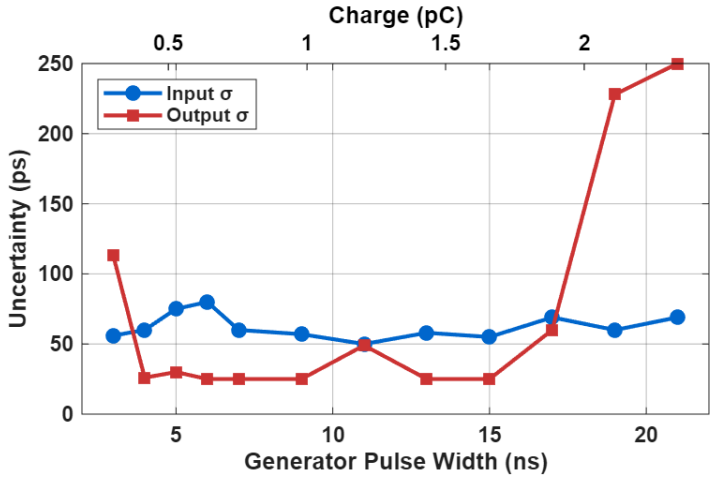
Stable operation confirmed down to 5.5 mV threshold.

Key Finding: System achieves picosecond-level timing resolution.

Linear response to injected meander shaped charge







Threshold = 147 mV we had stable LVDS pulse on 32dB and factor /2 from CAEN splitter.
32dB+splitter = 39.8*2 scale factor for Amplitude.

DISA second calibration test with delta function

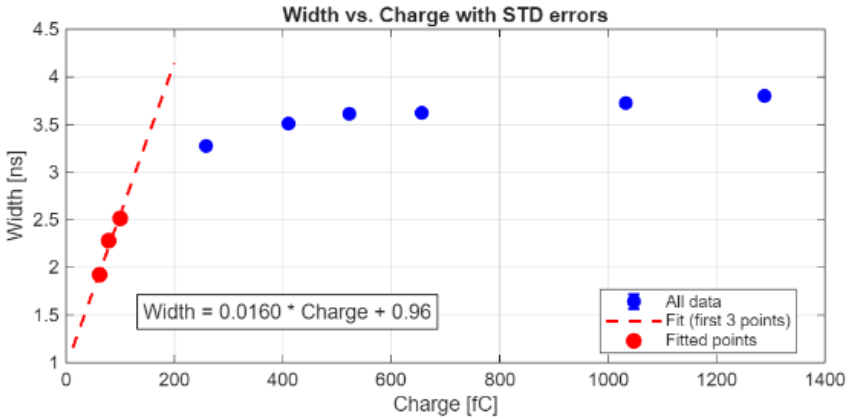
The conversion factor comes from the fit:

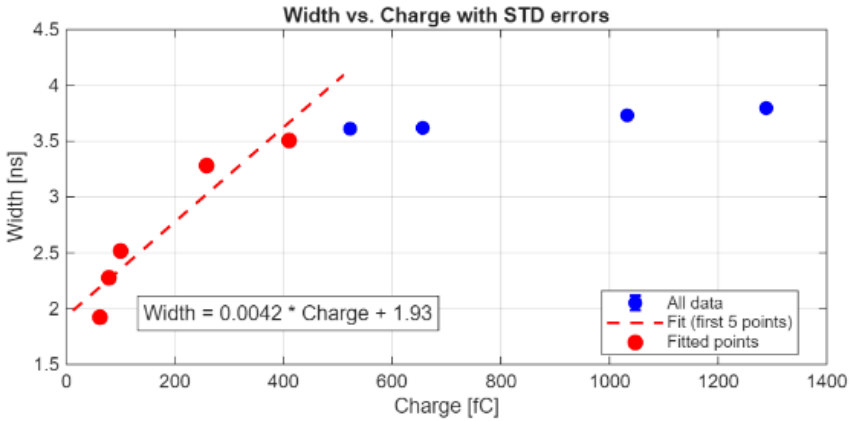
Width = A ·Charge + b, where A is in **ns/fC**.

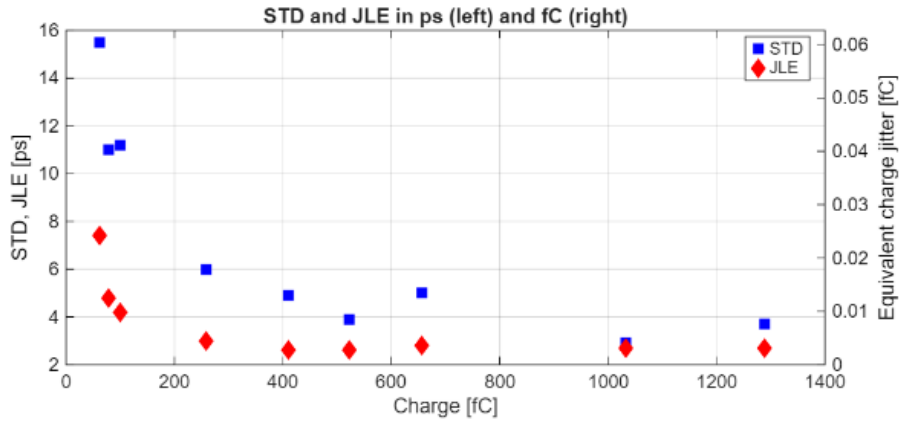
The derivative d(Charge)/d(Width) = 1/A (fC/ns).

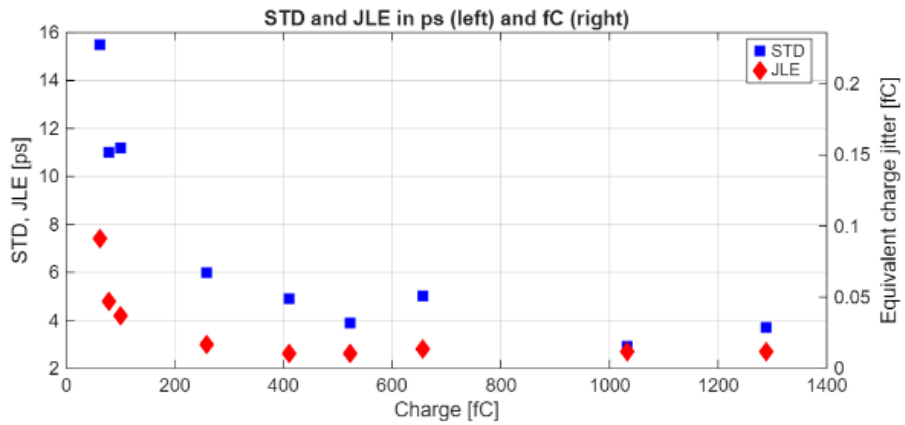
To convert a time interval Δt in ps to an equivalent charge ΔQ in fC:

$$\Delta Q = \Delta t\ [ps] \times \frac{1}{A}\ [fC/ns] \times \frac{1\ ns}{1000\ ps} = \frac{\Delta t}{A \cdot 1000}\ [fC]$$

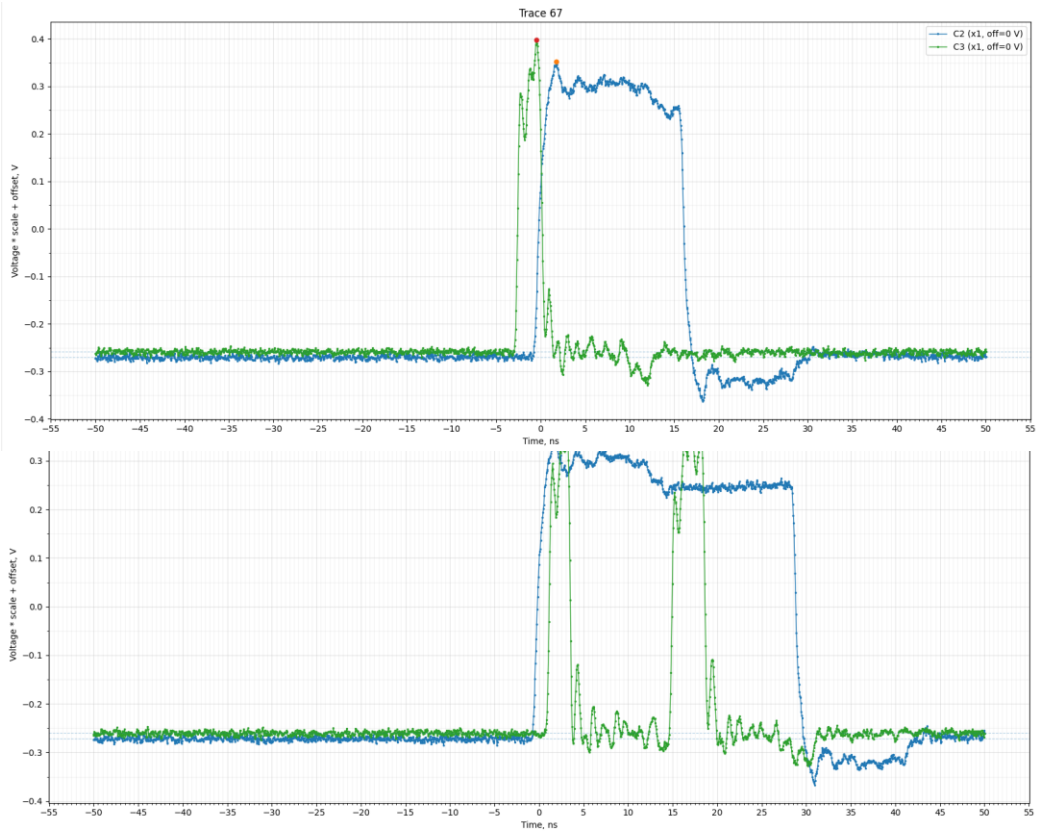






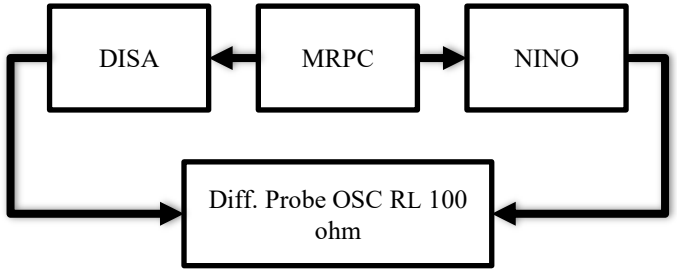


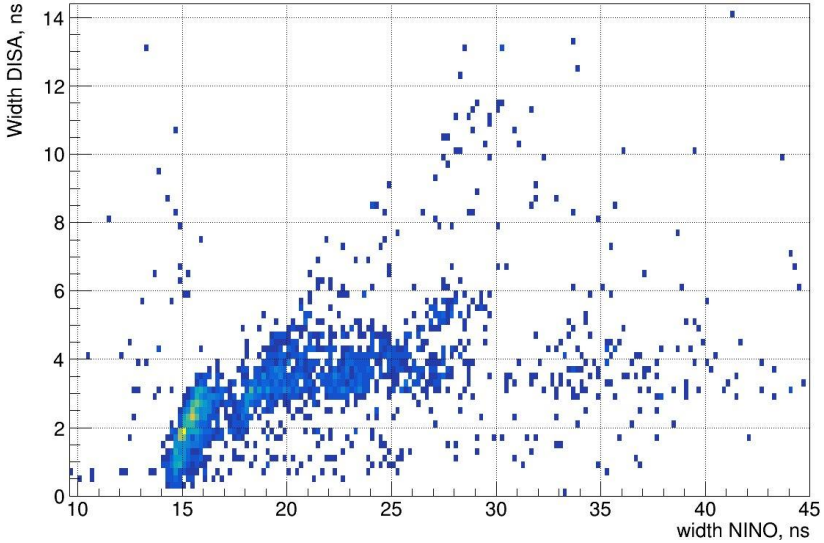
DISA and NINO response to MRPC signals comparison



Green – DISA, Blue – NINO

Stretcher is ON

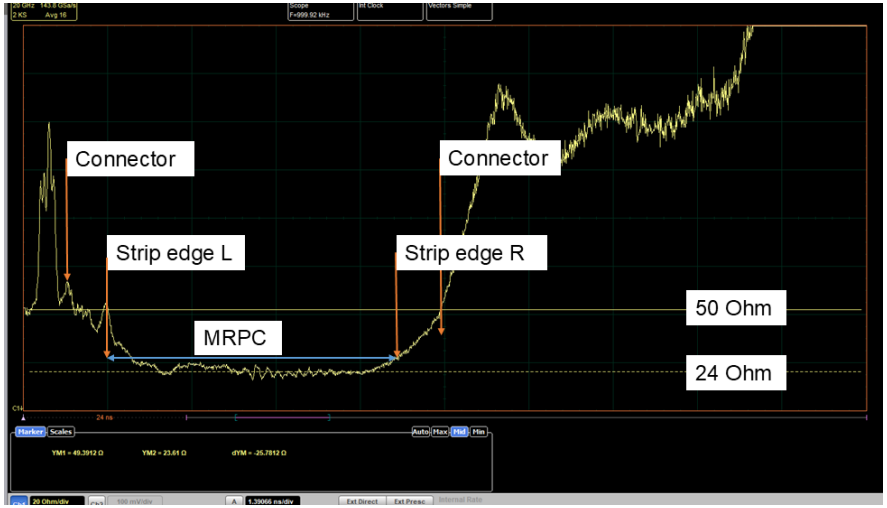


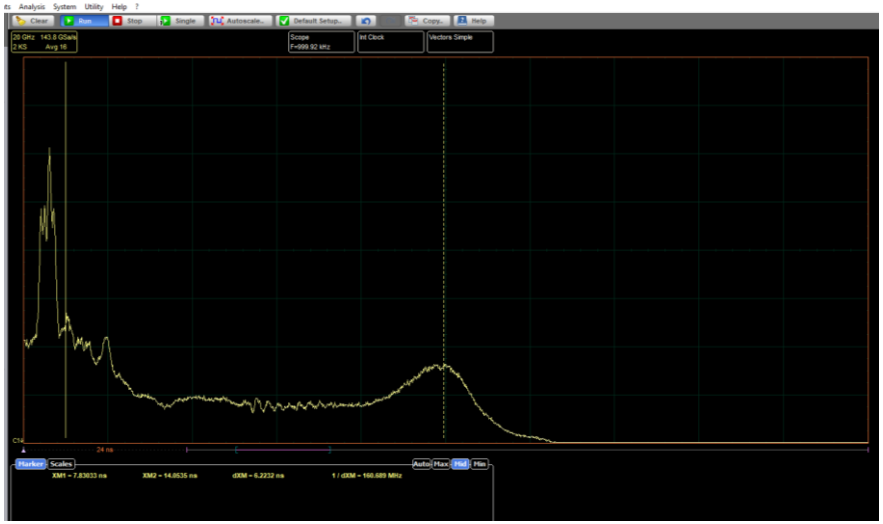


Pulse width distribution FEE for one same strip MRPC

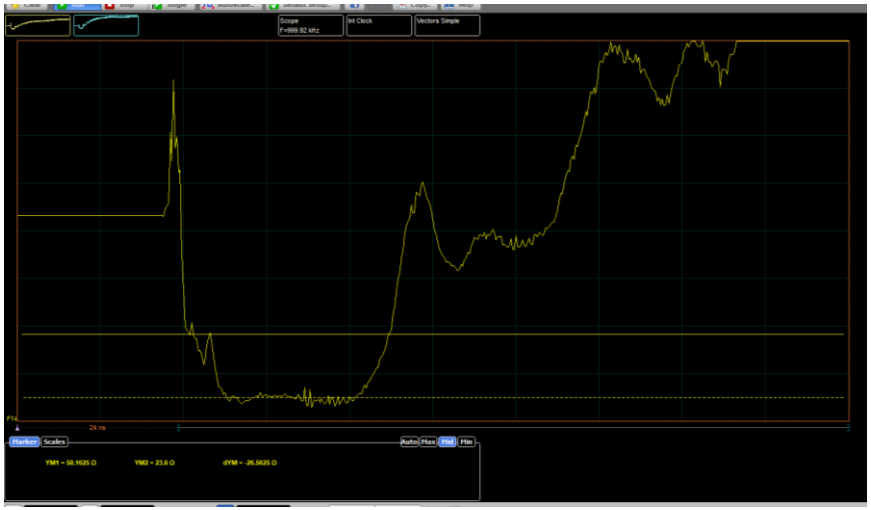
Impedance measurements for Protvino MRPC

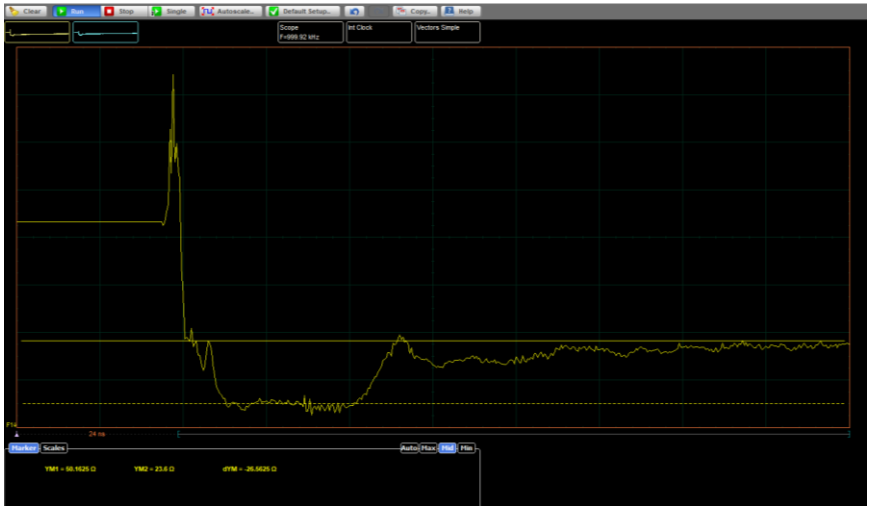
Unipolar readout mode





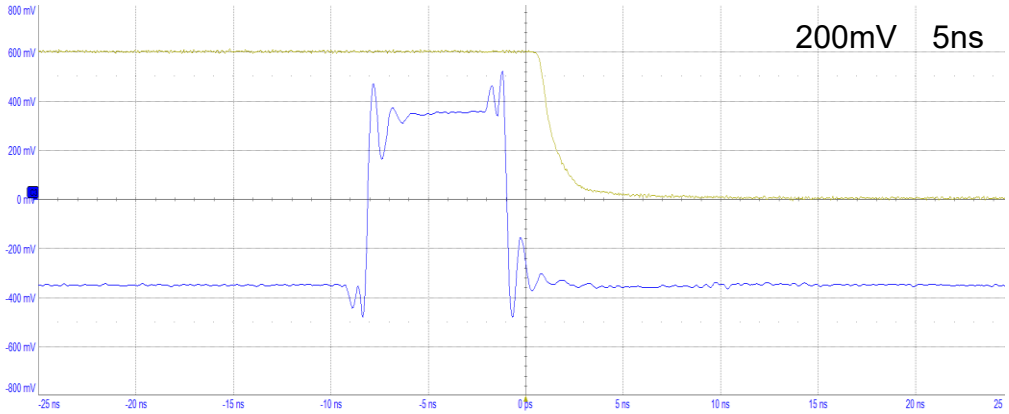
Differential readout mode



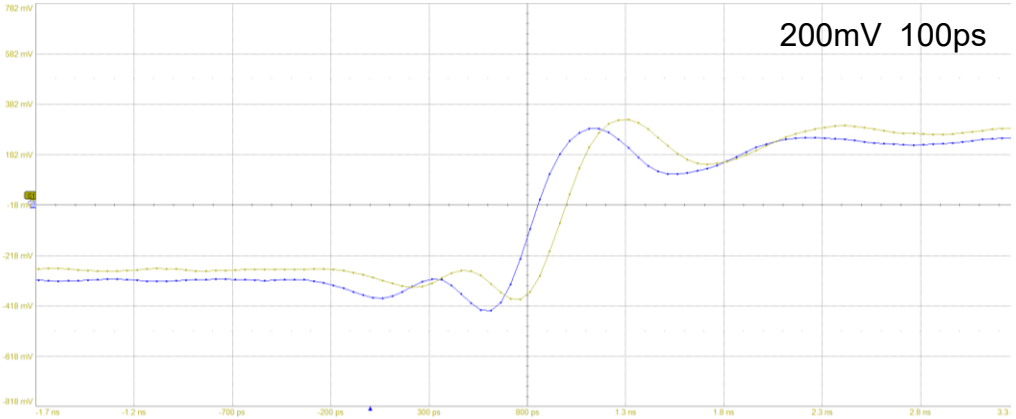


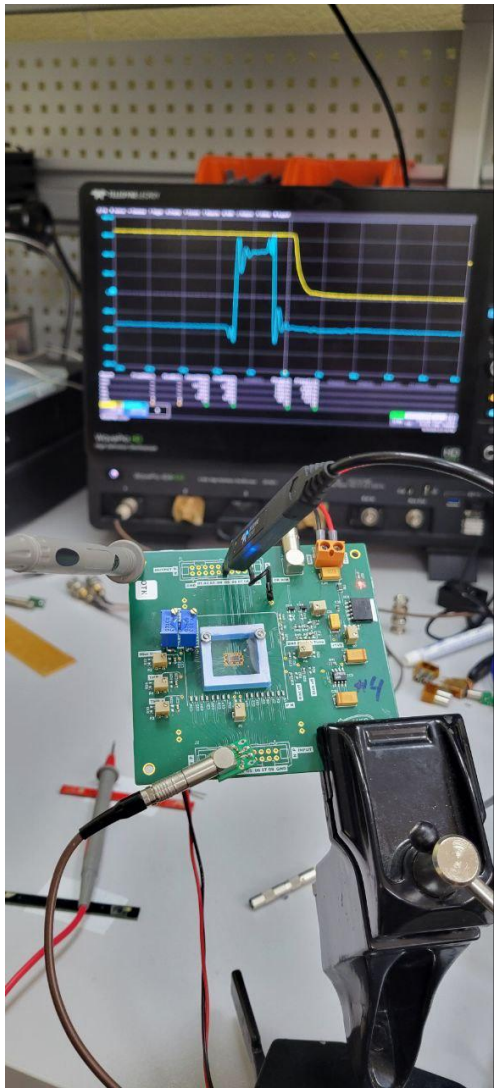
RUNO run#2 Chip ver#3

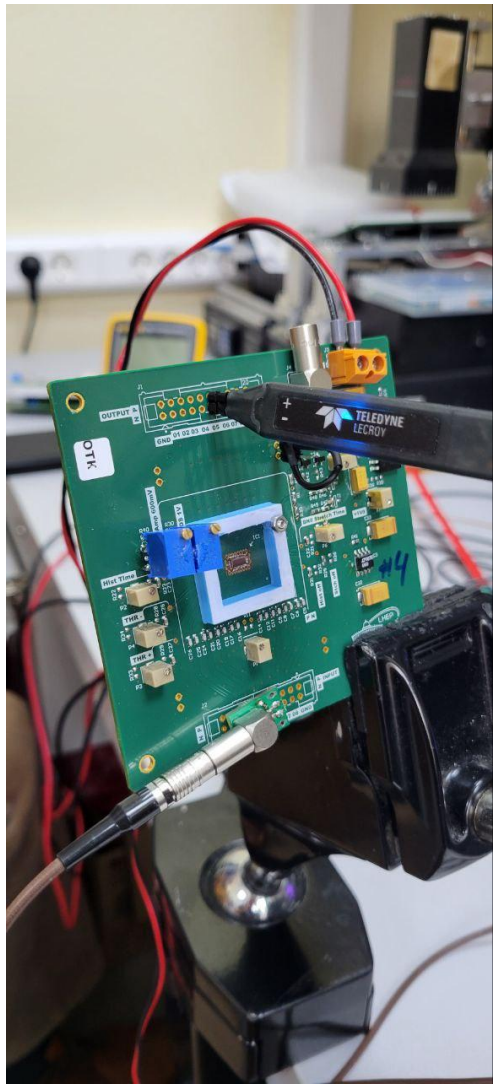
Minimum injected charge 15fC



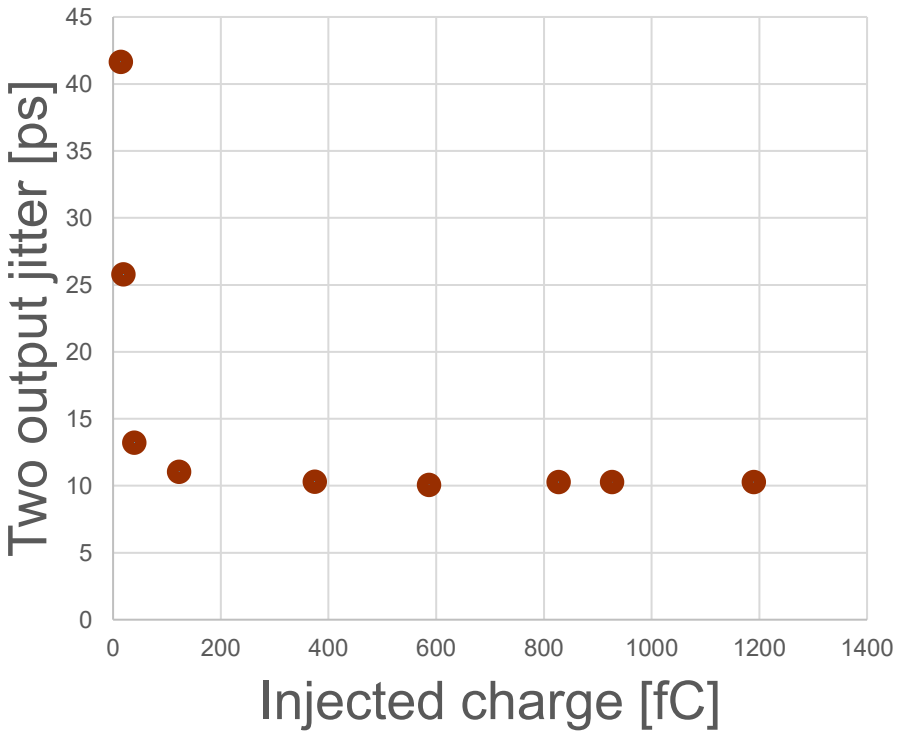
Intrinsic jitter 10ps

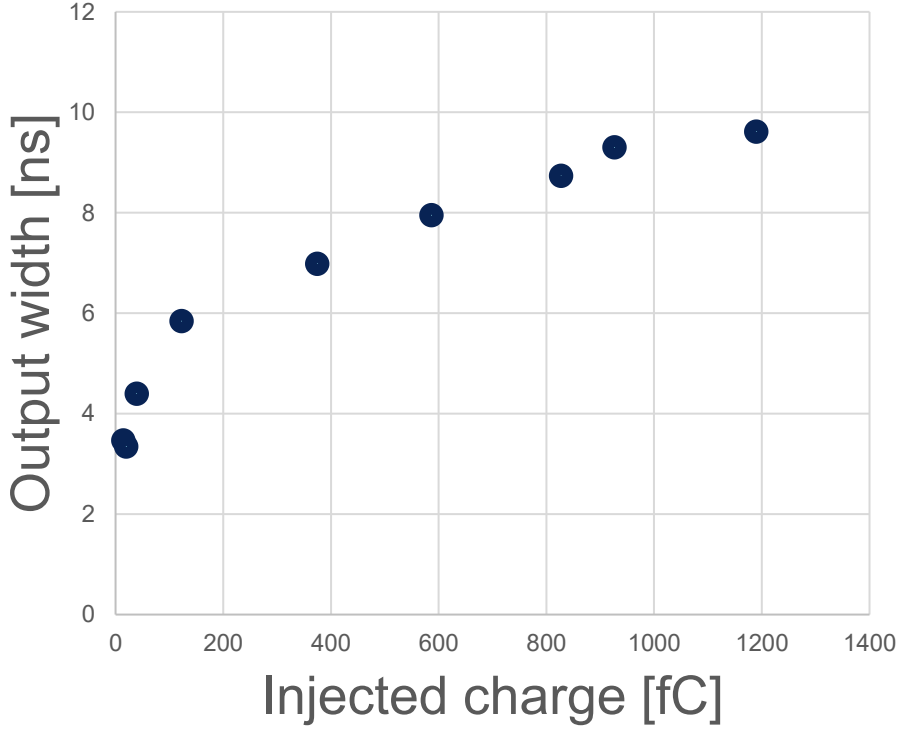






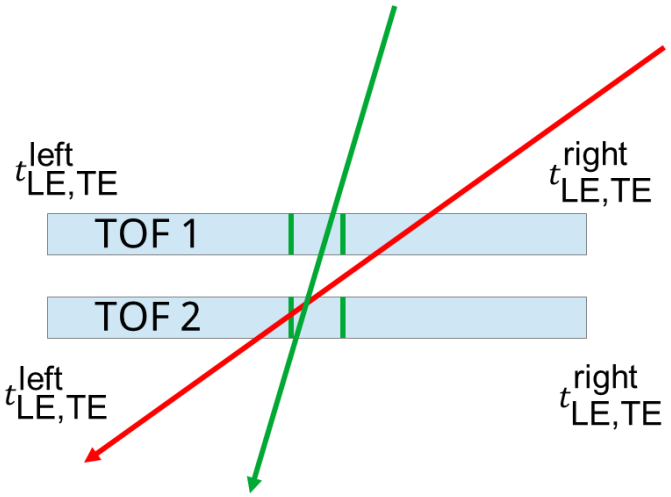
RUNO run#2 Chip ver#3



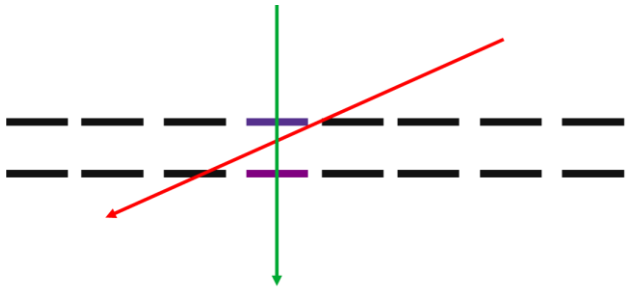


Input impedance is equal to 65Ohm, power consumption was: 1.8V*(0.166A-0.017A)/8=33.5mW/ch.

Track selection to improve time resolution



To remove inclined tracks



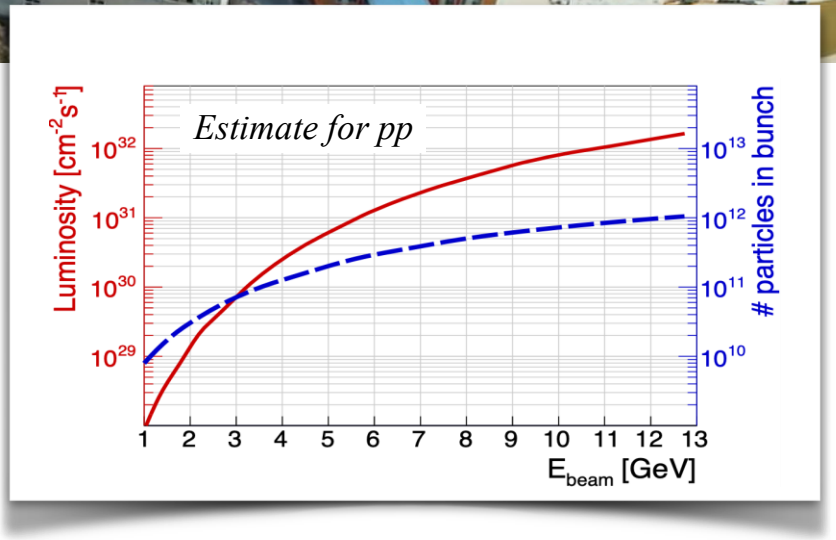
To remove inclined tracks along the strip

Accelerator complex NICA at JINR

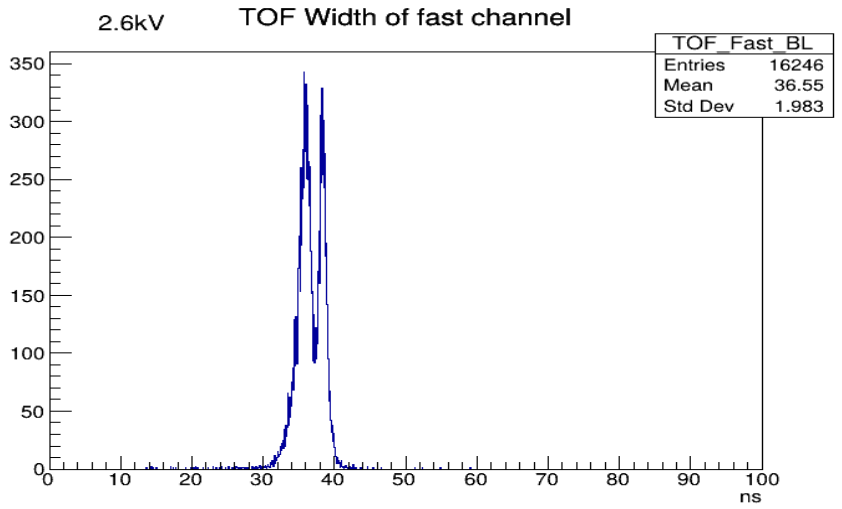


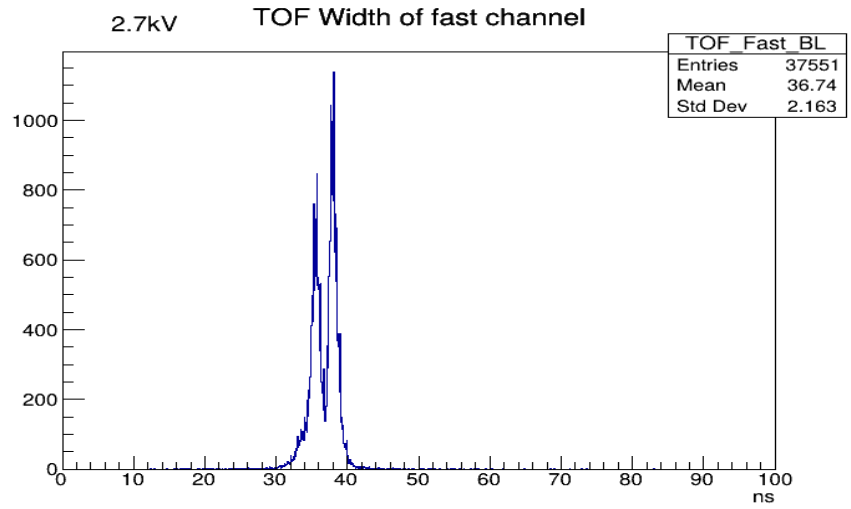
SPD project

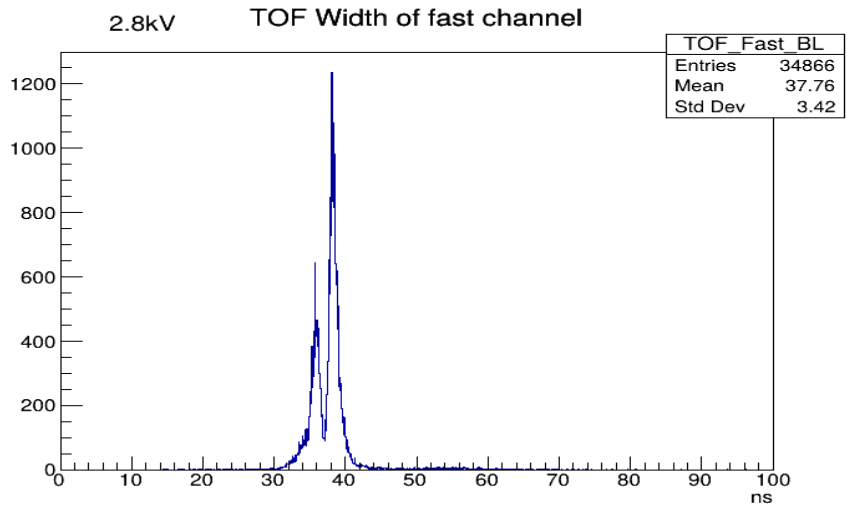
- SPD (Spin Physics Detector) is a universal facility with the primary goal to study *unpolarized and polarized gluon content of proton and deuteron*
- SPD project was approved in JINR and had its first proto-collaboration meeting in June 2019
- Conceptual Design Report (CDR) was released in January 2021, [arXiv:2102.00442]
- Official birthday of the SPD collaboration in June 2021
- Technical Design Report (TDR) of SPD was released in January 2023, NSR 1 (2024) 1, [arXiv:2404.08317], *http://spd.jinr.ru*

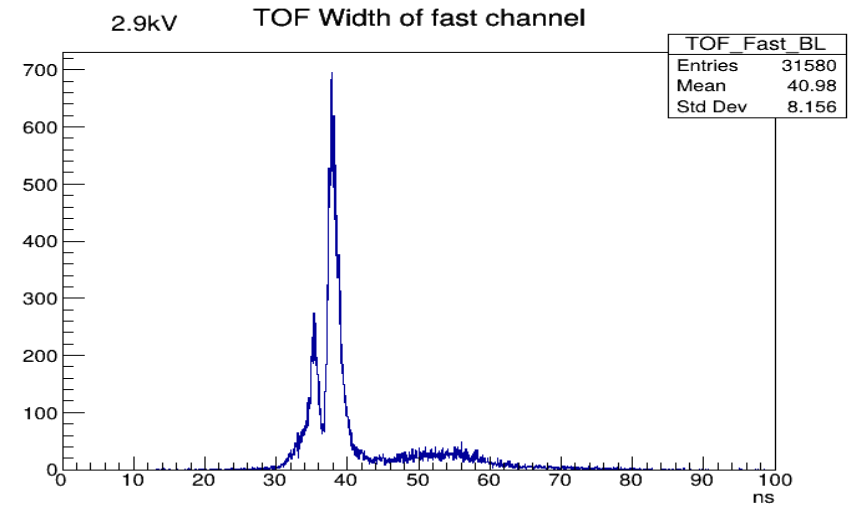


Width spectra for fast channels

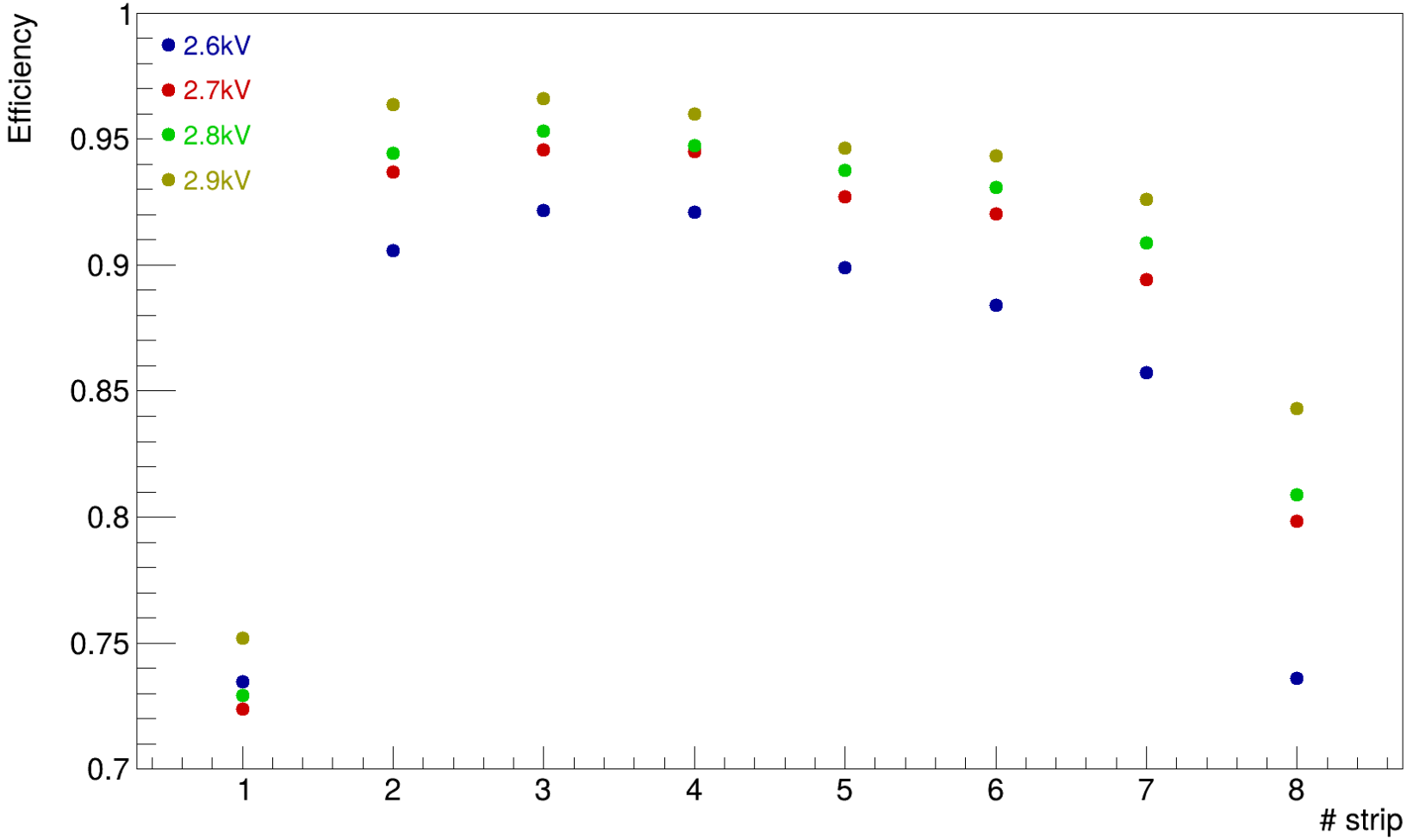






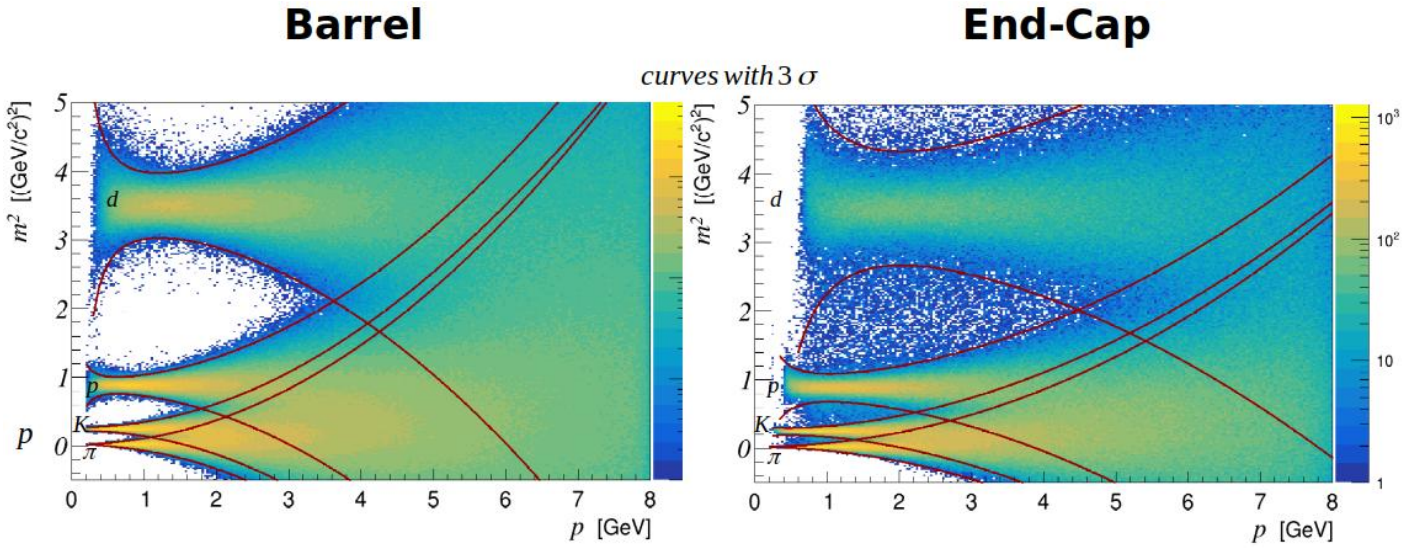


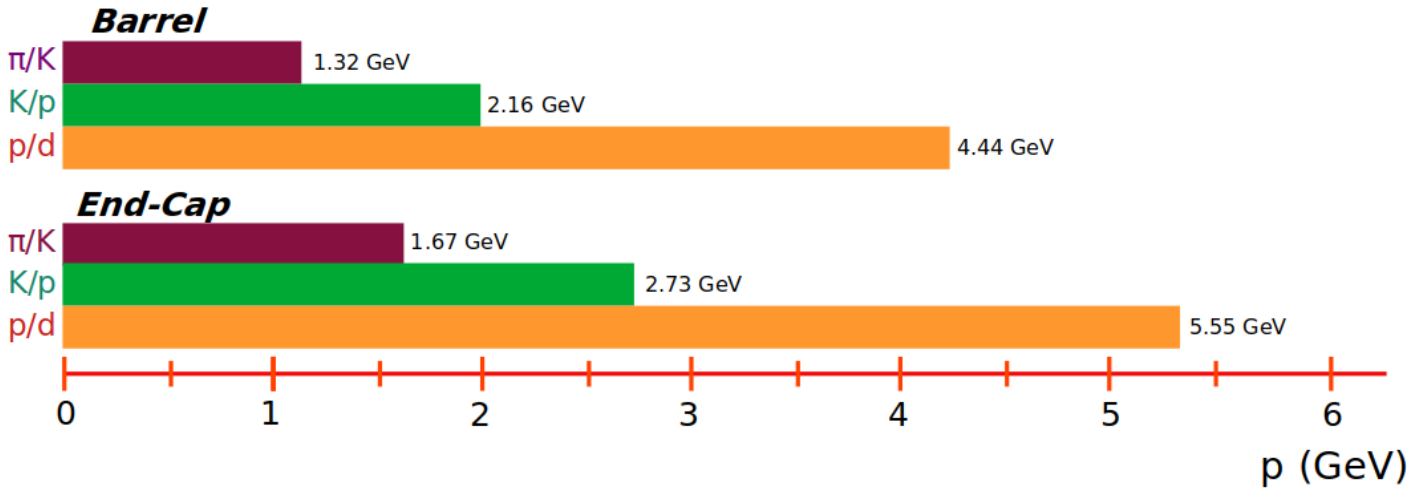
Detection efficiency



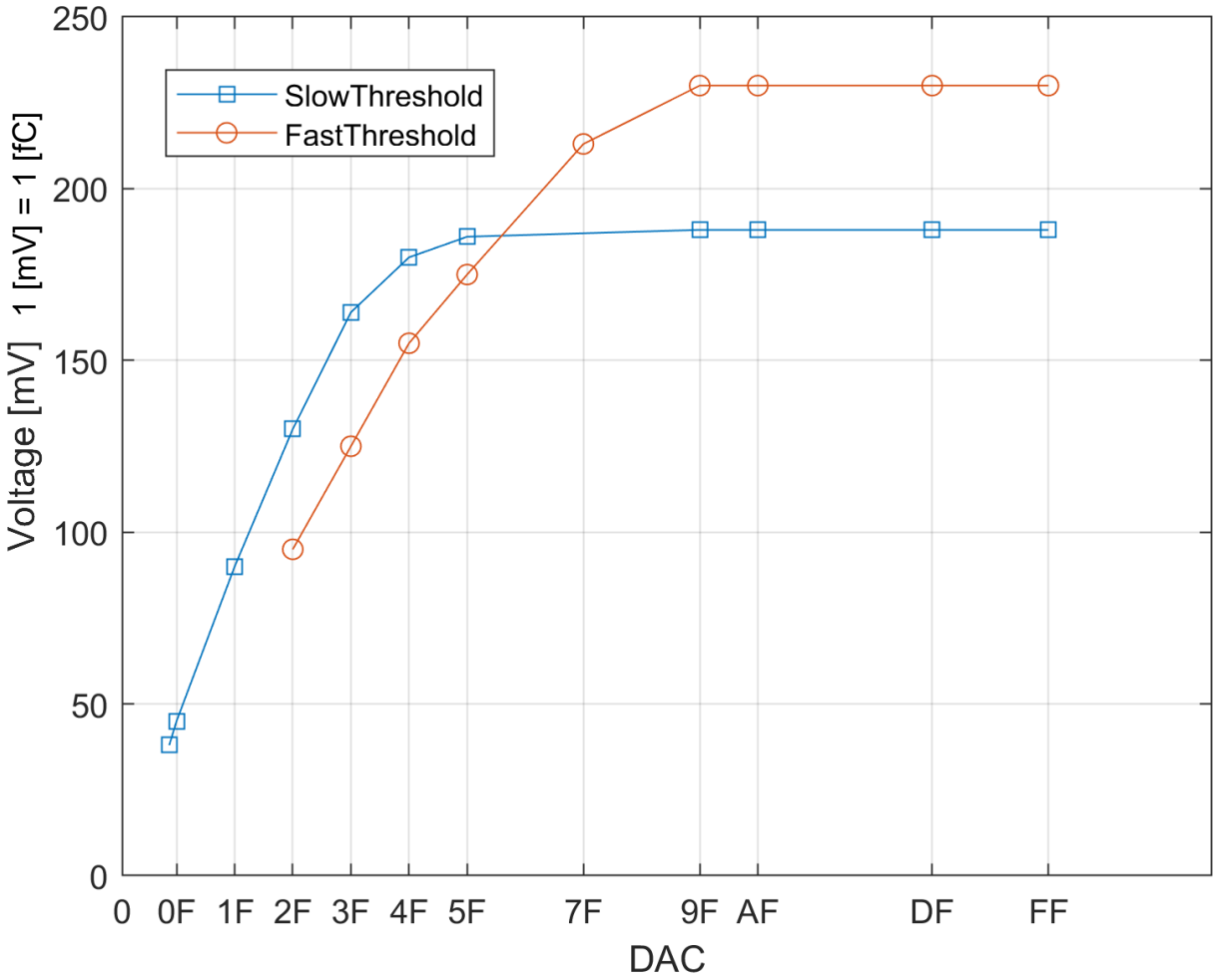
Particles ID for m^2 vs. p

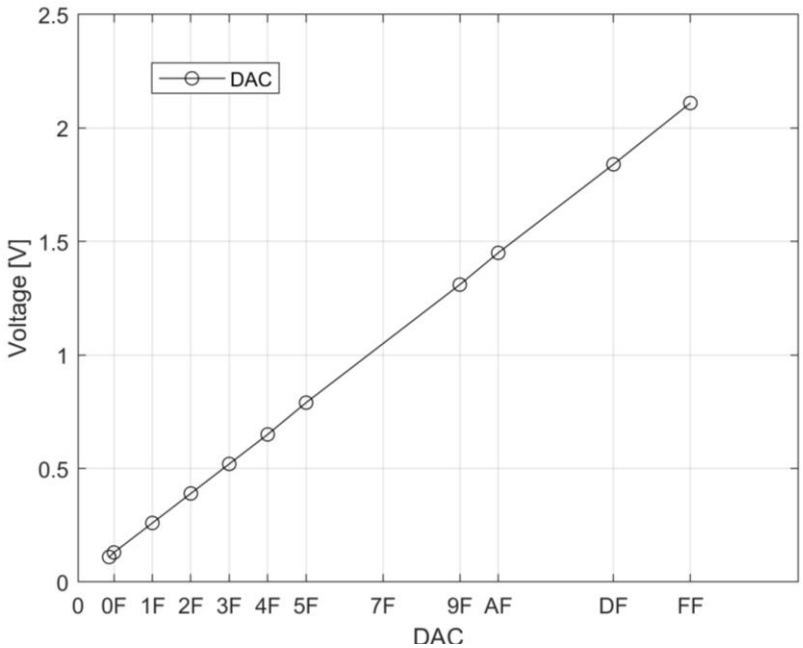
- π/K/p/d discrimination for momenta <2 GeV
- Determination of t0
- Time resolution requirement <60 ps.





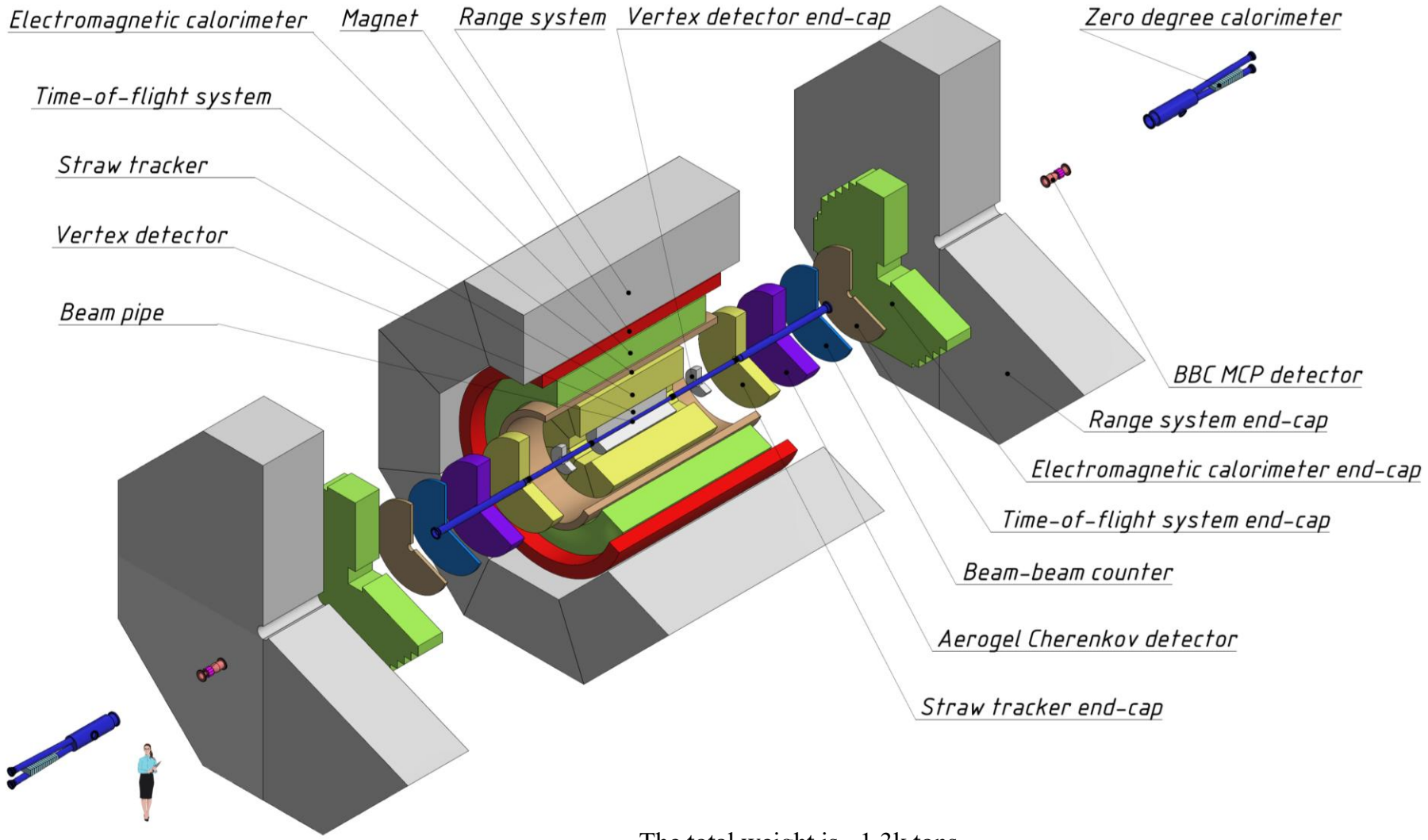
Threshold for Fast and Slow FEE output





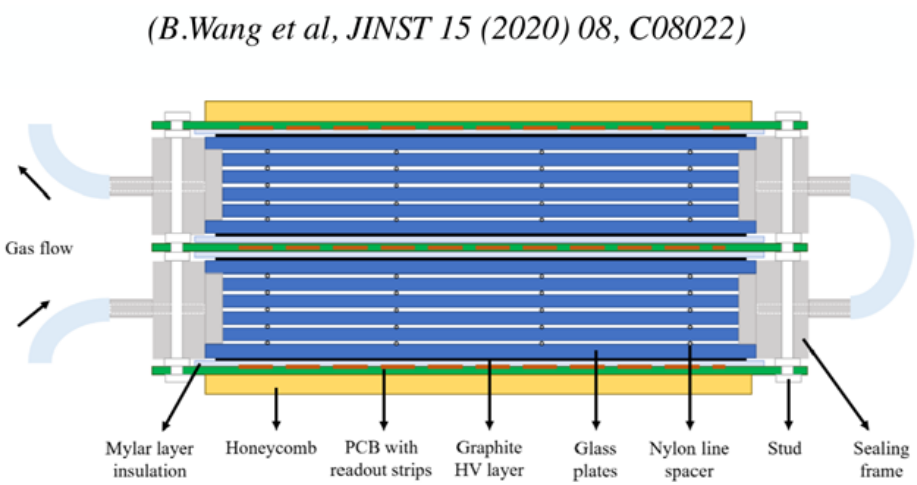
Counts on Fast and after for Slow channels becomes equal to triggers number (Threshold)

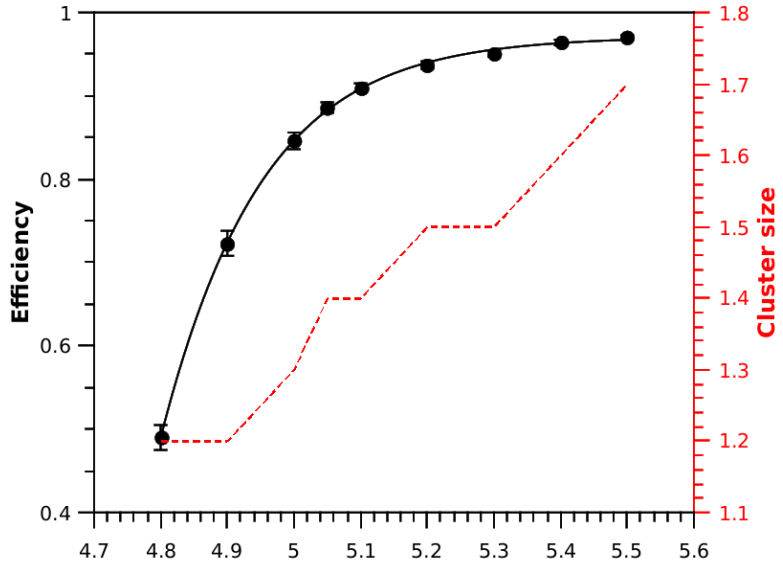
Schematic view of the SPD setup



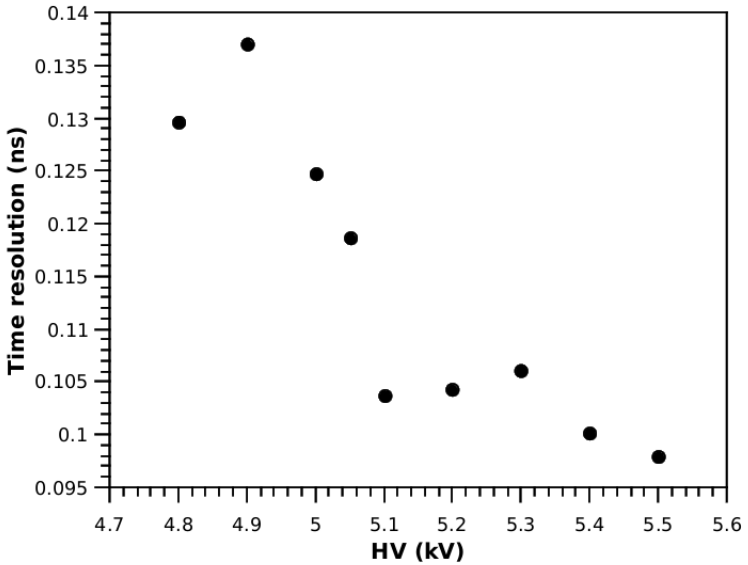
The total weight is ~1.3k tons

Sealed (MRPC) are the base option of today



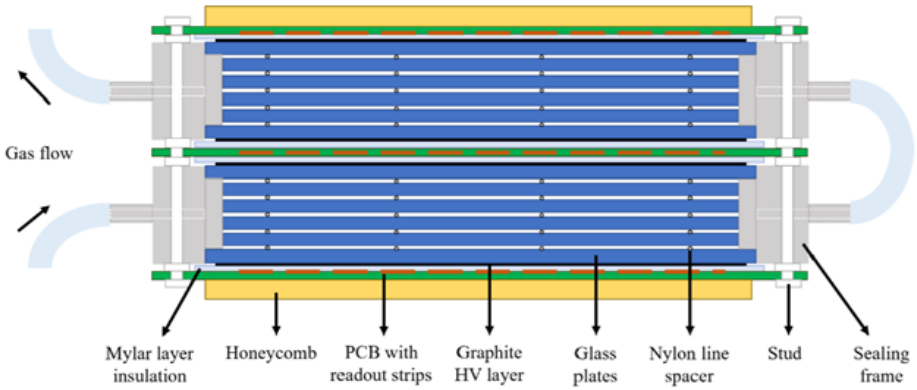


- The prototype was tested in cosmic rays along with 2 MRPC2 counters in the TRBv3 test stand.
- The plateau efficiency is 97%, with a 1.6 cluster size and a 100 ps flight-time resolution.
- The systematic time resolution of the prototype is about 60 ps. if we reasonably expect the same timing precision between two MRPCs.
- The prototype has the same working point at ±5.4 kV with standard gas flow (Freon/iC_4H_{10} = 90/5/5

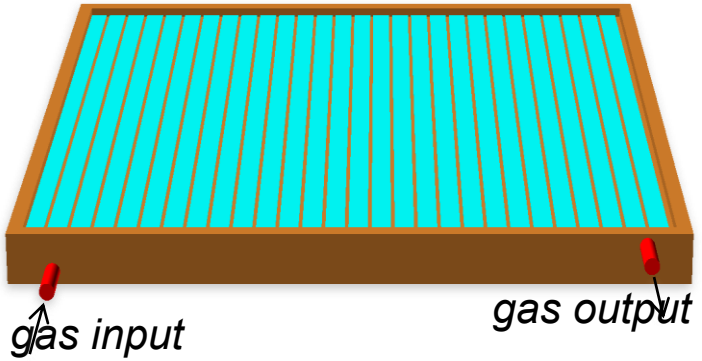


Sealed MRPC for SPD TOF

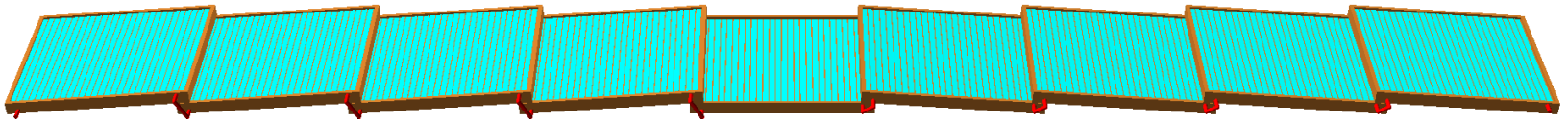
(B.Wang et al, JINST 15 (2020) 08, C08022)



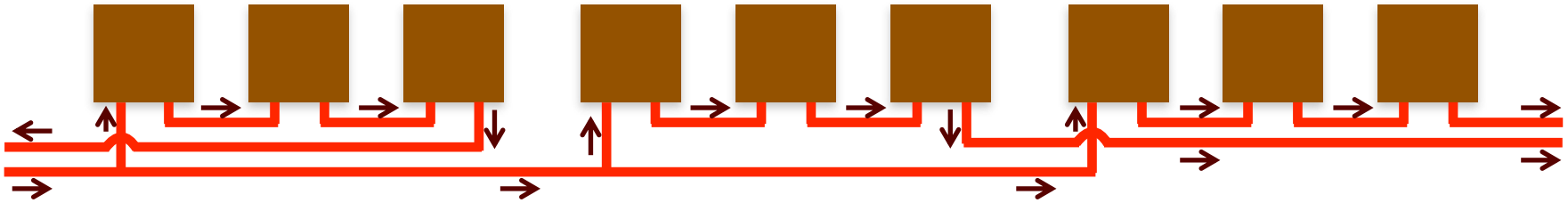
Sealed MRPC proposed for CBM-TOF



Sealed MRPC proposed for SPD-TOF

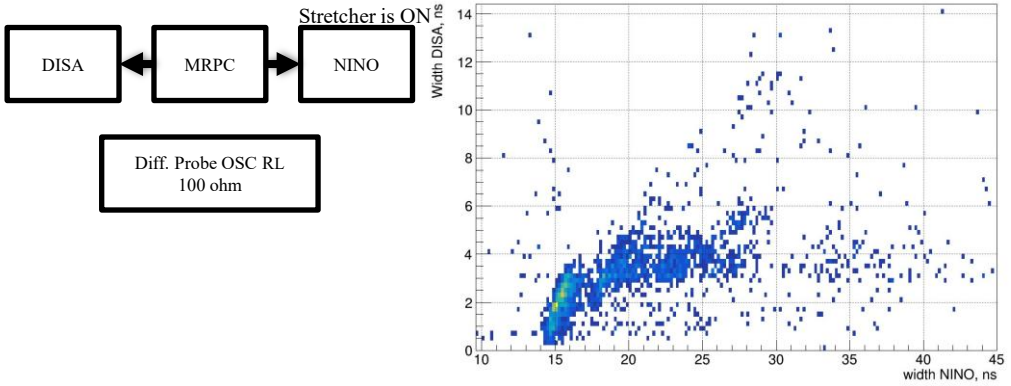


Serial gas connection of MRPCs in a single super module



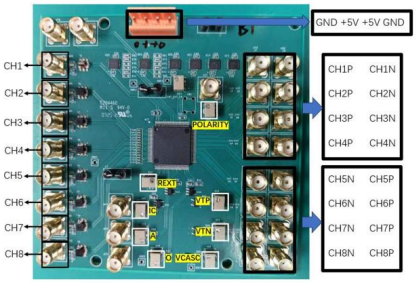
Time-of-flight (TOF) system

DISA to NINO comparison



Pulse width distribution FEE for one same strip MRPC

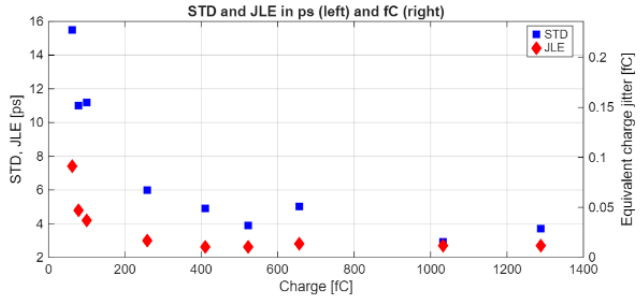
DISA evaluation board



DISA calibration and jitters

$$\Delta Q = \Delta t\ [ps] \times \frac{1}{A}\ [fC/ns] \times \frac{1\ ns}{1000\ ps} = \frac{\Delta t}{A \cdot 1000}\ [fC]$$





Impedance measurement for Protvino MRPC

