FRONT-END ELECTRONICS FOR TPC/MPD DETECTOR OF NICA PROJECT

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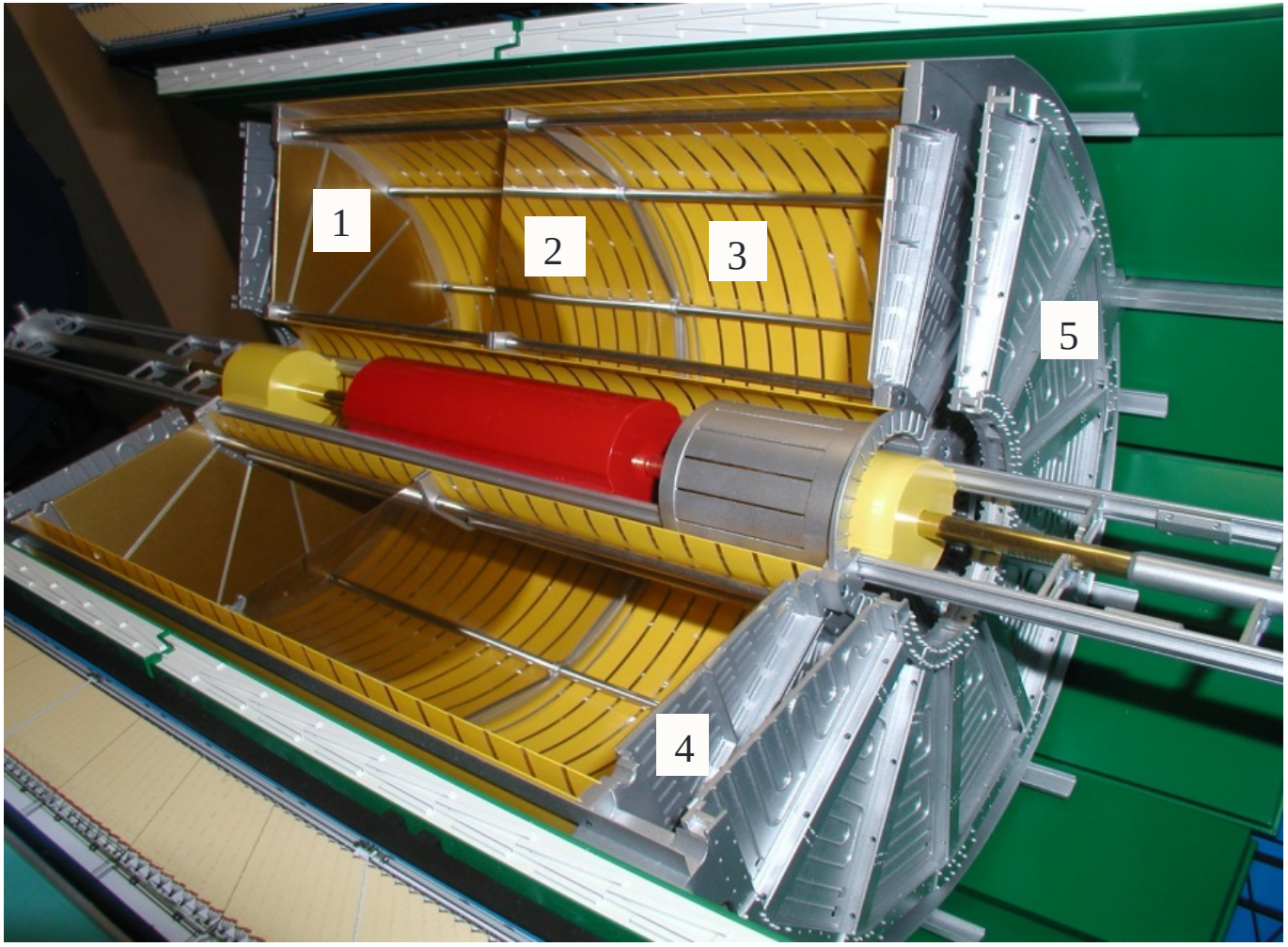
Central part of the MPD mock up with TPC cross-section



The TPC/MPD design requirements:

The overall acceptance: $\eta < 1.2$

The momentum resolution for charged particles is under 3% in the transverse momentum range $0.1 < pt < 1$ GeV/c

Two-track resolution of about 1 cm

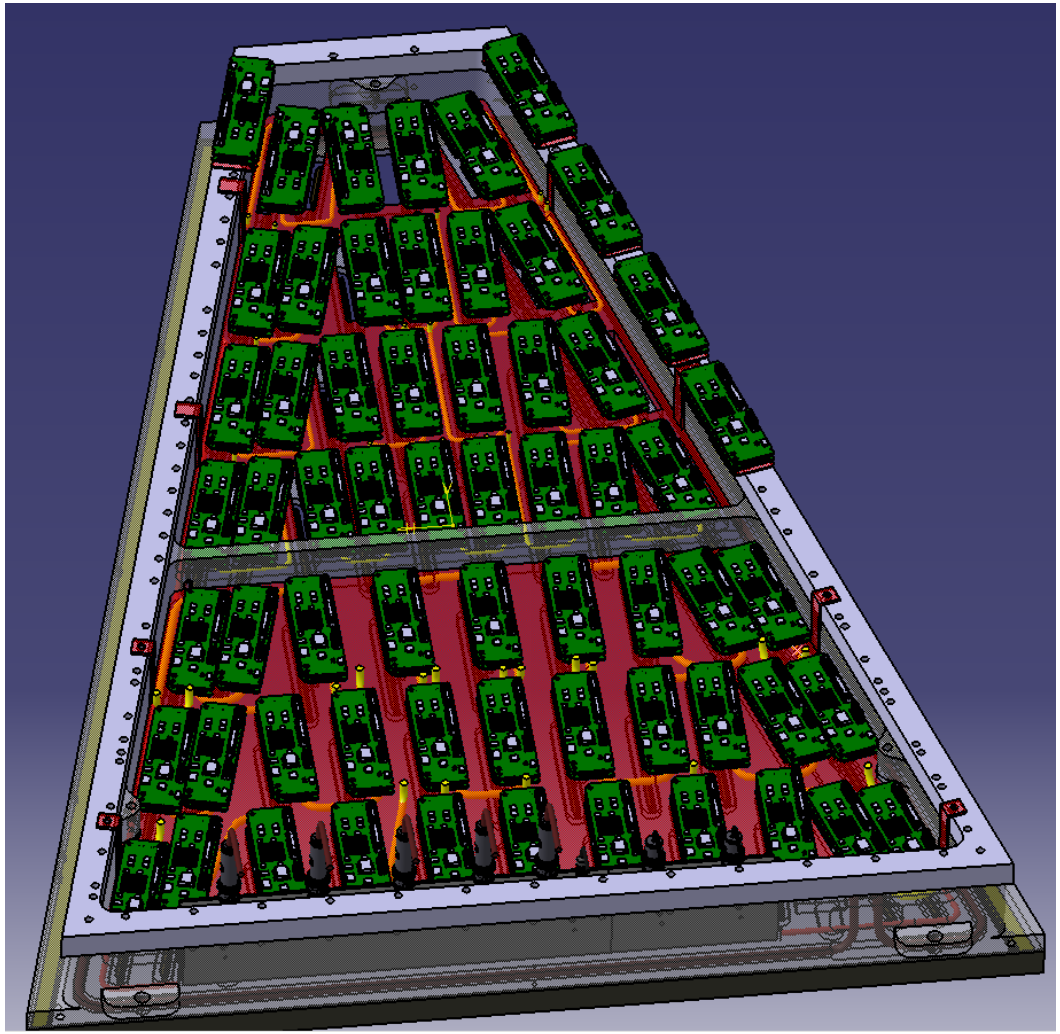
Hadron and lepton identification by dE/dx measurements with a resolution better than 8%

Data flow rate up to 100 GBps at trigger rate 7 KHz

1- MWPC;
2 - HV electrode;
3 - Field cage;
4 - FEE position;
5 - End cap thermal screen.

Concept of electronics integration for ROC

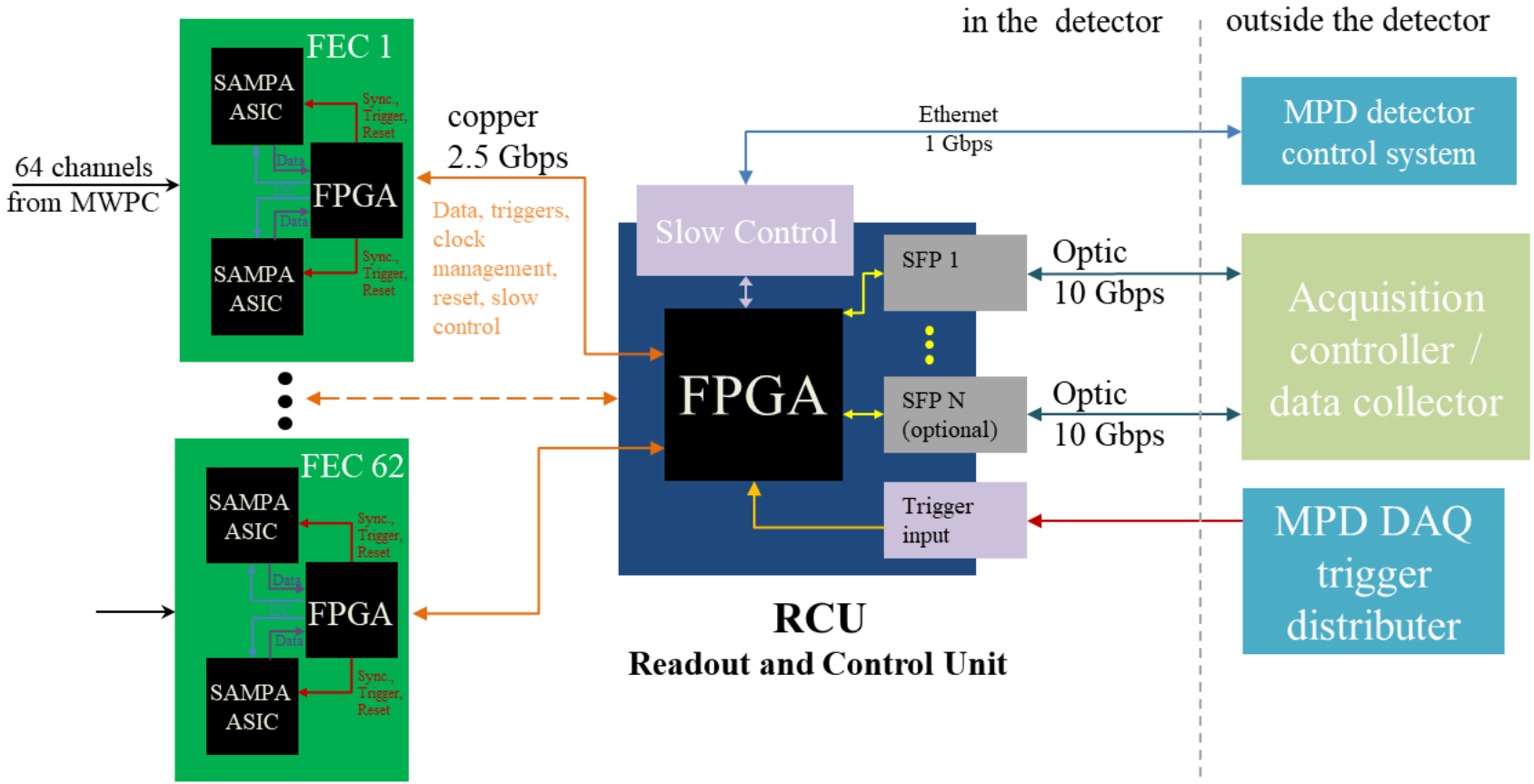
The necessity not only to reduce the amount of material at the TPC endcaps, but also to distribute it evenly, has forced the group to develop a card from two boards.



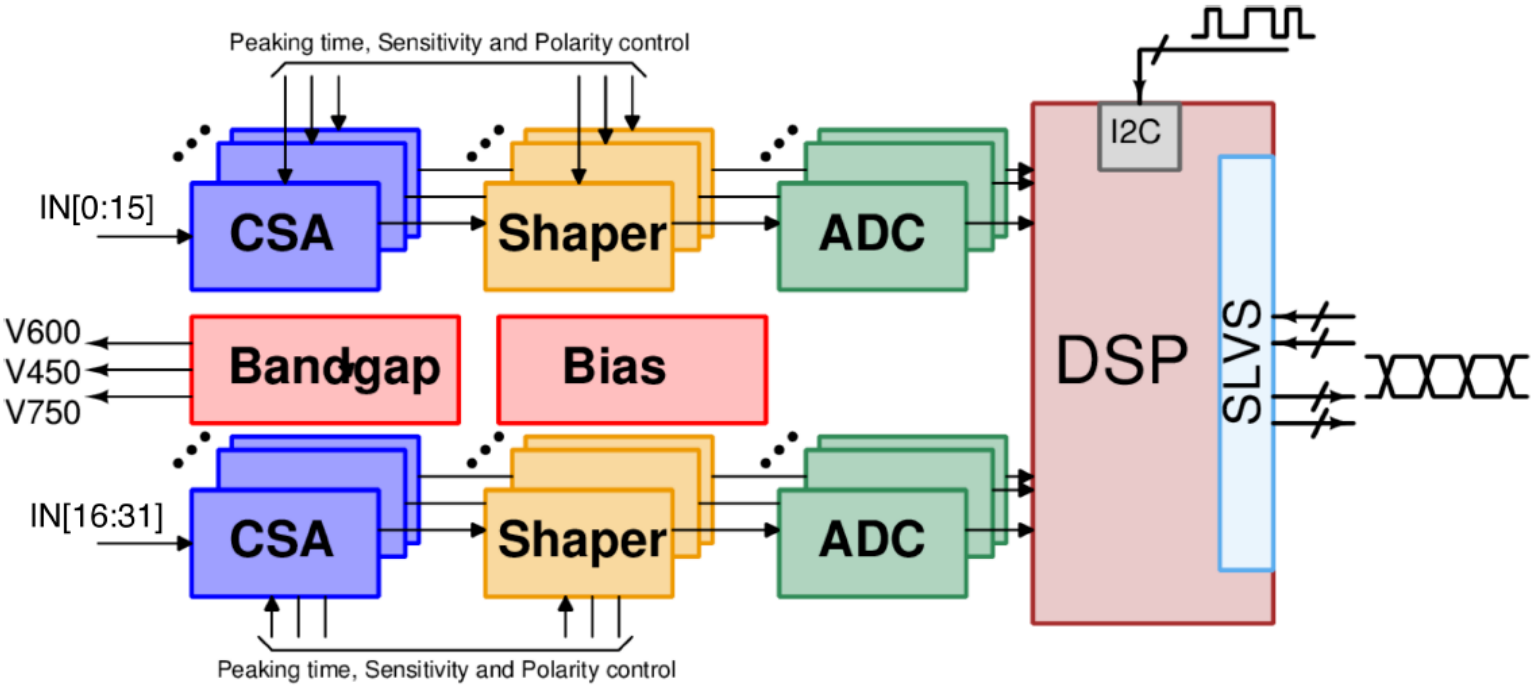
FEE status

- Concept of the TPC data readout system was determined.
- Actual size FEC (28x91 mm^2)satisfying integration demands was designed, limited number of FECs produced and tested.
- FECs testing with readout controller prototype based on Arria 10 GX FPGA on the way.

Block diagram of one chamber readout

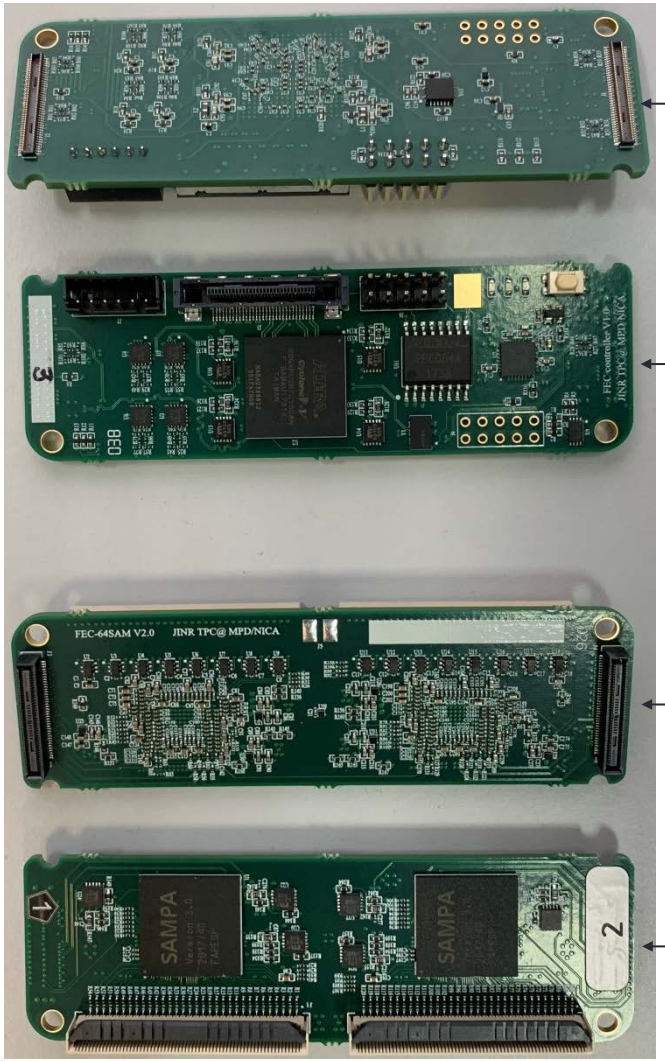


SAMPA chip: the core of FEE



[1] J. Adolfsson, et al., SAMPA chip: the new 32 channels ASIC for the ALICE TPC and MCH upgrades, JINST 12 (04) (2017) C04008.

FEC view



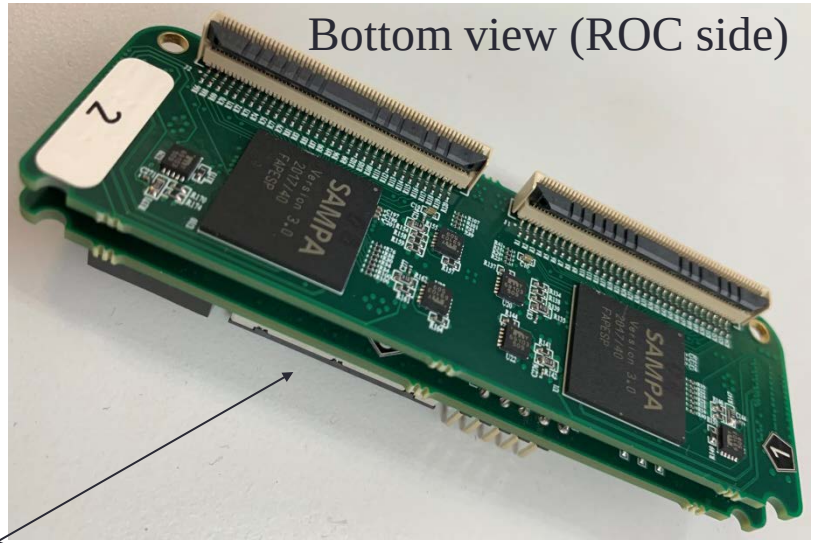
FEC controller
Bottom view

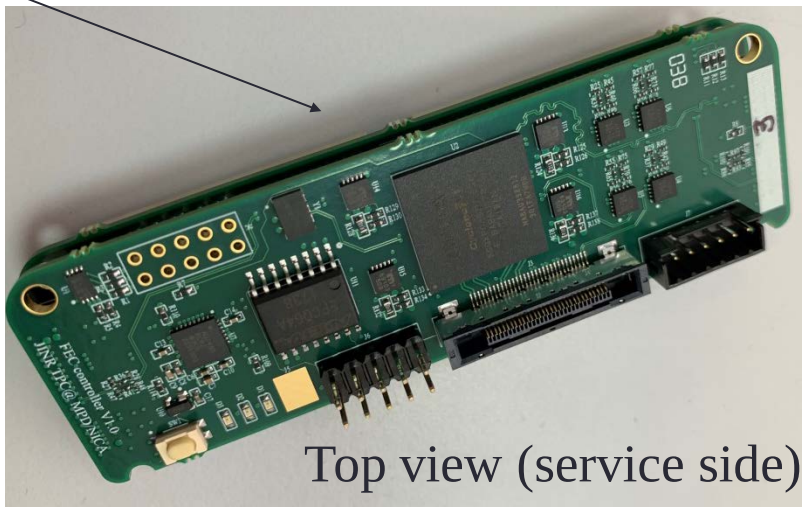
FEC controller
Top view

FEC assembly
view

SAMPA FEC
Top view

SAMPA FEC
Bottom view





FEC main parameters and functionality:

- The total number of registration channels: 64
- Input signal dynam. range: 100 fC
- ADC resolution: 10 bit
- ENC: less than 1000e^-
- SAMPA chips configured and controlled via FPGA
- Readout serial interface: up to 2.5 Gbps

➢ *Double-board FEC provides opportunities for possible upgrade of the card readout.*

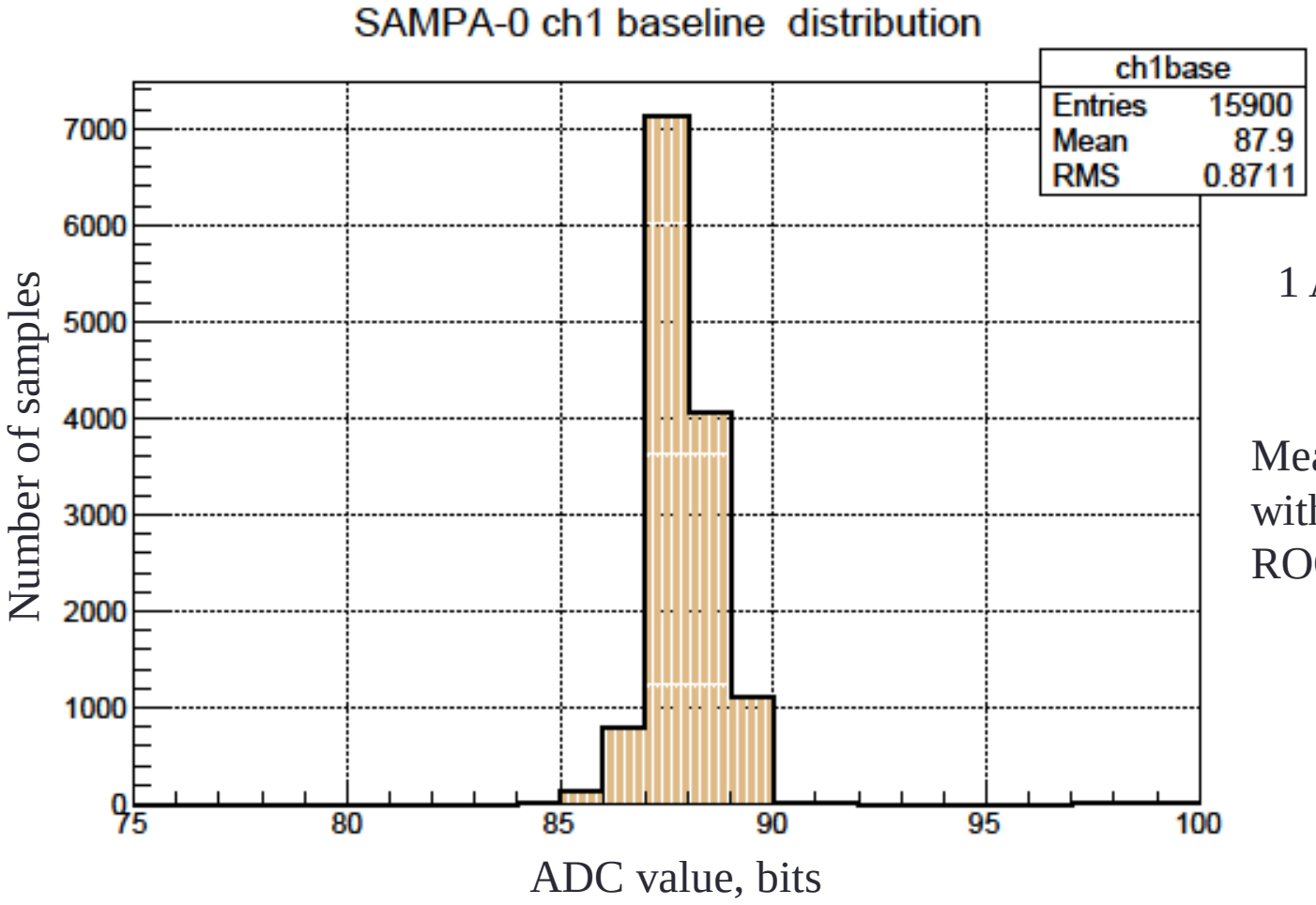
➢ *Transfer of data and trigger signals was realized with the same high-speed serial interface.*

➢ *16 values of currents, voltages and board temperatures are controlled with ADC.*

➢ *External circuit and embedded protection functionality against SEU are provided.*

➢ *Remote system update for FEC firmware was provided.*

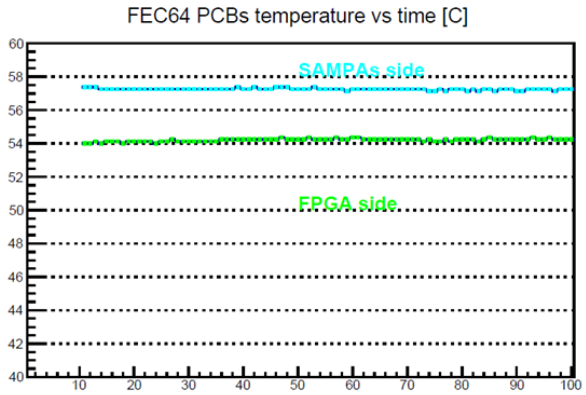
Typical noise distribution of a SAMPA channel

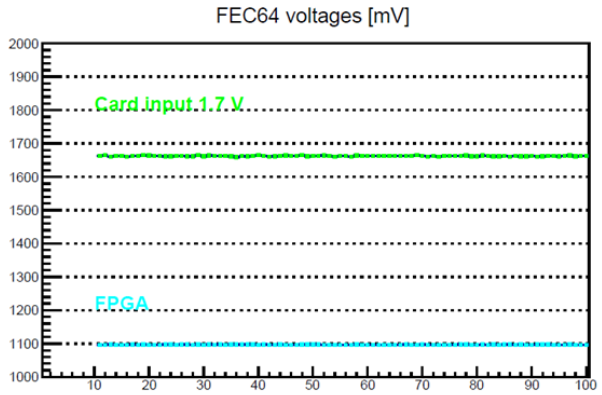


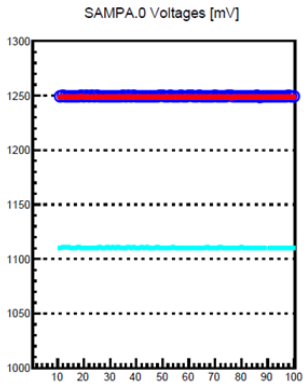
1 ADC LSB = 670 e^-

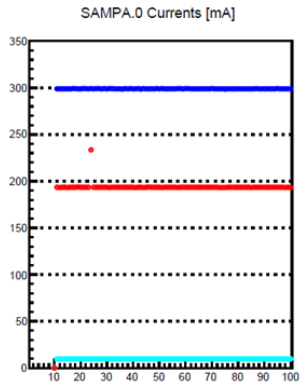
Measurement was done without connection with ROC

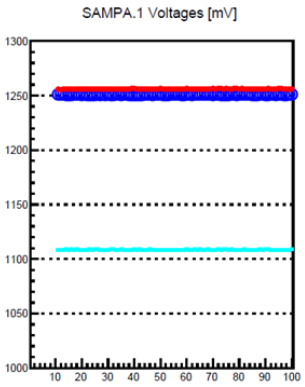
FEC slow control data

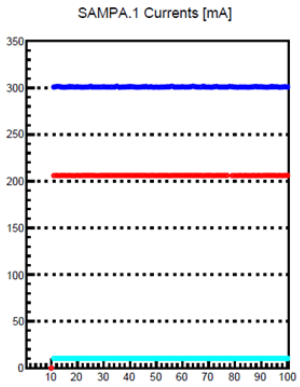






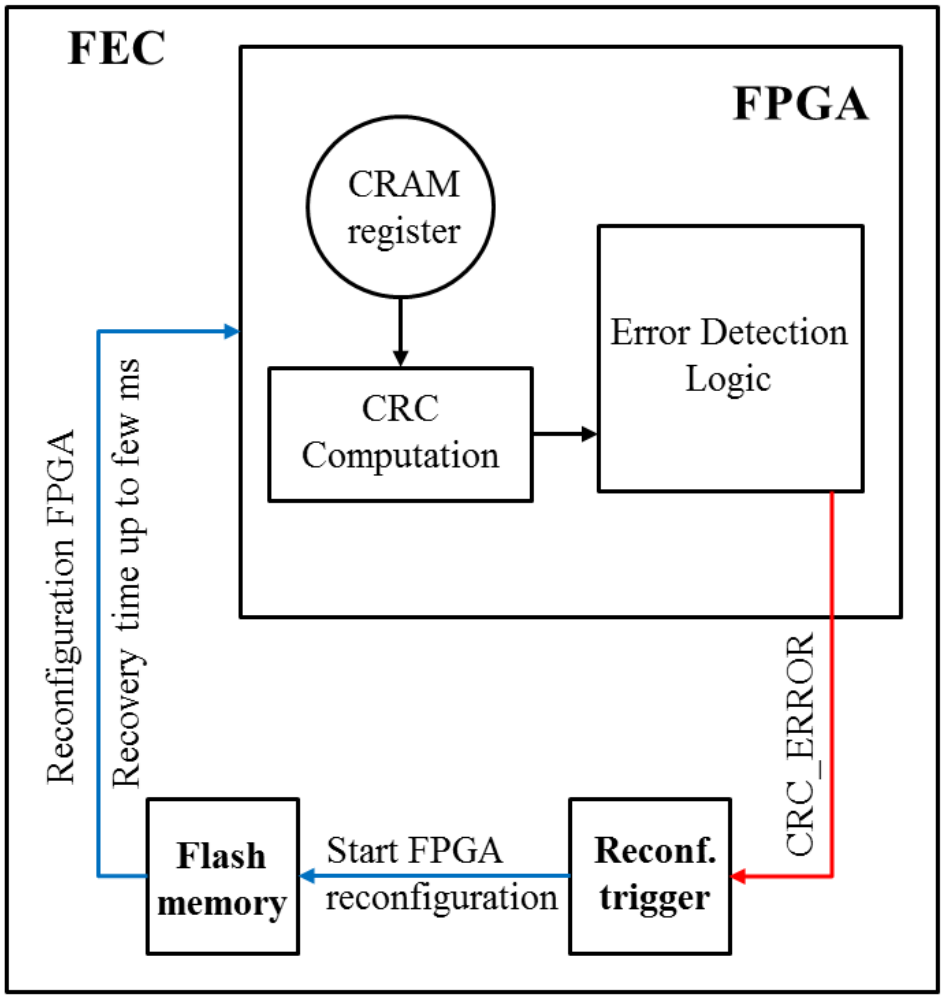






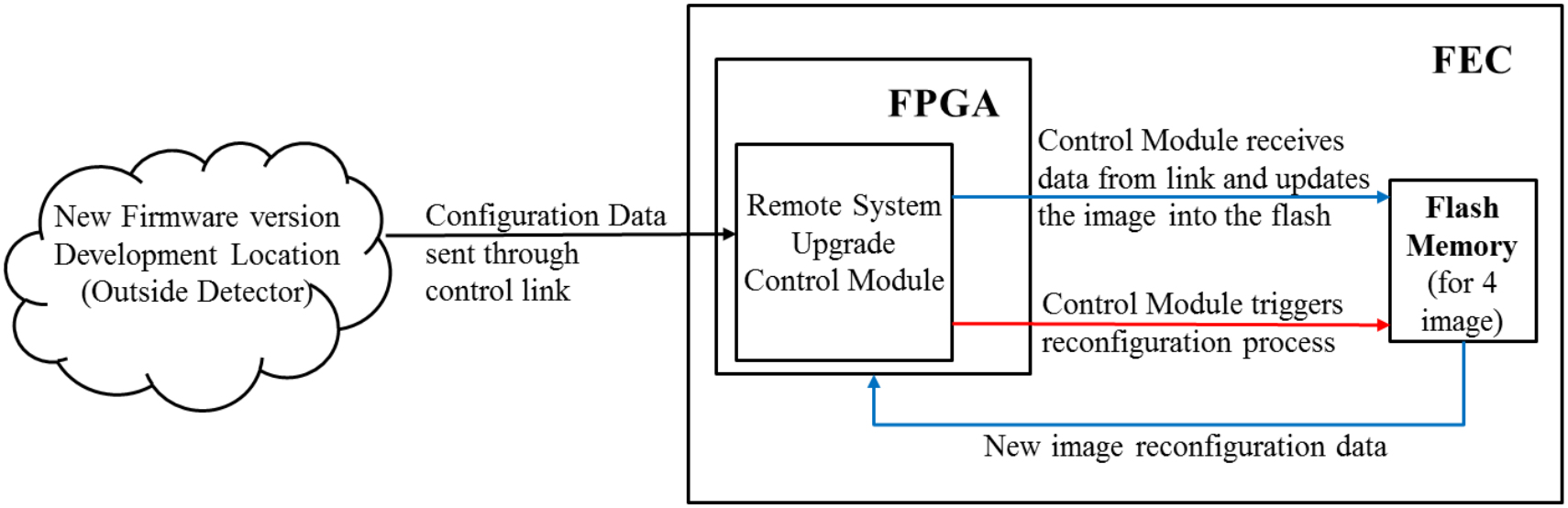
16 values of voltages, currents and temperatures are continuously measured on each FEC. The FPGA control state machine processes the data of the control ADC and, in case of problems, forms an interrupt vector.

SEU recovery circuitry



- Due to the FECs operation in a radiation environment, it is reasonable to have mechanisms to protect the FPGA firmware from SEU.
- The CRC circuit can detect all single-bit and multi-bit errors within the FPGA configuration memory.
- In case of detecting a firmware error, the onboard trigger initiates the reconfiguration process from the external flash memory.

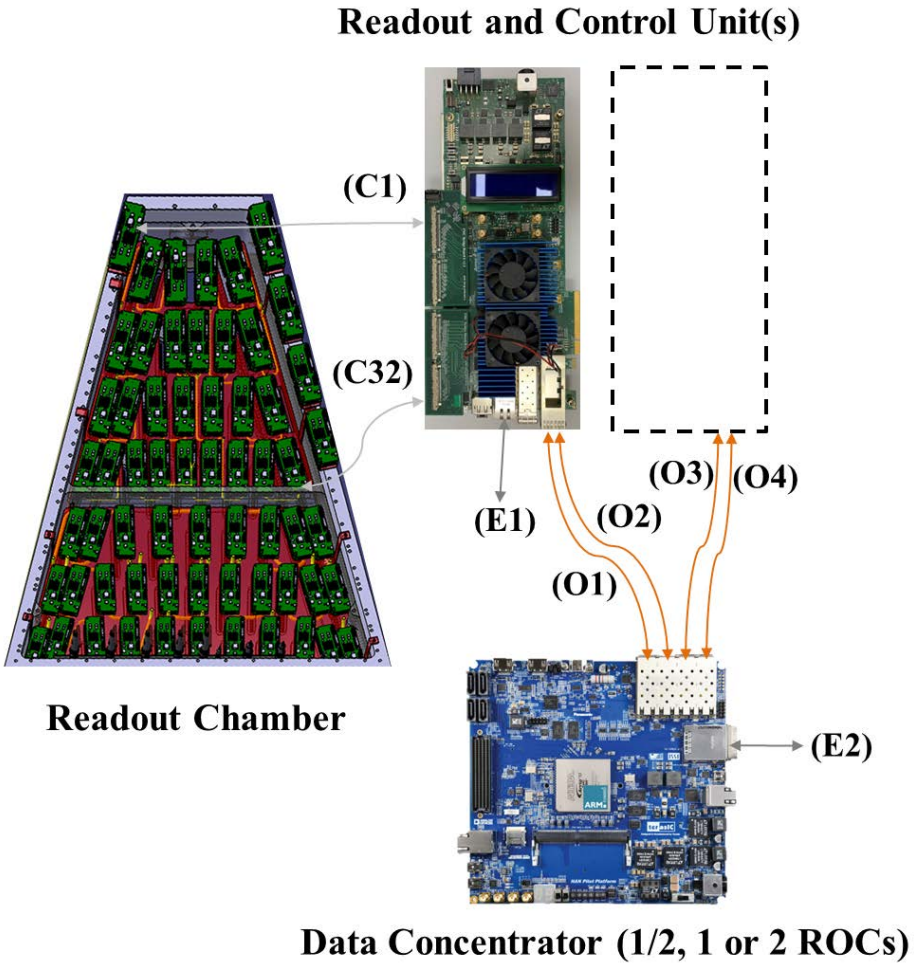
Remote firmware update



Anticipating limited access to the electronics installed on the detector, it is desirable to provide remote update of the firmware. Remote firmware upgrade feature was implemented into FPGA design of the FEC controller.

Towards multichannel readout

Half-ROC (2048 ch.) system



C1..C32: Micro-coaxial coper cables. Data, triggers, reset, slow control information. Up to 2.5 Gbps.
E1,E2: STP, Ethernet 1 Gbps. E1: to/from Detector control system; E2: for remote access to embedded Linux.
O1-O4: SFP optical cables. Up to 10 Gbps. O1,O2: from/to RCU1; O3,O4: from/to RCU2.

Features of A10GX – readout system core

Flow Summary

<<Filter>>

Flow Status	Successful - Fri Sep 27 13:48:04 2019
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Pro Edition
Revision Name	top
Top-level Entity Name	top
Family	Arria 10
Device	10AX115S2F45I1SG
Timing Models	Final
Logic utilization (in ALMs)	22,658 / 427,200 (5 %)
Total registers	44746
Total pins	178 / 960 (19 %)
Total virtual pins	0
Total block memory bits	29,797,388 / 55,562,240 (54 %)
Total DSP Blocks	3 / 1,518 (< 1 %)
Total HSSI RX channels	34 / 72 (47 %)
Total HSSI TX channels	34 / 72 (47 %)
Total PLLs	44 / 144 (31 %)

Resources estimate for RCU design.

- Intel 20nm FPGA Arria 10 was selected as a base of data readout.
- 72 embedded transceivers is sufficient to implement the RCU on a single FPGA.
- ALMs and memory resources allow for the implementation of all the necessary data transfer system algorithms
- Excess FPGA resources allow further system improvement

Conclusion

- The FEE for the TPC was designed on base of the ASIC SAMPA and Intel FPGAs with high-speed serial links.
- The FECs form factor of 28x91mm^2 conforms to the detector design constraints.
- The design of the FEC provides opportunity for future upgrade.
- The readout system prototype is considered as a starting point for full-featured TPC readout system design.

Thank you!