FELIX: commissioning the new detector interface for the ATLAS trigger and readout system

27th Symposium on Nuclear Electronics and Computing (NEC 2019)

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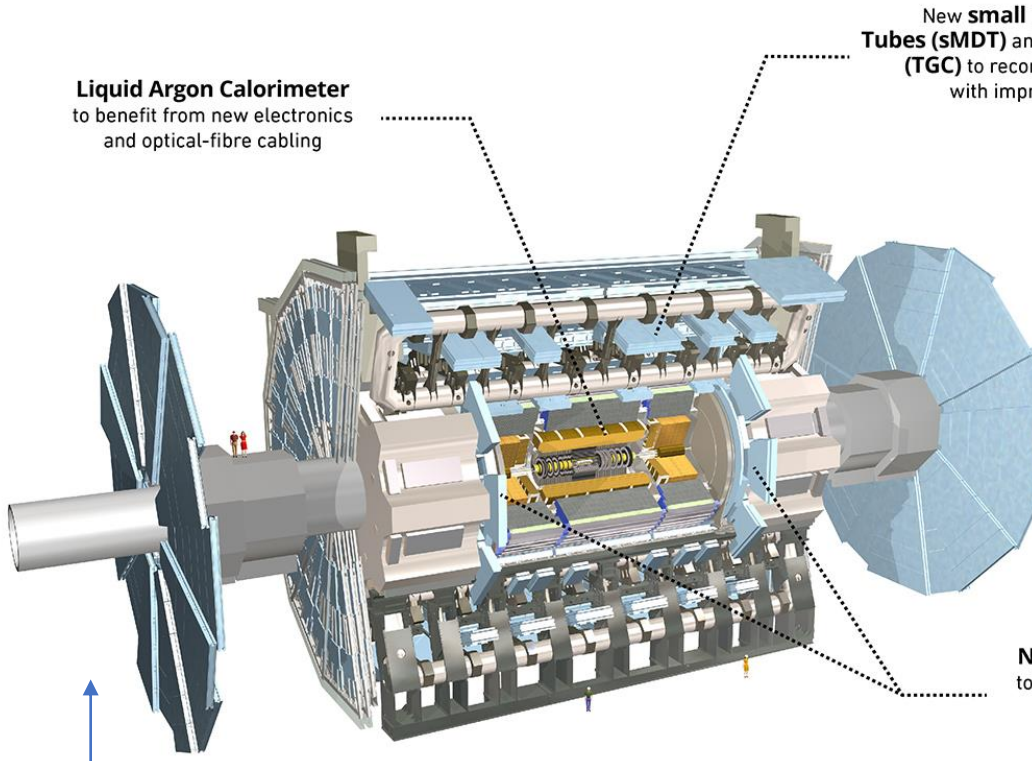
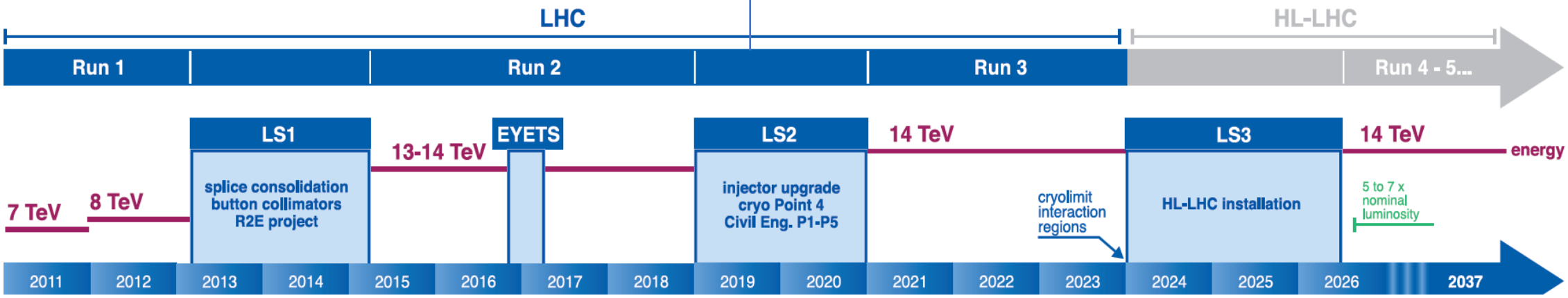
Outline

- Introduction
- FELIX Board Production
- FELIX Firmware
- FELIX Server & Software
- Software ROD/ROS
- Integration Tests
- Performance Studies
- Summary & Outlook

Introduction

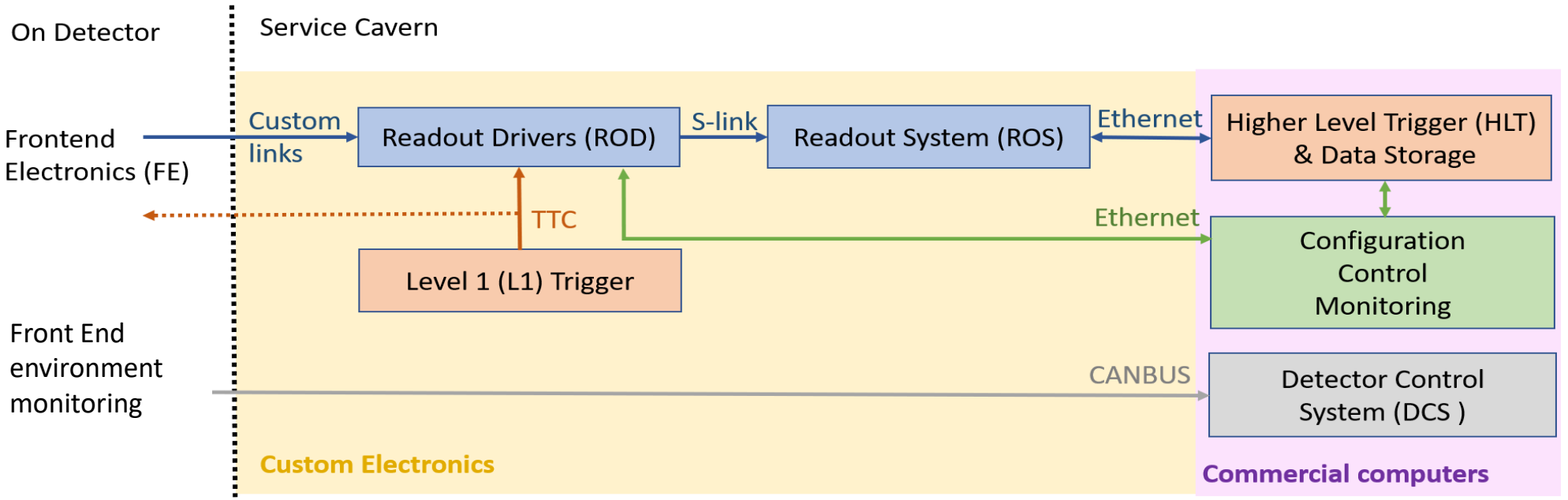




Phase I

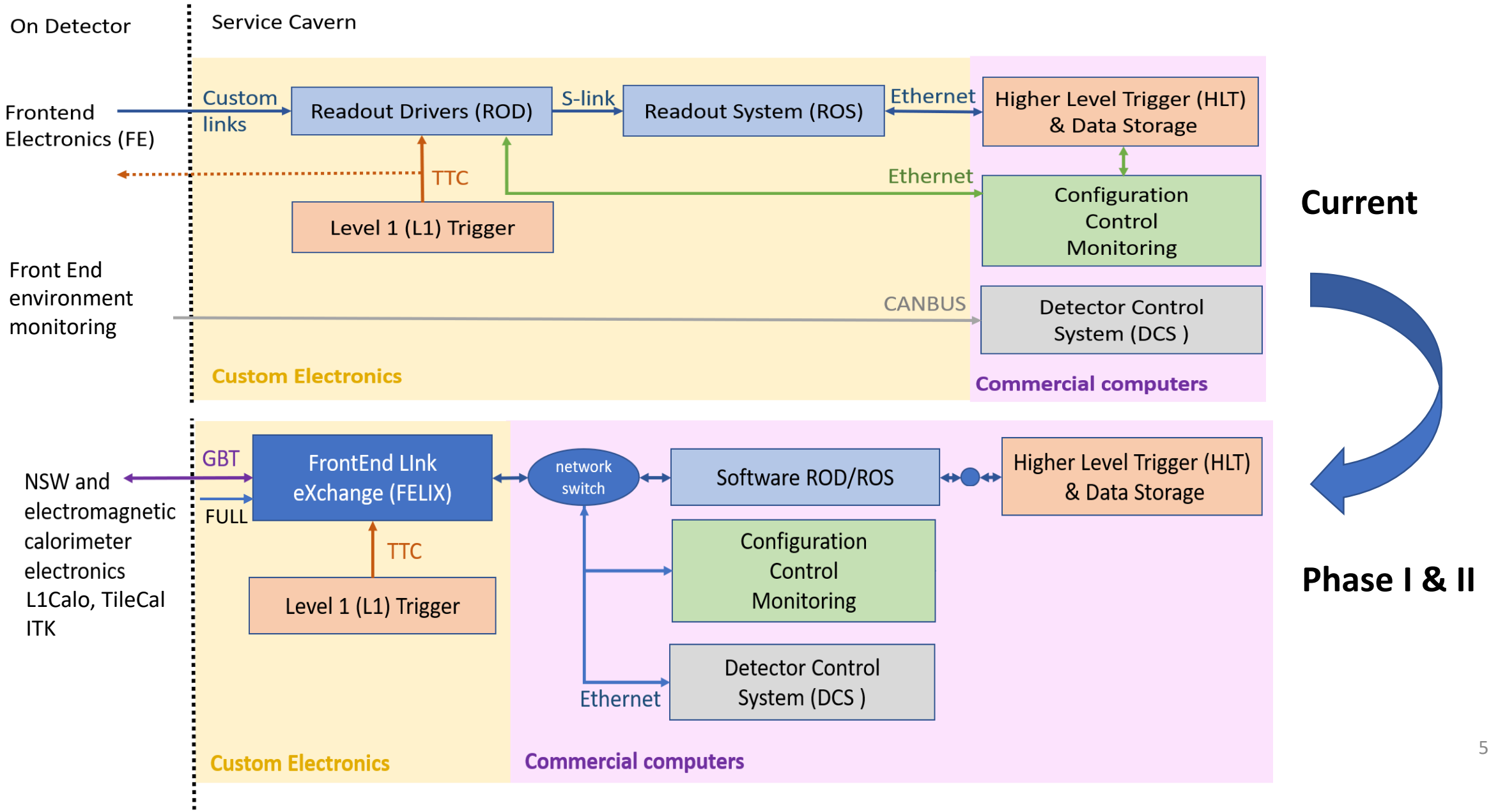
Phase II

Introduction

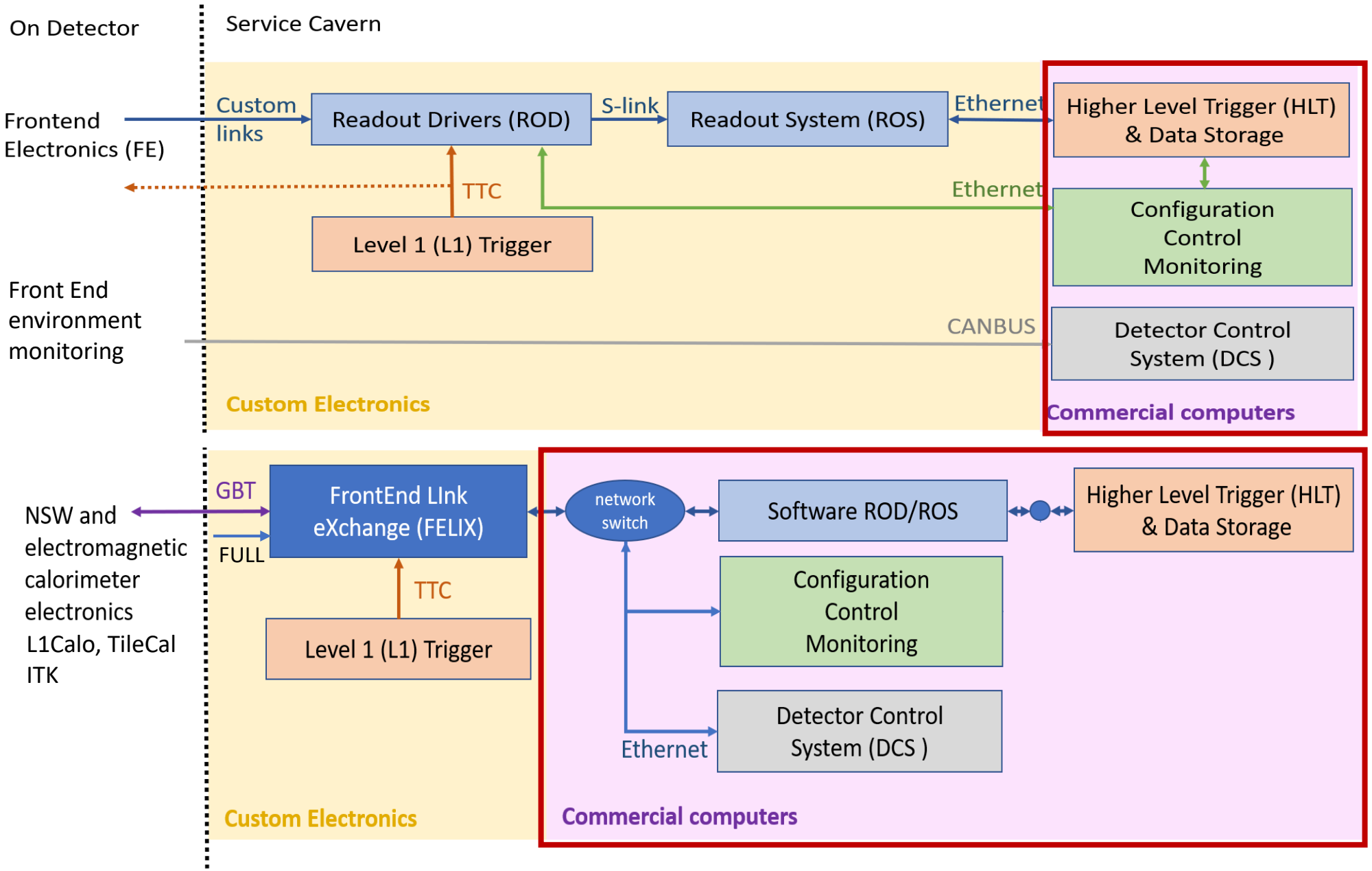


Current

Introduction



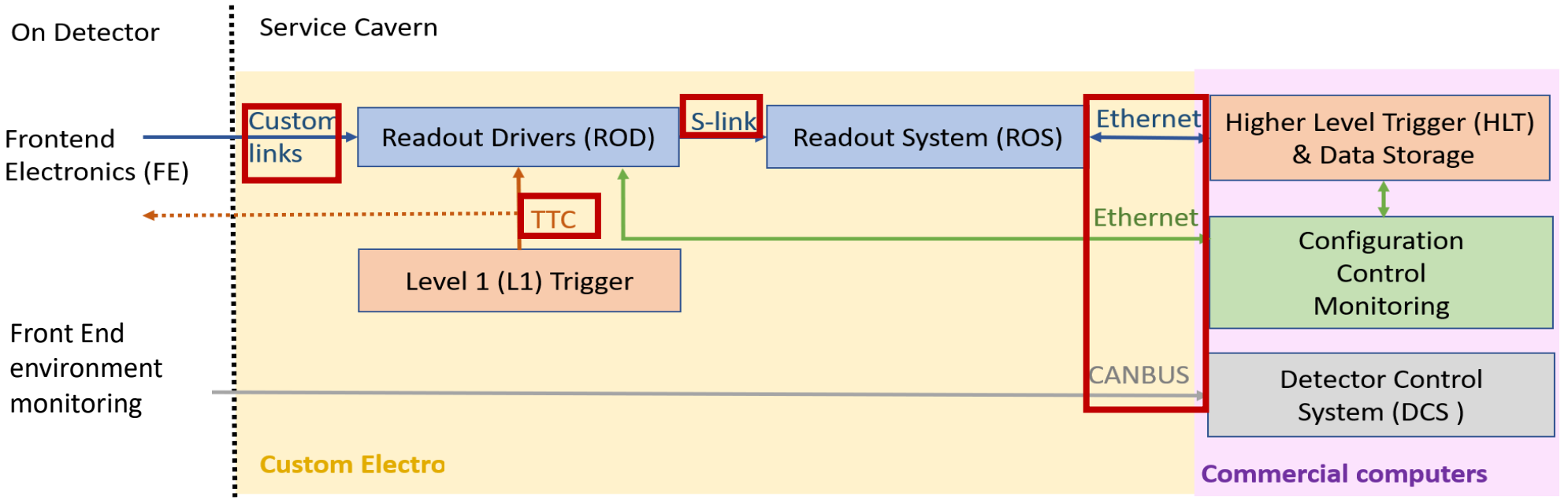
Introduction

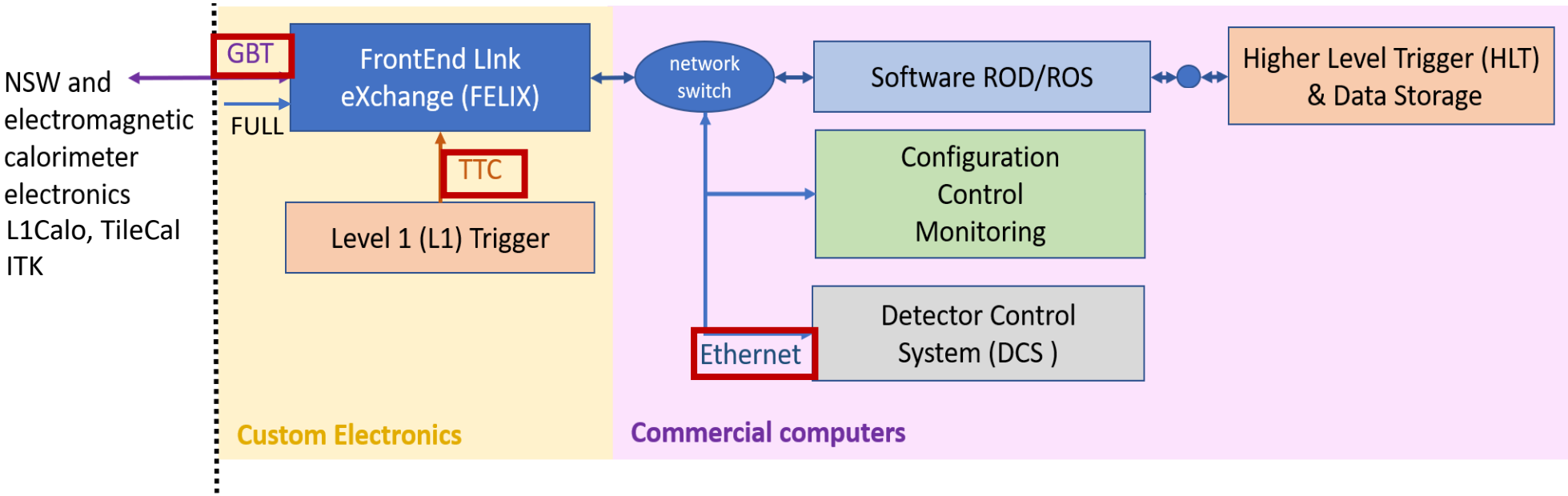


Move to more commercially available components sooner in readout chain

The custom readout drivers become software on commercial PCs ("data handlers" in Phase II)

Introduction

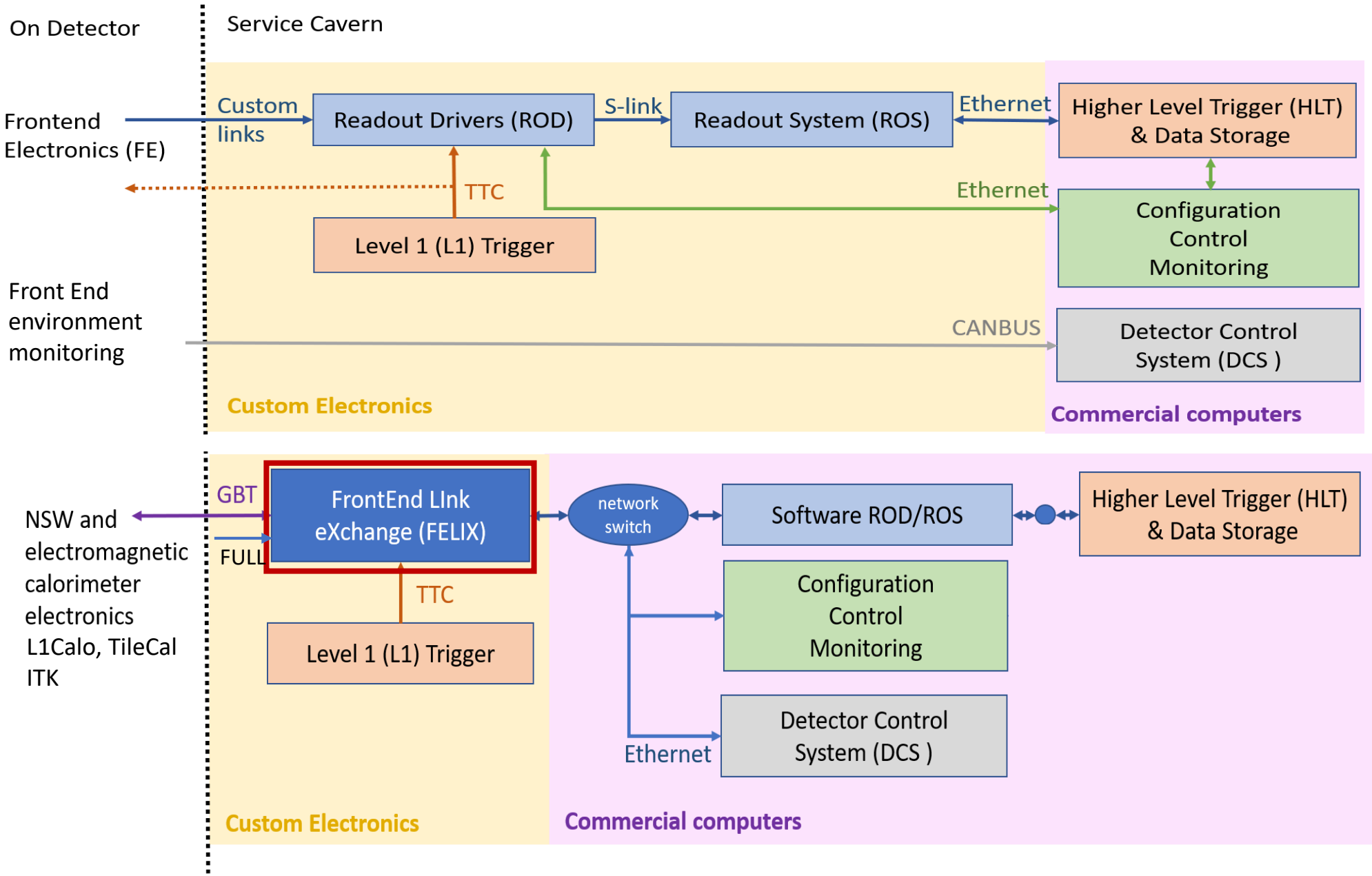




Reduces number of custom links needed to transmit data and timing signal, configure & control detector

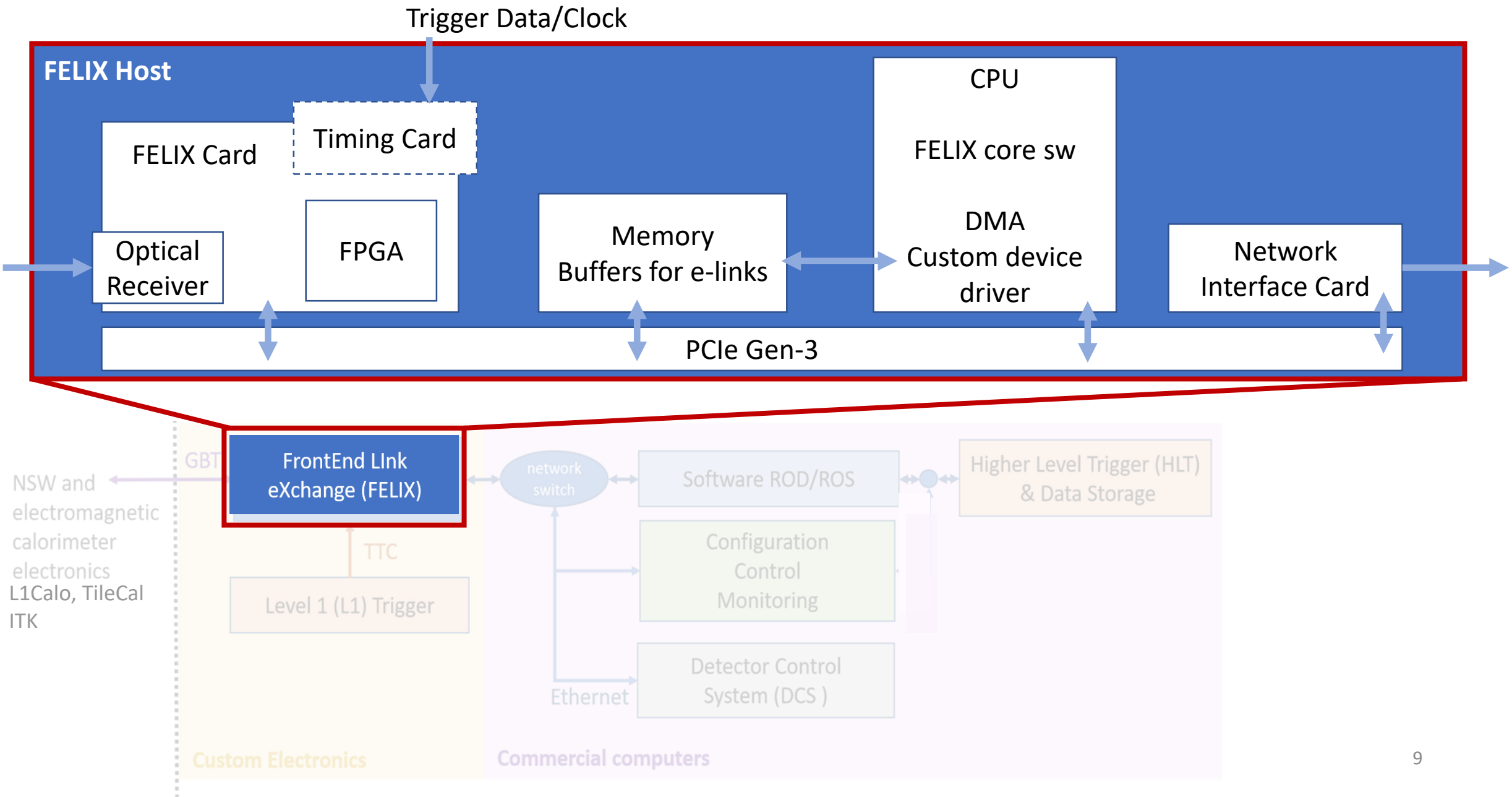
GBT (Gigabit transceiver): GBTx ASIC aggregates slow electrical links (E-links) from front end ASICs into fast optical link. Includes error correction for high radiation environment

Introduction

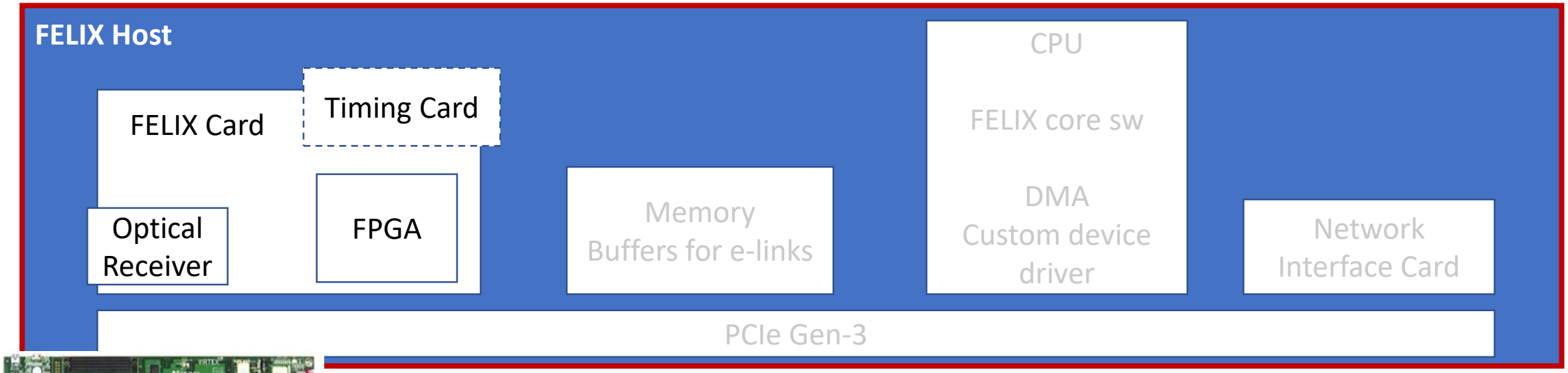


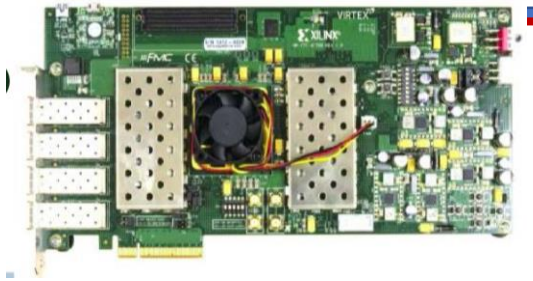
FELIX is always running, doesn't touch the data format, doesn't know about the status of the detector (like a switch that routes different data types)

Introduction



FELIX Board Production





FLX-709 (VC 709):
4 10 Gbps links (4 SFP+)
Virtex-7 X690T FPGA
PCIe Gen 3x8 lanes

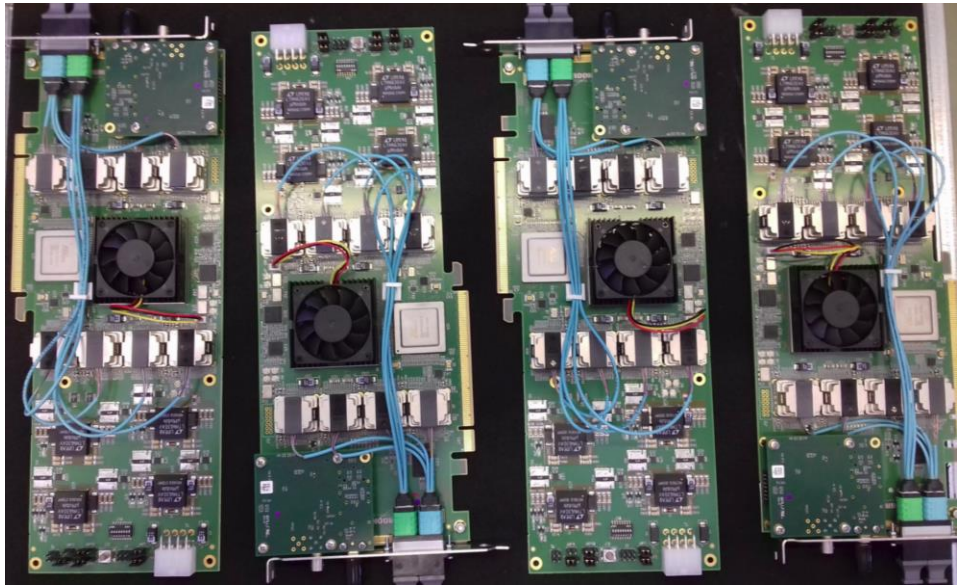
BNL 712:
Kintex Ultrascale FPGA
PCIe Gen 3x16 lanes
8 minipods

24 **4.8G** GBTx links,
12 **9.6G** links at PCIe limit
48 links as a TTC distributer

FELIX Board Production

FELIX Pre-series

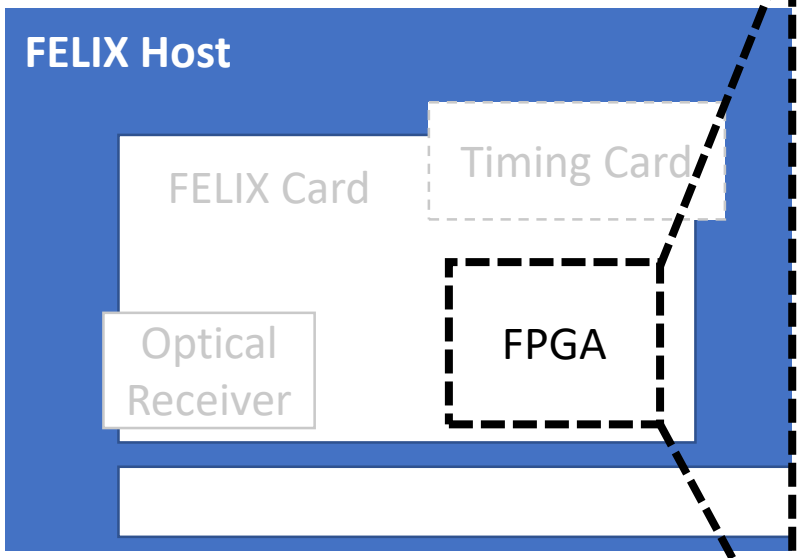
- Validated pre-series production of 23 FLX-712
  - 2 thermal cycles at 85 C, xray check of soldering, check voltage values
  - FPGA, FLASH and microcontroller programming, eyescans ($< 10^{-9}$) and BER ($< 10^{-12}$), functionality tests, 8 hour loop back tests, slow control adapter tests, trigger & timing tests, BUSY tests, jitter tests
  - Thermal testing on 8 cards to test 5 year lifetime = 50 cycles – passed functionality tests
  - ALL CARDS PASSED TESTS



FELIX Mass production for Phase I

- Launching production of 120 cards. Production in Fall and installation by mid-December

FELIX Firmware

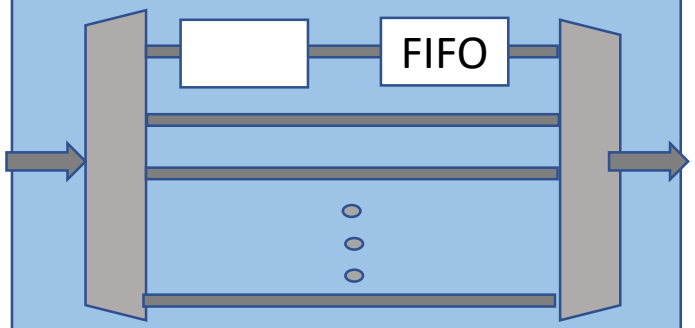


TTC & BUSY:
Decode trigger data and recover LHC clock

GBT Wrapper:
Send/receive GBT Data

Central Router: Map GBT data to E-link format

Demultiplex GBT link into data streams, decode data stream (8b/10b or HDLC), form 1 kbyte blocks read by DMA

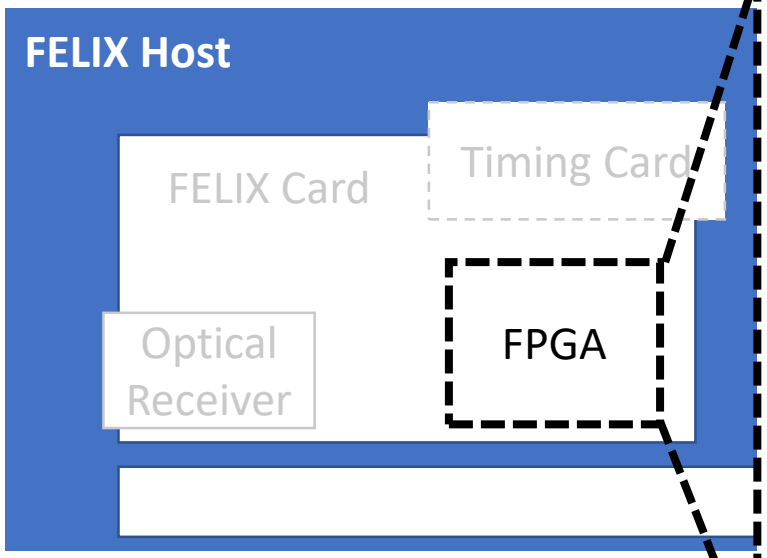


Wupper PCIe/ DMA Engine:
Push data to the memory

GBT Mode: 24 bi-directional radiation-hard, GBT links (4.8Gb/s – 3.2Gb/s with error correction)

FULL Mode: 12 links, custom light-weight protocol from front-end-path (9.6Gb/s – 7.68Gb/s with 8b/10b)

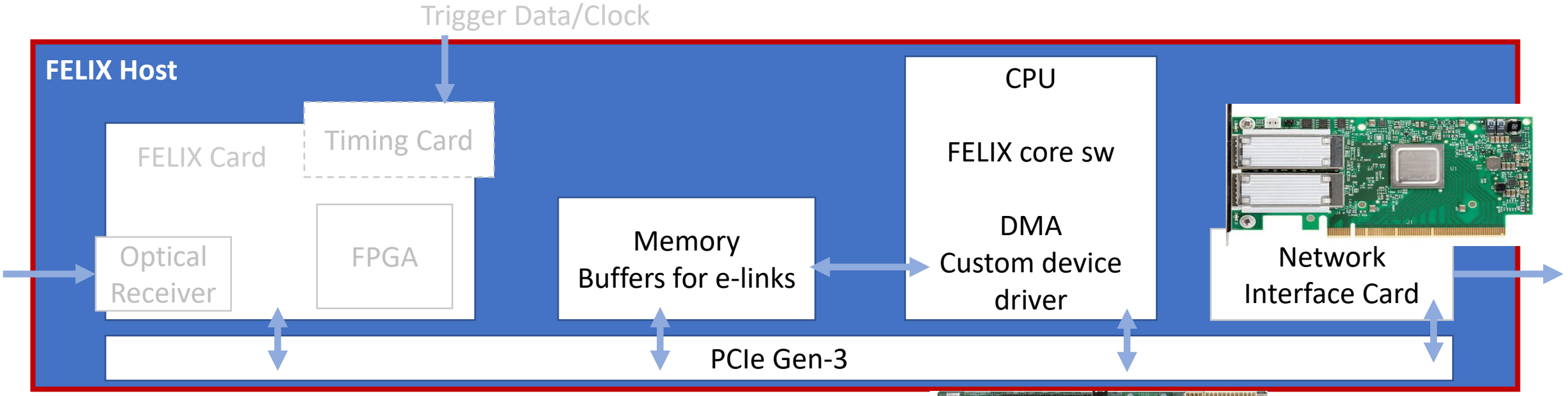
FELIX Firmware



	FLX-709 # chans	FLX-712 # chans
GBT dynamic - All combos of elinks (2,4,8) and modes (8b/10b, HDLC)	4	4+4
GBT semi-static - Static & configurable links	--	12+12
FULL - 6+6 channel matches maximum PCIe bandwidth (x16 Gen3). 12+12 channel is lower bandwidth	4	12+12
LTDB mode - Only clock distribution, trigger, slow control/monitor (to DCS)	--	24+24 (LTDB)

Name	Chunksize (worst case)	Rate per channel	Channels per FELIX (worst case)	Total Chunkrate per FELIX	Total Datarate per FELIX
GBT-Mode	40 Byte	100 kHz	384	38.4 MHz	15 Gbps
FULL-Mode	4800 Byte	100 kHz	12	1.2 MHz	46 Gbps

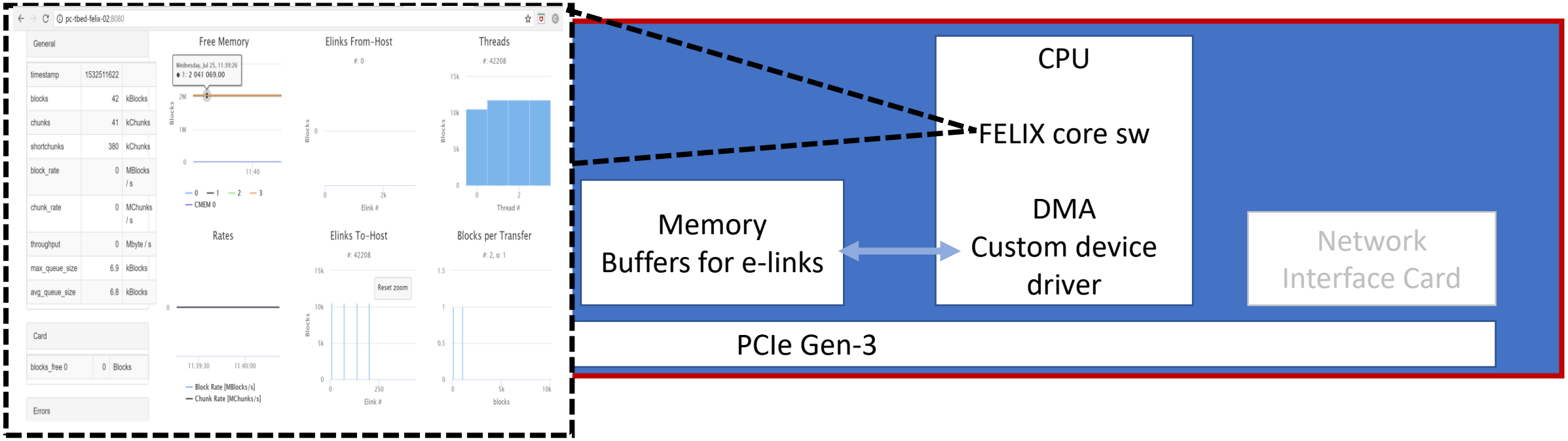
FELIX Server & Software



Component	Specification
Motherboard	Supermicro X10SRW-F
CPU	Intel(R) Xeon(R) CPU E5-1660 v4, 8 cores @ 3.20GHz *Intel Xeon Gold 5118 CPU (if more perf needed)*
Memory	32 GB (4x8GB DIMMs for full memory bandwidth) *48 GB (6x8GB DIMMs) (if more perf needed)*
Network Cards	Dual-port 100/25 GbE Mellanox ConnectX-5 EN

FELIX PC from Action (Poland) will be ordered soon

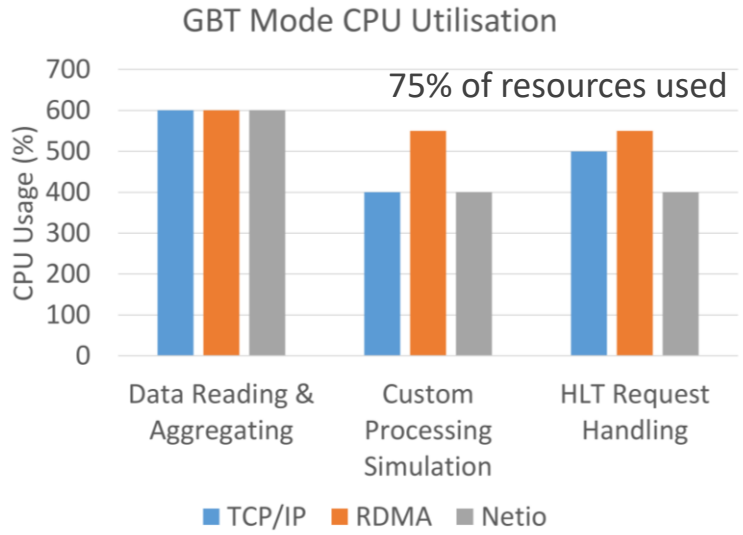
FELIX Software



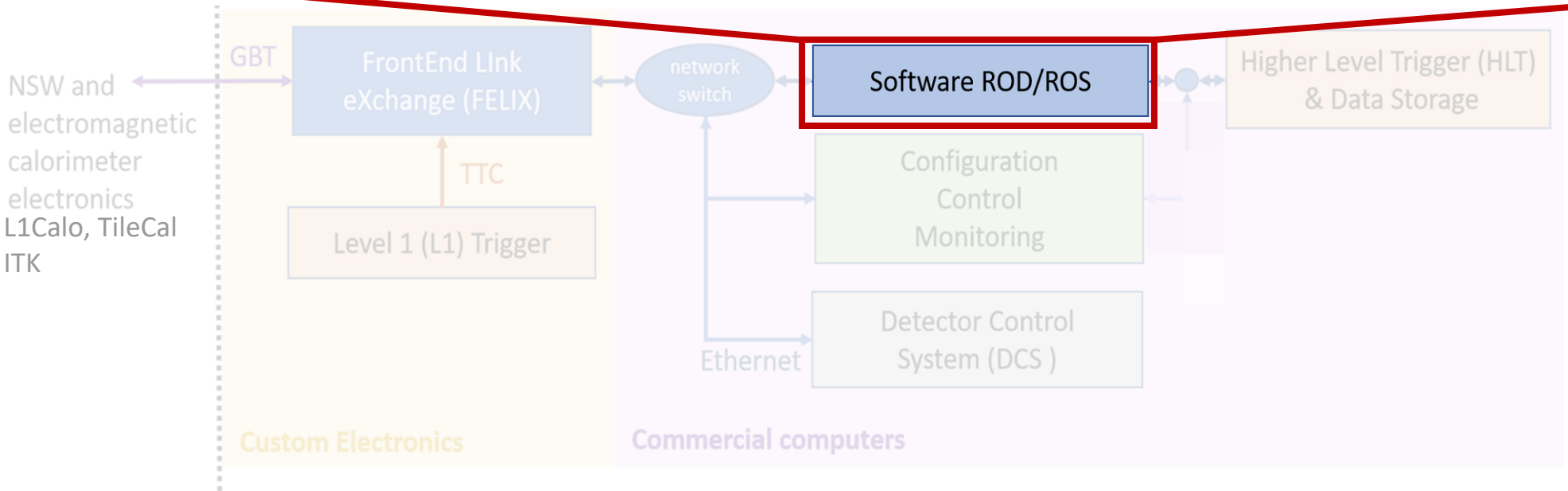
- Access to the FELIX hardware controlled via device drivers
- Low Level software: basic configuration/monitoring (electrical link configuration, felix-monitoring)
- Higher Level Software: data rate and channel monitoring
- Subscription to electrical links is made from SW ROD

Software ROD/ROS

Validated specifications depending on user needs

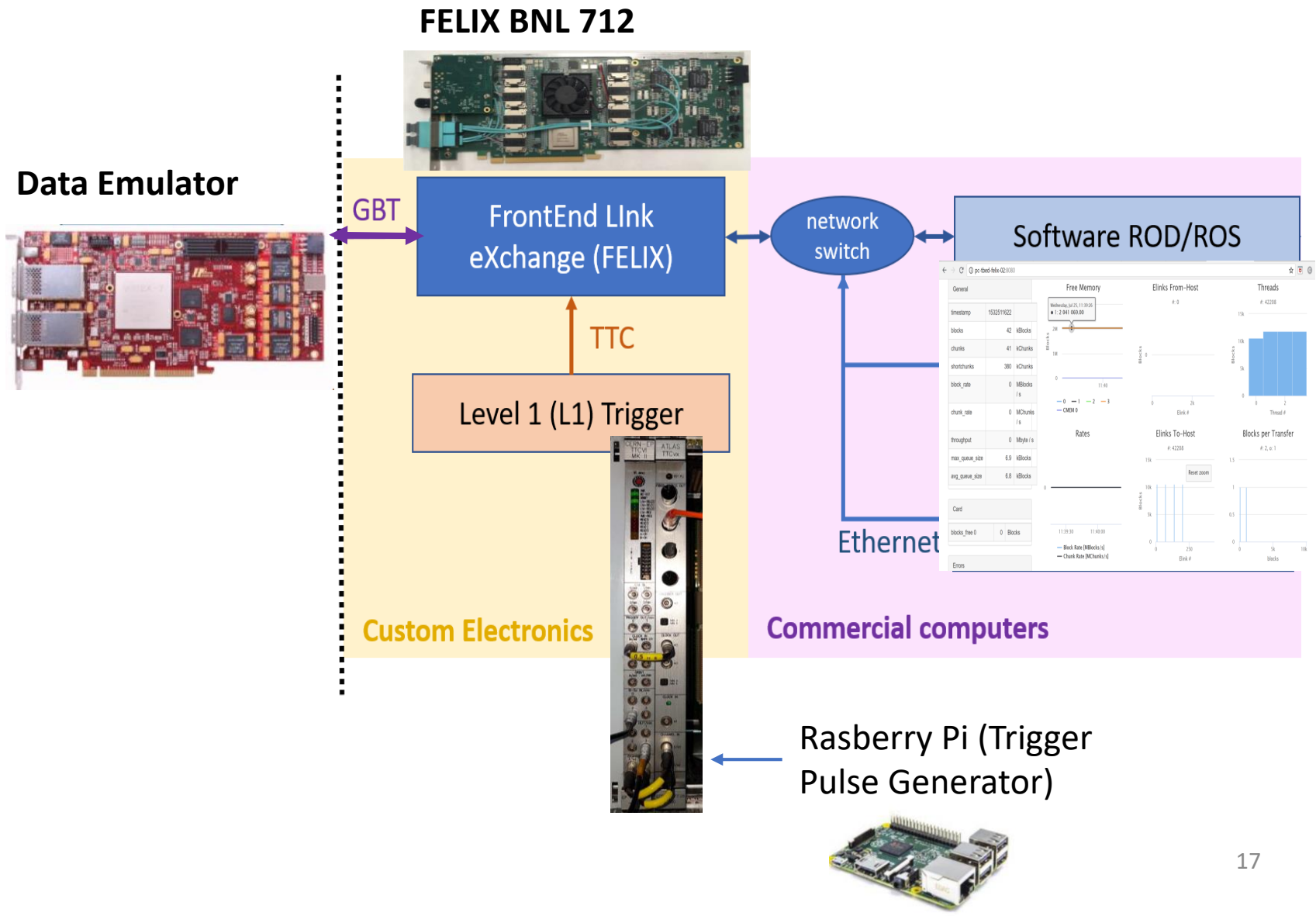


Component	Specification
Motherboard	Supermicro X10SRW-F
CPU	Dual Intel(R) Gold 5218 CPU @ 2.30 GHz (16 cores)
Memory	96 GB ECC REG DDR4-2666
Network Cards	Mellanox MT27700/MT27800

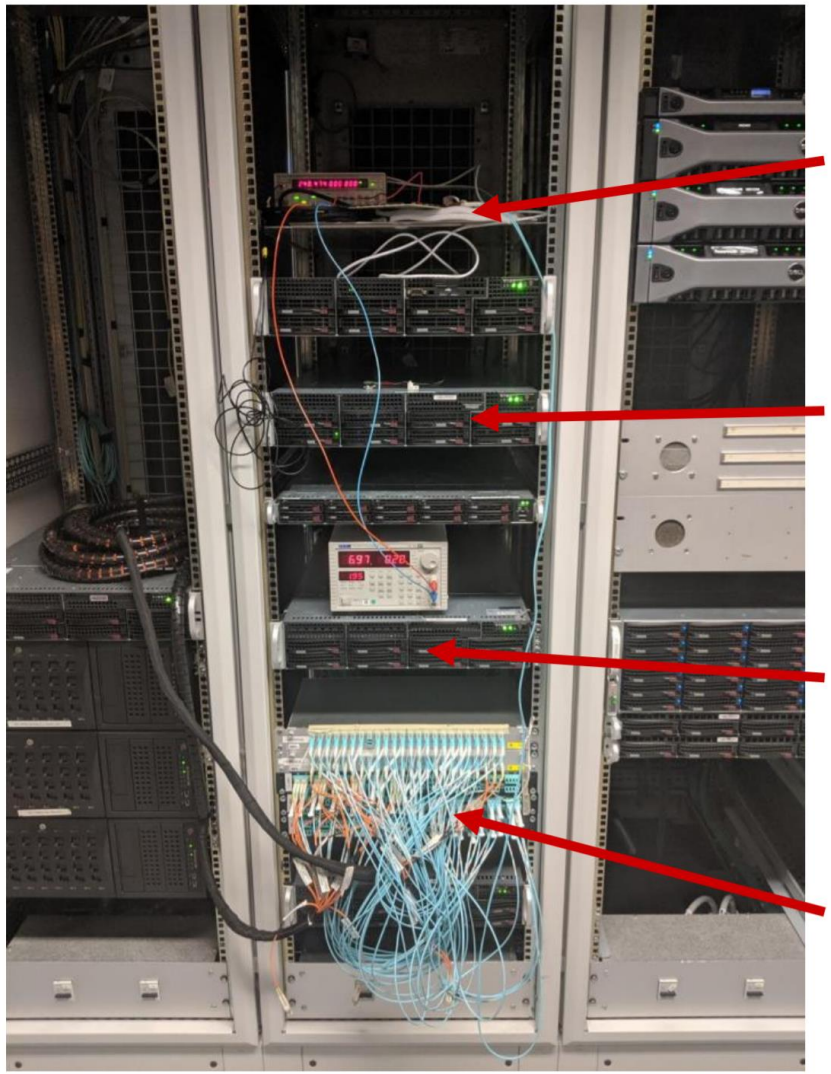


Integration Tests

- Integration of all supporting systems in Laboratory with emulated FULL and GBT mode data
- Commissioning with different input of trigger & timing & testing back pressure



Integration Tests

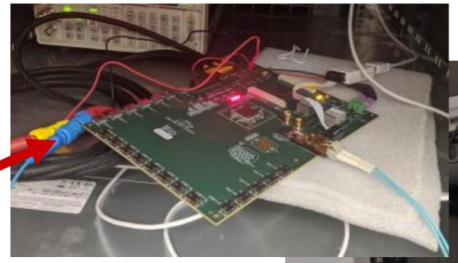


VLDB

FELIG Data Generator

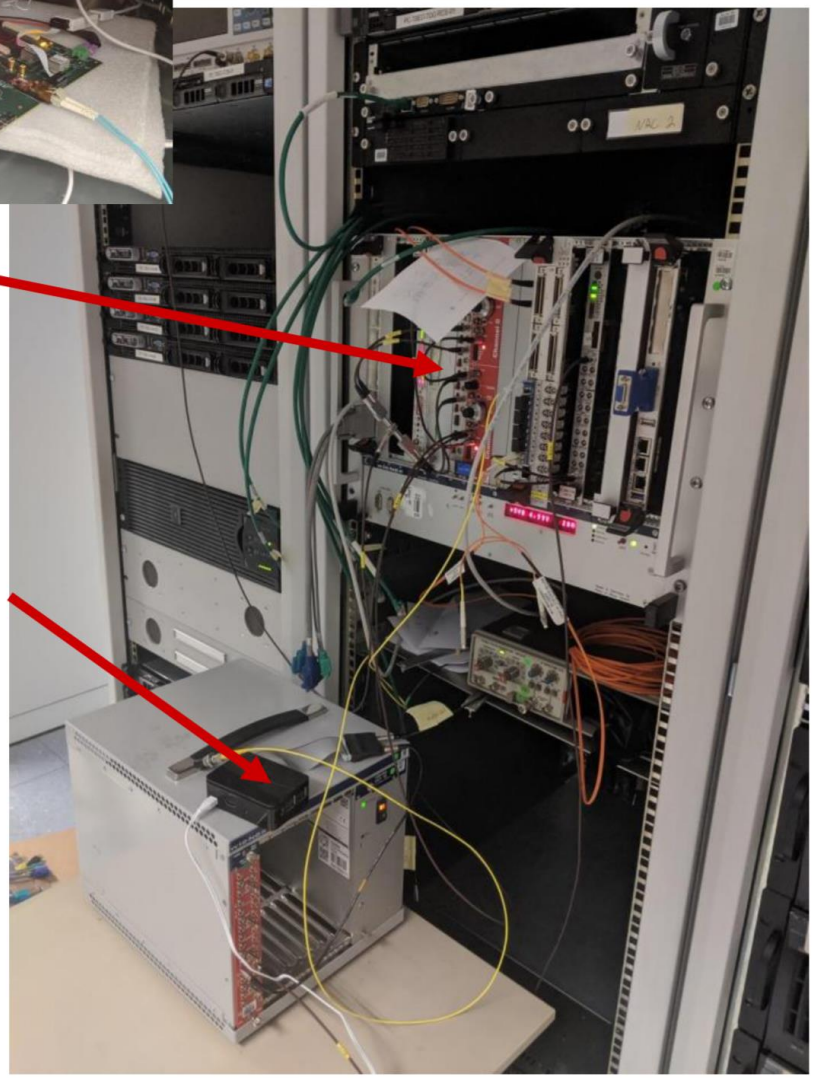
FELIX

Patch panels



TTC Crate

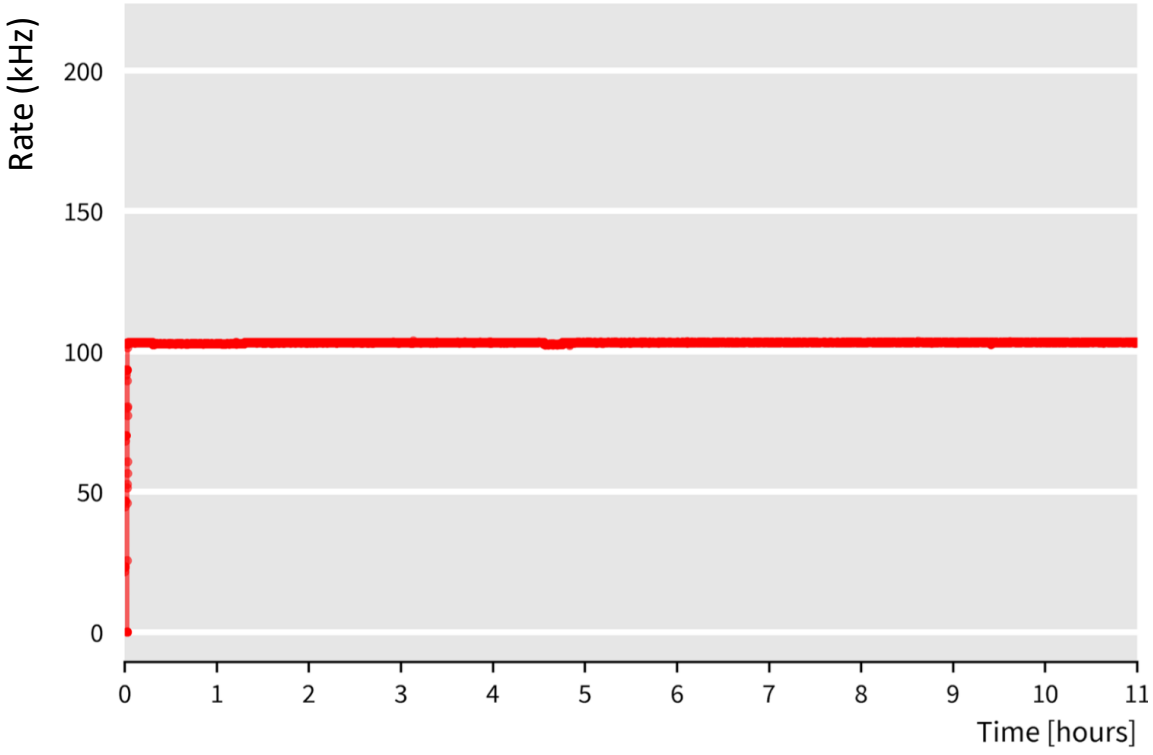
RaspberryPi



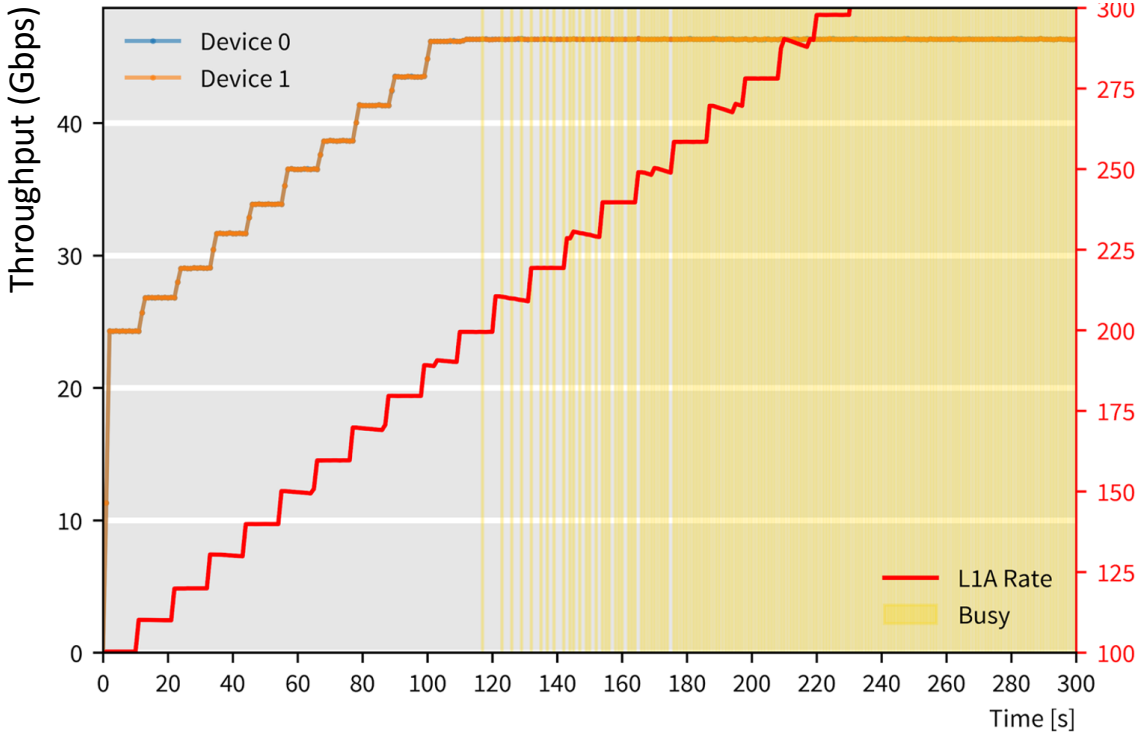
Performance studies

- Measured FELIX performance (including FPGA temperature) under demanding operating conditions. Realistic traffic patterns (random trigger at different average rates, variable data size) were used.

GBT Mode



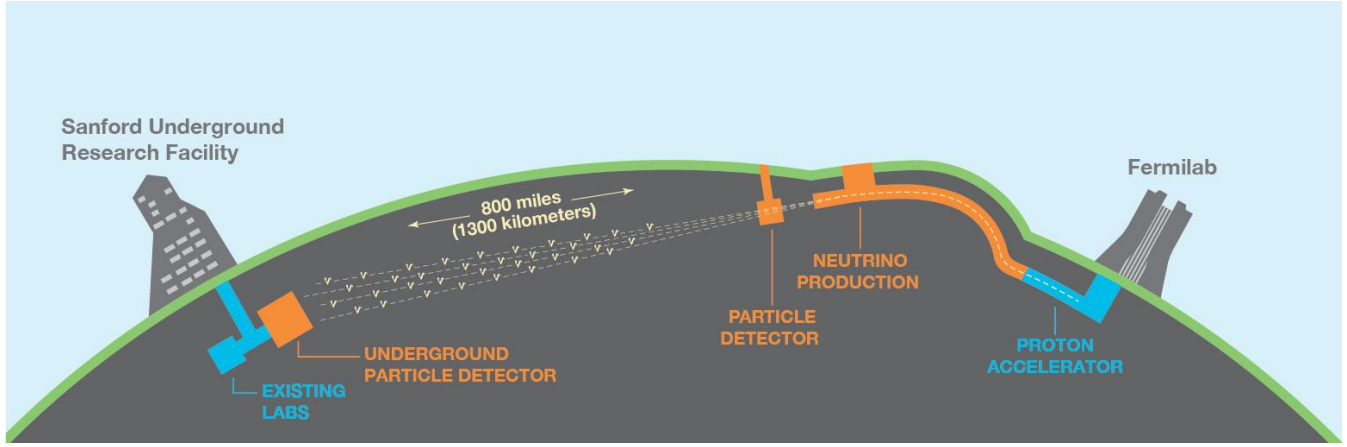
Full-Mode BUSY test



Performance Studies

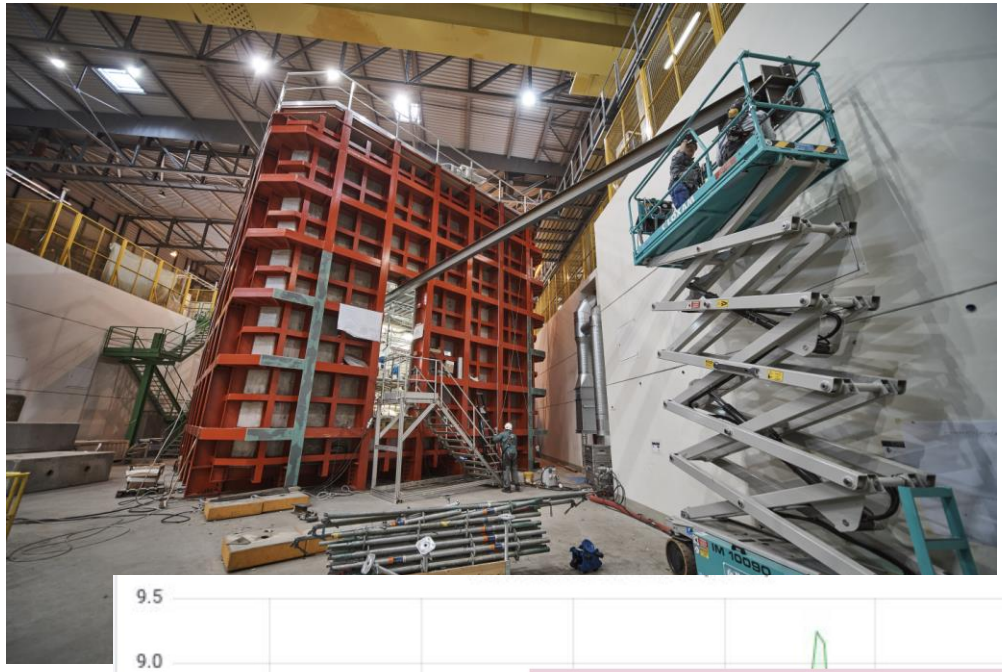
FELIX taking data in ProtoDUNE

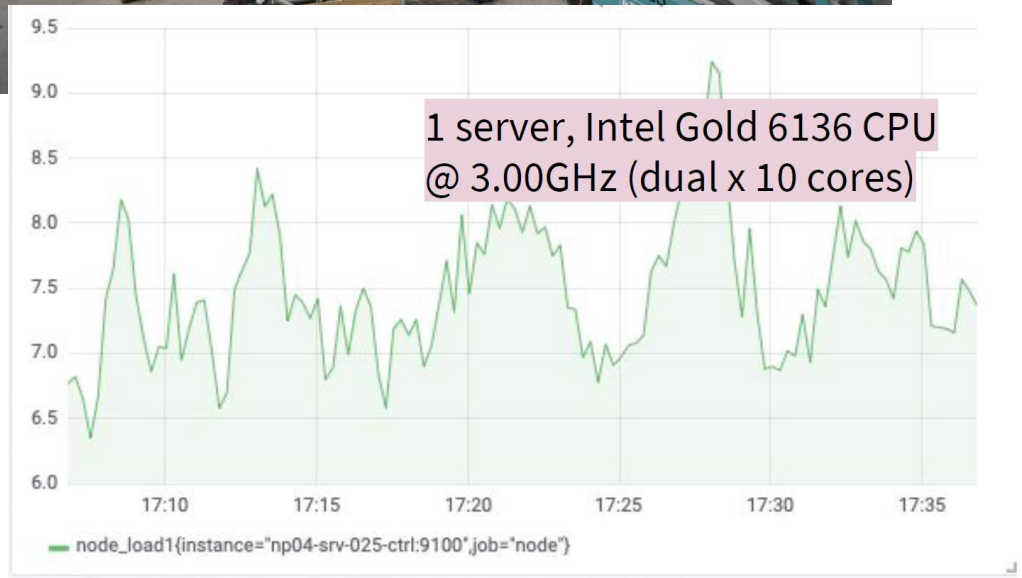
DUNE



ProtoDUNE

arXiv:1706.07081





1 server, Intel Gold 6136 CPU
@ 3.00GHz (dual x 10 cores)

ProtoDUNE uses FULL-mode FELIX.
Firmware modified to support jumbo-blocks (4kB instead of 1kB).
Up to 6 consecutive chunks of 464 Byte are merged, chunksize is 2784 Byte at a rate of 333 kHz.

Other experiments also considering FELIX

Summary & Outlook

- 23 pre-series FELIX board passed tests
- Firmware and software being finalized to user specifications
- FELIX shows good performance in lab tests as well as ProtoDUNE
- 120 FELIX boards with FELIX and SW ROD servers to be ordered soon and arrive in the fall for 2020 installation