Electronics upgrade for the CMS CSC muon system at the High Luminosity LHC

Isabelle De Bruyn (UW-Madison)

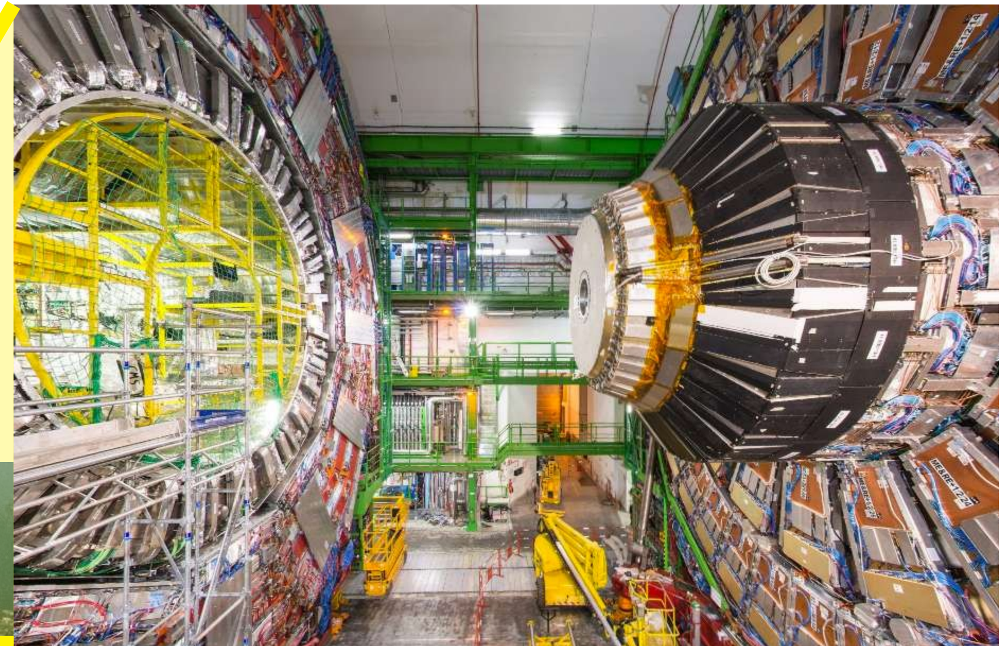
on behalf of the CMS Collaboration

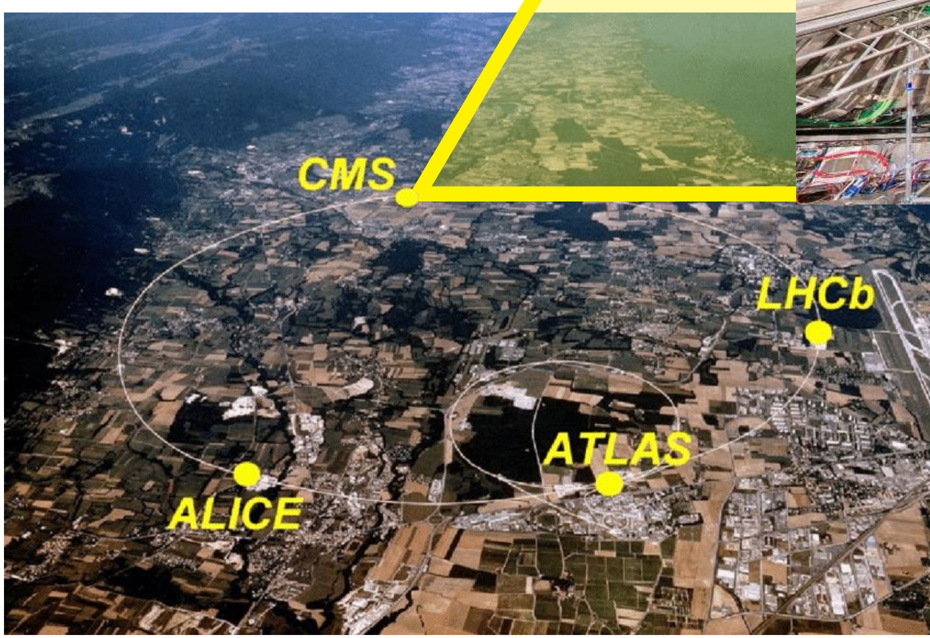
NEC2019

Becici, Montenegro

The CMS experiment

CMS is located at one of the 4 interaction points of the LHC accelerator complex at CERN

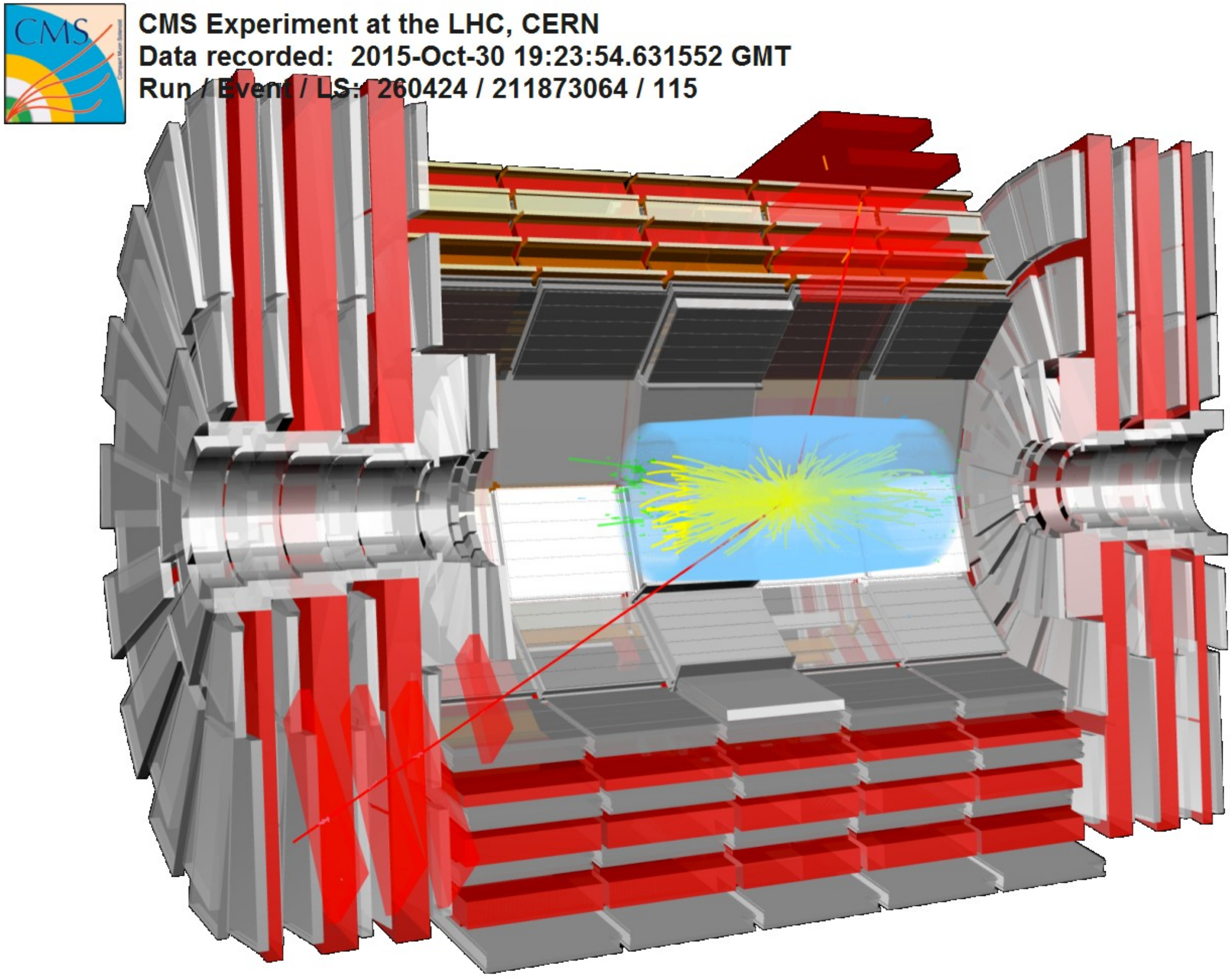




The Cathode Strip Chambers (CSCs) are aimed at detecting muons and are located in the endcaps of CMS, at high pseudorapidity ($0.9 < \eta < 2.4$)

→ higher rates of particles

Muon detection and triggering with CSCs



event display showing a muon going through several CSC chambers

- 4 stations / endcap for redundancy on muon triggering and tracking
- 2 or 3 rings / station
- 18 or 36 CSCs per ring

Total: 540 CSCs

→ more than 500,000 channels for triggering and 2D tracking

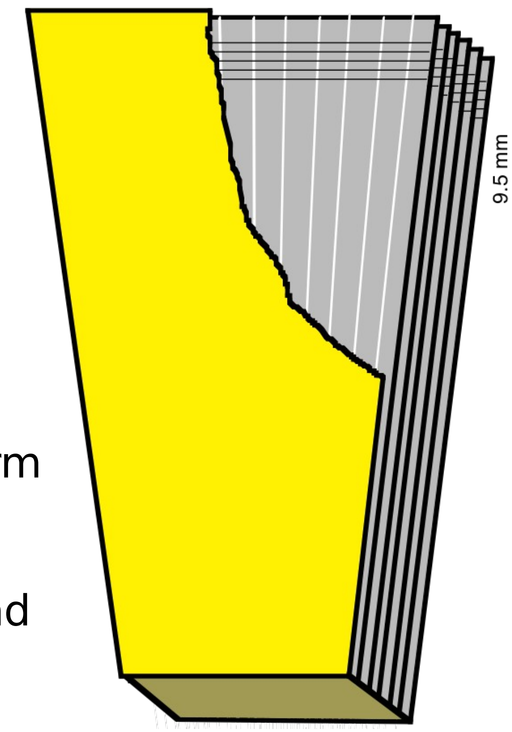
CSC chamber

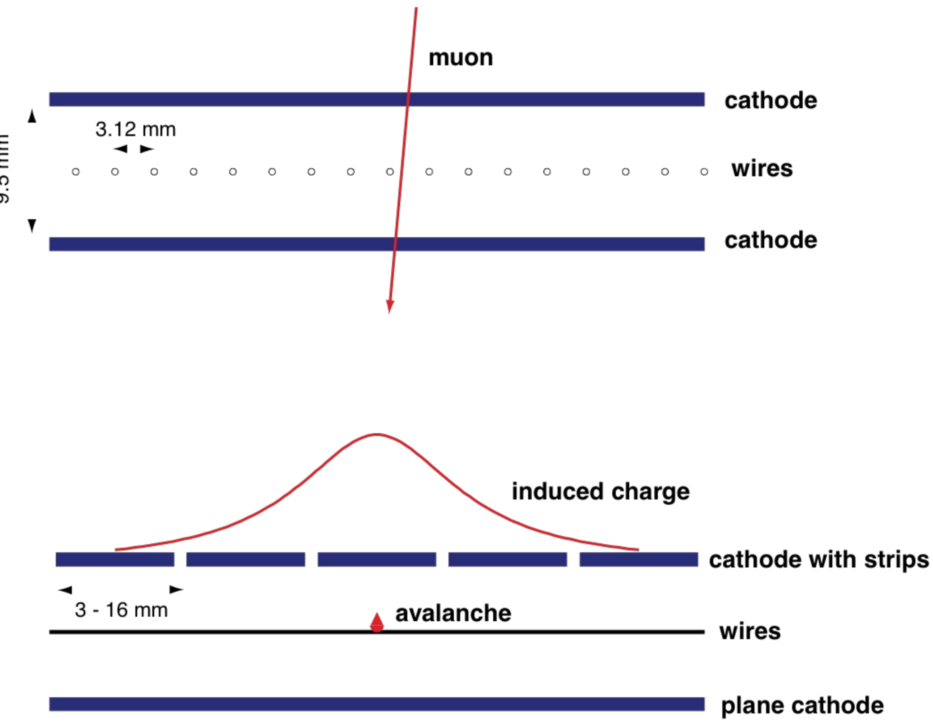
Each chamber has 6 independent layers that measure points (hits) along the muon trajectory

- 7 cathode panels forming six gas gaps
- 6 cathode panels are segmented into radial strips (measure φ accurately)
- 6 wire layers (anodes) in the middle of each gas gap running transversally

Muons ionize gas
(Ar / CO_2 / CF_4, 50:40:10%)
in each gap

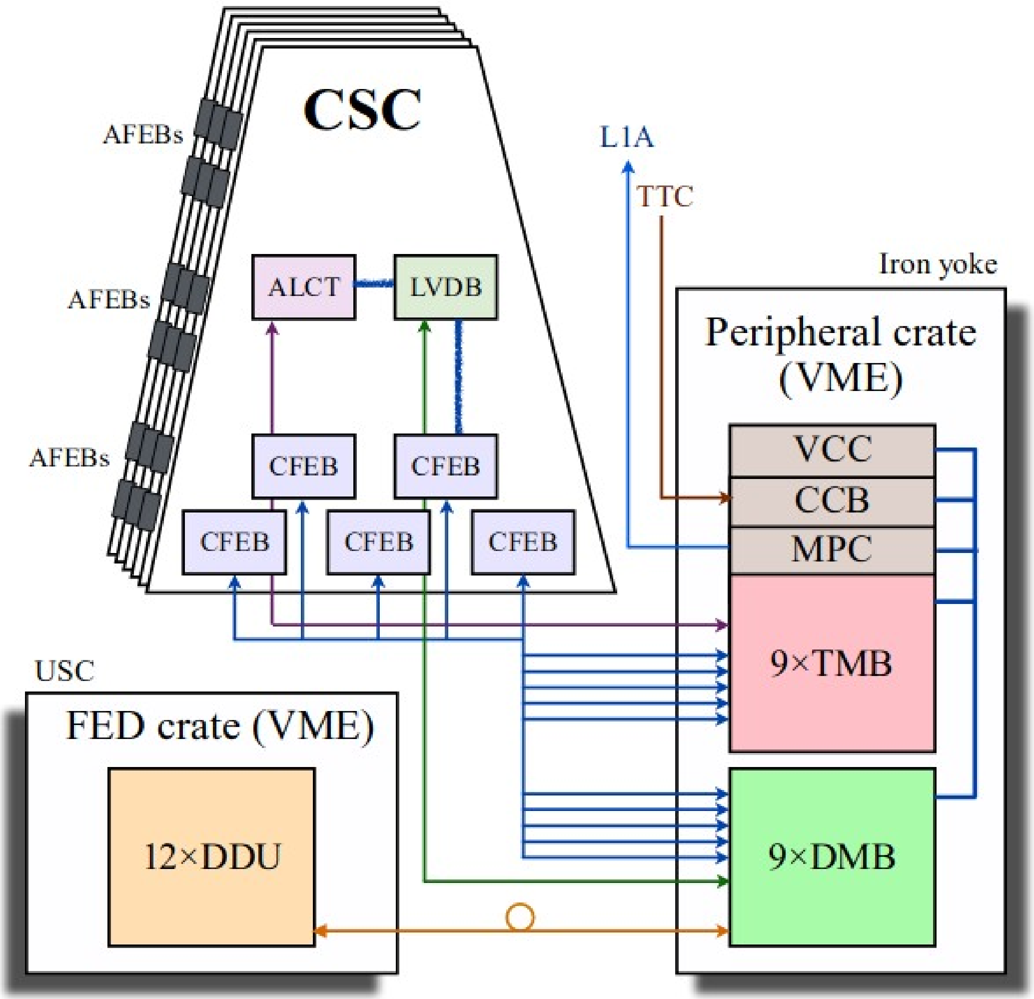
- electrons (ions) drift to wires (strips)
- signals read out and processed by several electronic boards to form coincidences of anode and cathode signals → trigger primitives and trajectory hits





CSC Electronics

- strips are read out and processed by **Cathode Front-End Boards (CFEBs)**
- wires are read out and processed by the **Anode Local Charged Track (ALCT) board**
- **Low Voltage Distribution Board (LVDB)** is providing power to the boards
- **Trigger Motherboard (TMB)** and **Data Motherboard (DMB)** are located in peripheral crates located at the periphery of the endcap disks
- backend: data sent from DMB to **detector dependent unit (DDU)** in Front End Driver (FED) crate (= interface between front end electronics and global CMS data acquisition system)

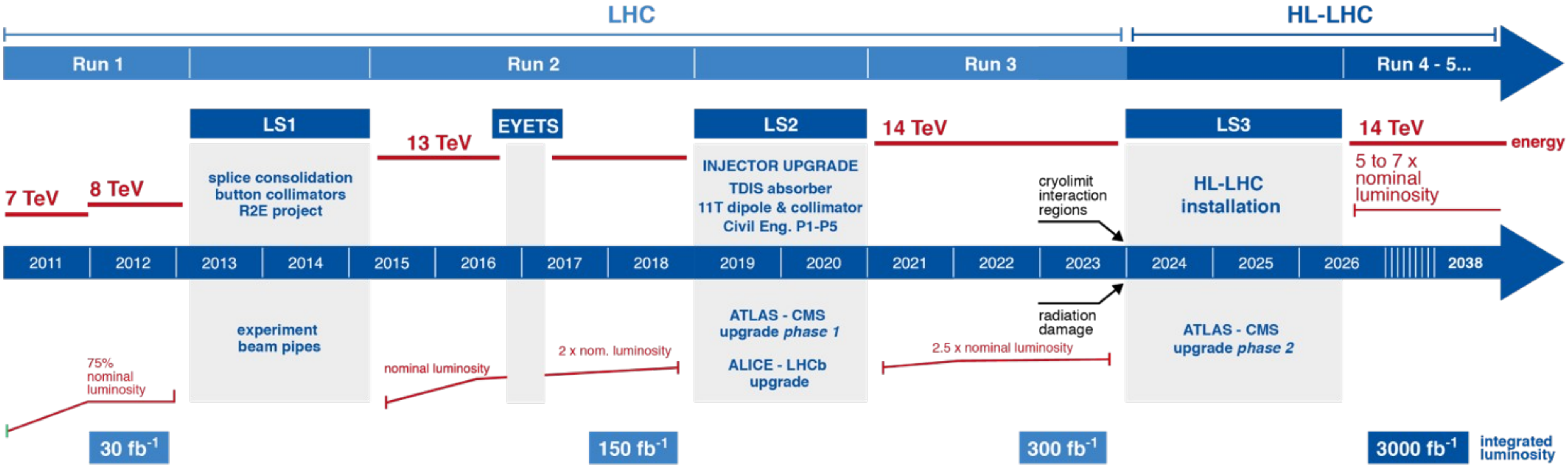


High Luminosity LHC (HL-LHC)

Upgrade of the LHC:

- instantaneous luminosity of up to 7.5 10^{34} $cm^{-2}s^{-1}$ (5x nominal LHC value)
- collecting up to 3000-4000/fb of data
- at nominal energy of 14 TeV

→ will require CMS to be able to handle a L1 trigger latency of 12.5 µs
and a L1 trigger rate of 750 kHz



Upgrade motivation

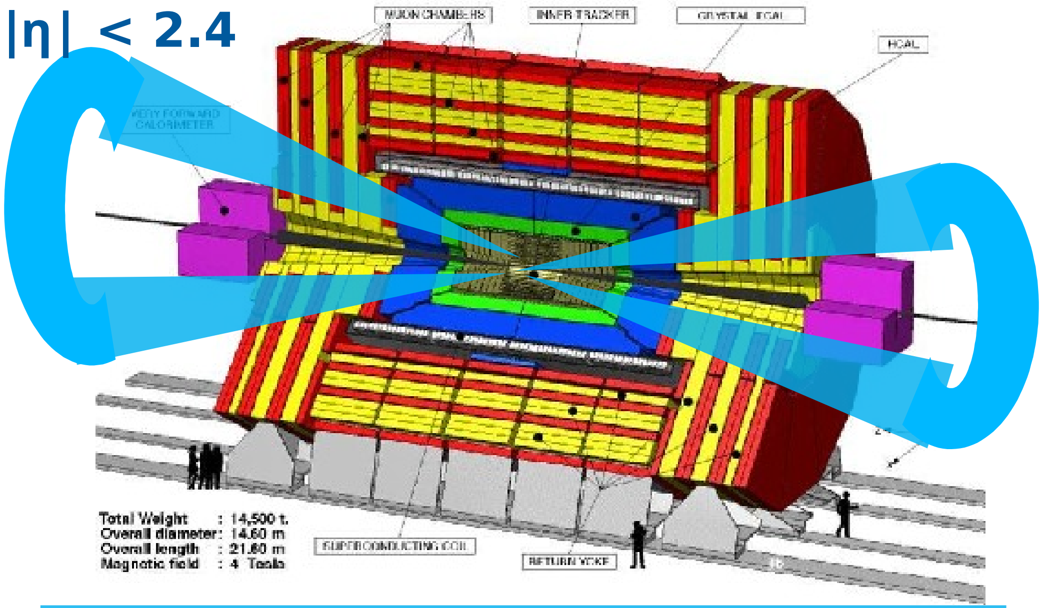
Upgrade of the high-eta CSCs (innermost rings)

Limiting factors of the present electronics:

- **L1 trigger rate:** old CFEBs do not have enough buffering for chambers closest to beamline
- **Longer L1 trigger latency:** required for new track trigger
- Output **bandwidth** and **pipeline length** (not enough BRAM in Virtex-E FPGA) of ALCT electronics not sufficient
- GBTx (instead of EEPROM) programming to mitigate EEPROM failures experienced in 2017 in high-occupancy CSCs (ME1/1)

HL-LHC schedule imposes changes after LS3, but CMS **installation opportunity in LS2**

$1.6 < |\eta| < 2.4$

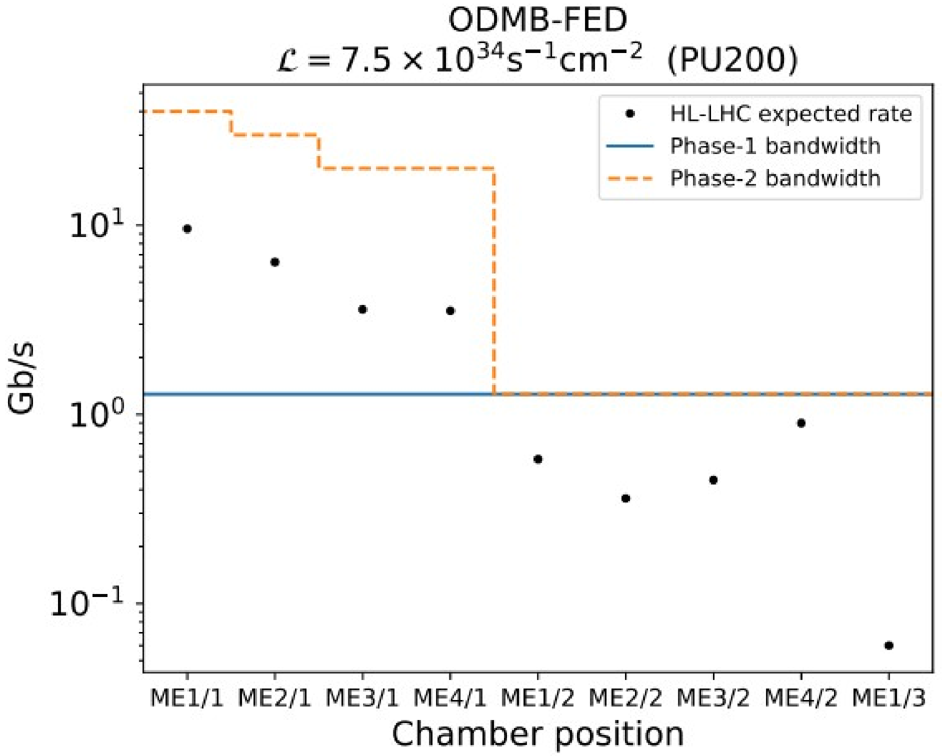


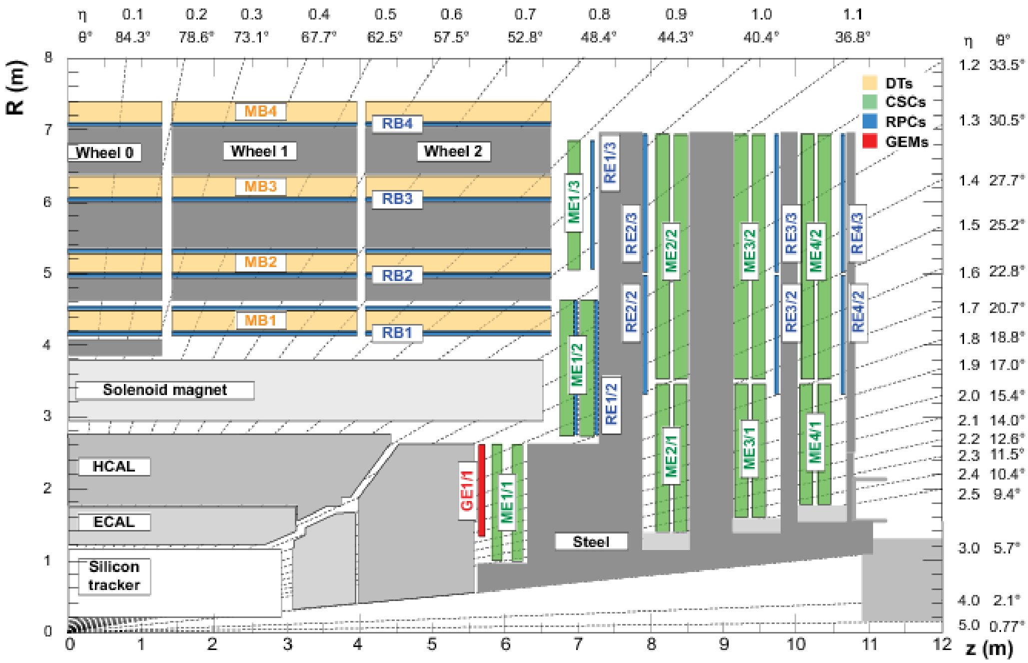
Approximate angular region of the inner rings:
ME1/1, ME2/1, ME3/1, ME4/1
= 180/540 chambers

Upgrade motivation

Bandwidth of ODMB output (currently 1 Gb/s) insufficient for expected HL-LHC rates

→ upgrade of optical links and redesign of backend with ATCA technology

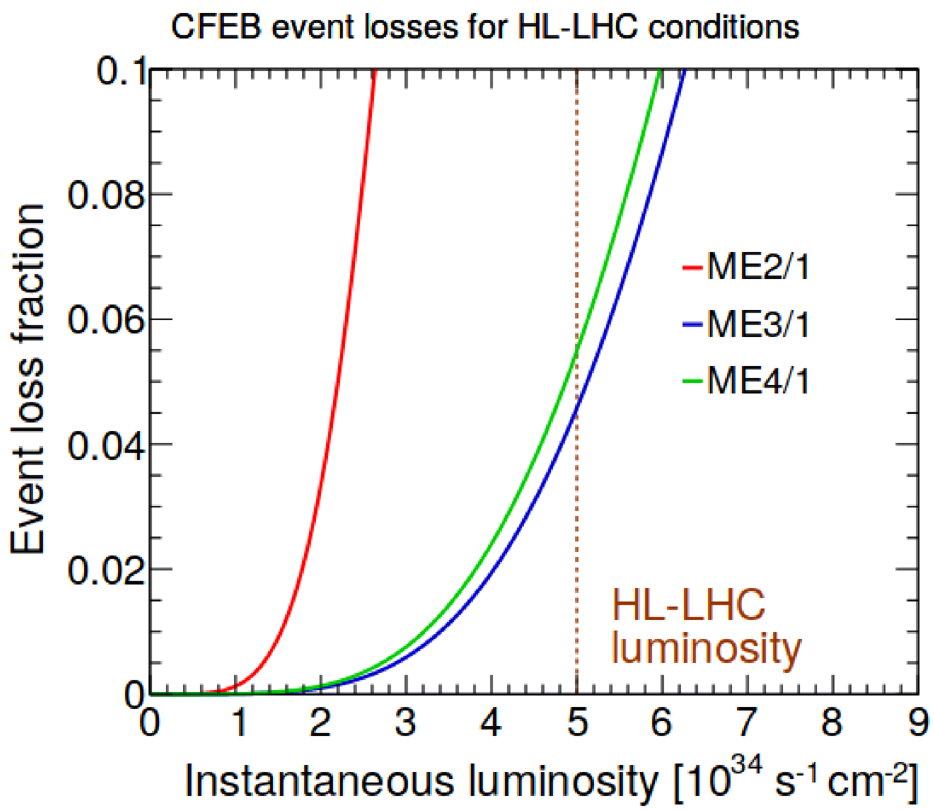


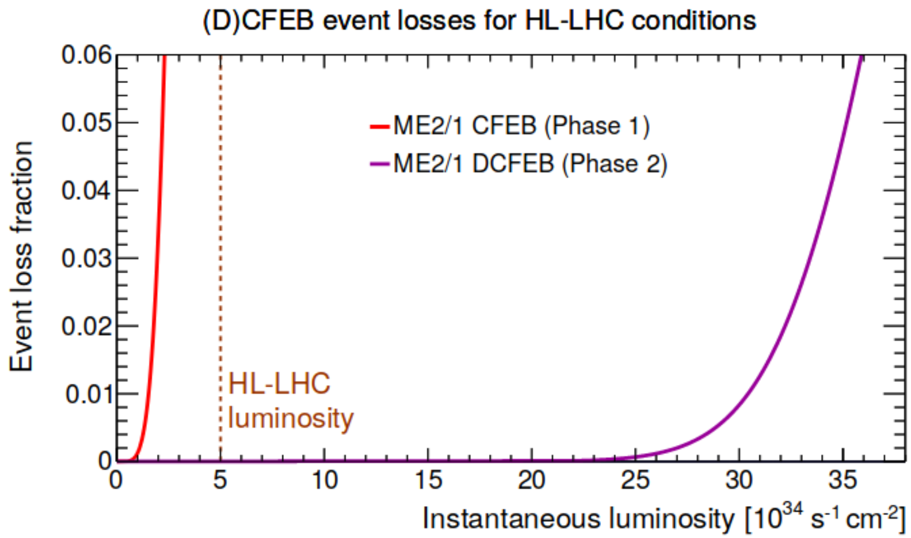


Upgrade motivation

Expected data loss with current electronics due to:

- insufficient buffer size of front end electronics
- longer latency requirements
- insufficient output bandwidth due to higher L1 trigger rates and occupancy





Expected to lose entire ME2/1 ring with current CFEB
→ no data loss with upgraded DCFEB

Radiation hardness

Electronics need to survive high rate of collision and background particles, especially in inner ring chambers

→ new boards and components (optical transceivers, regulators, EPROM, ...) underwent radiation tests

at CHARM, CERN (mixed hadron spectrum)
Texas A&M cyclotron (neutrons)
UC Davis cyclotron (protons)

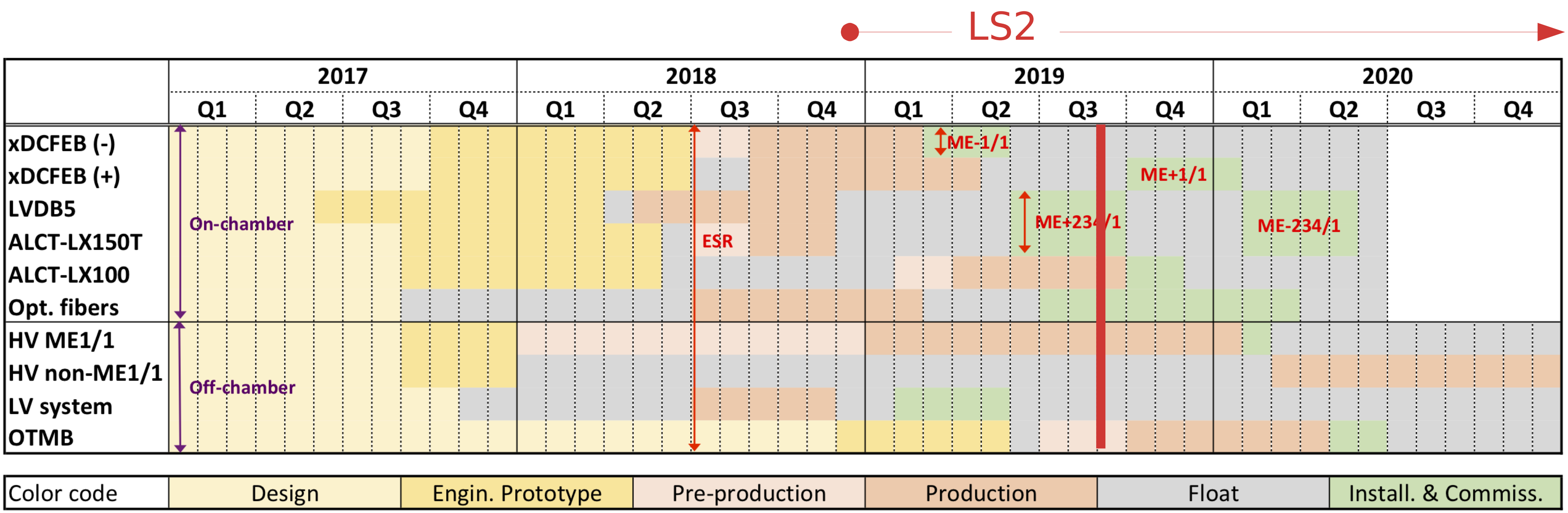
- total integrated dose up to 30 kRad
(3x expected 10 kRad for 3000/fb at HL-LHC)

- susceptibility of electronics to single-event upsets (SEUs)
change of state caused by one single ionizing particle striking a sensitive node in a micro-electronic device
  - study SEU rate and electronics deadtime

Timeline

LS2 (2019-2020) : on-chamber electronics (DCFEB, ALCT, LVDB)
+ Trigger Motherboard (OTMB)
+ general services (LV, HV)

LS3 (2024-2026) : Data Motherboard (ODMB) + backend
+ high bandwidth optical links

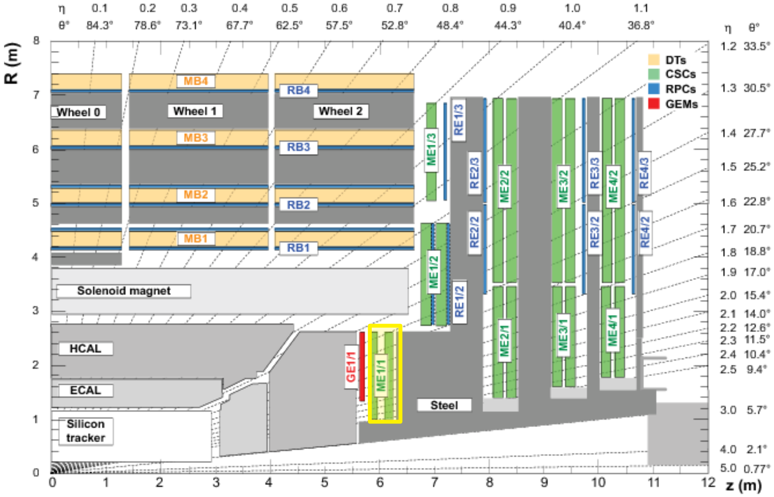


New Digital Cathode Front End Board (xDCFEB)

LS2

Remote programming of FPGA via Gigabit optical Transceiver (GBTx) as alternative to programming via EEPROM after experiencing instances of EEPROM corruption in 2017

Replacing existing DCFEBs (installed in LS1) on inner ring of station 1 (ME1/1) to enhance operational stability at highest radiation doses (~10kRad for 3000/fb at HL-LHC)



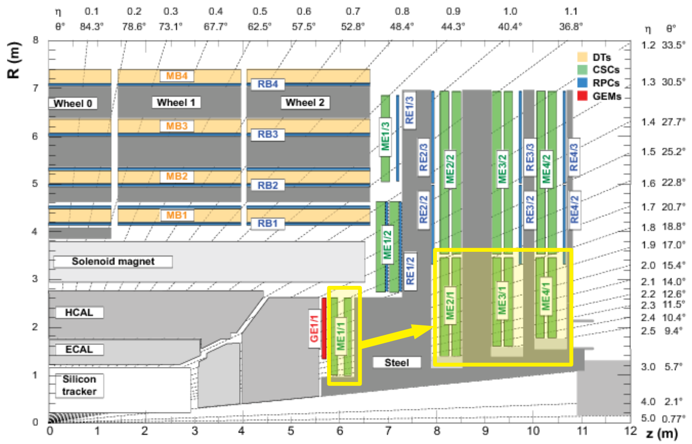
Digital Cathode Front End Board (DCFEB)

LS2

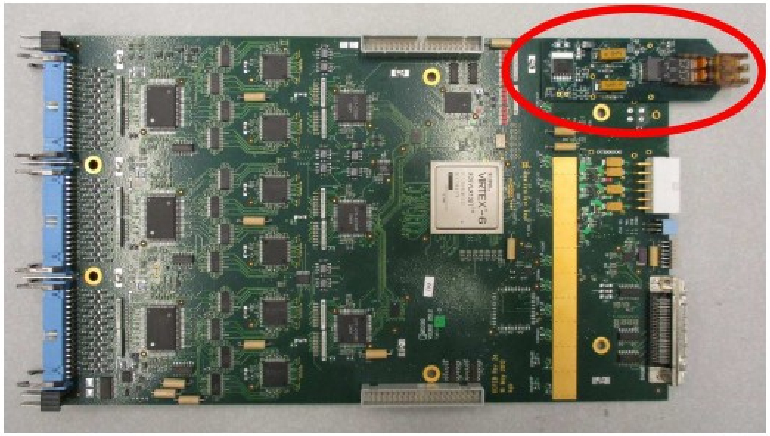
Existing DCFEBs from inner ring of station 1 (ME1/1) are being installed on CSCs of inner ring of stations 2, 3, 4 (lower radiation dose)

Additionally, replacement of optical transceivers:

- 6 (10) failing (no output light) Finisar optical transceivers in 2018 (2017)
- Temporary optical link loss due to SEU (~1/day in 2018)
  - recovered by powercycling the DCFEB
- Replace Finisars by VTTx's (SEU immune)



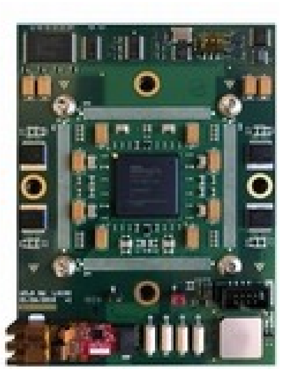
⇒

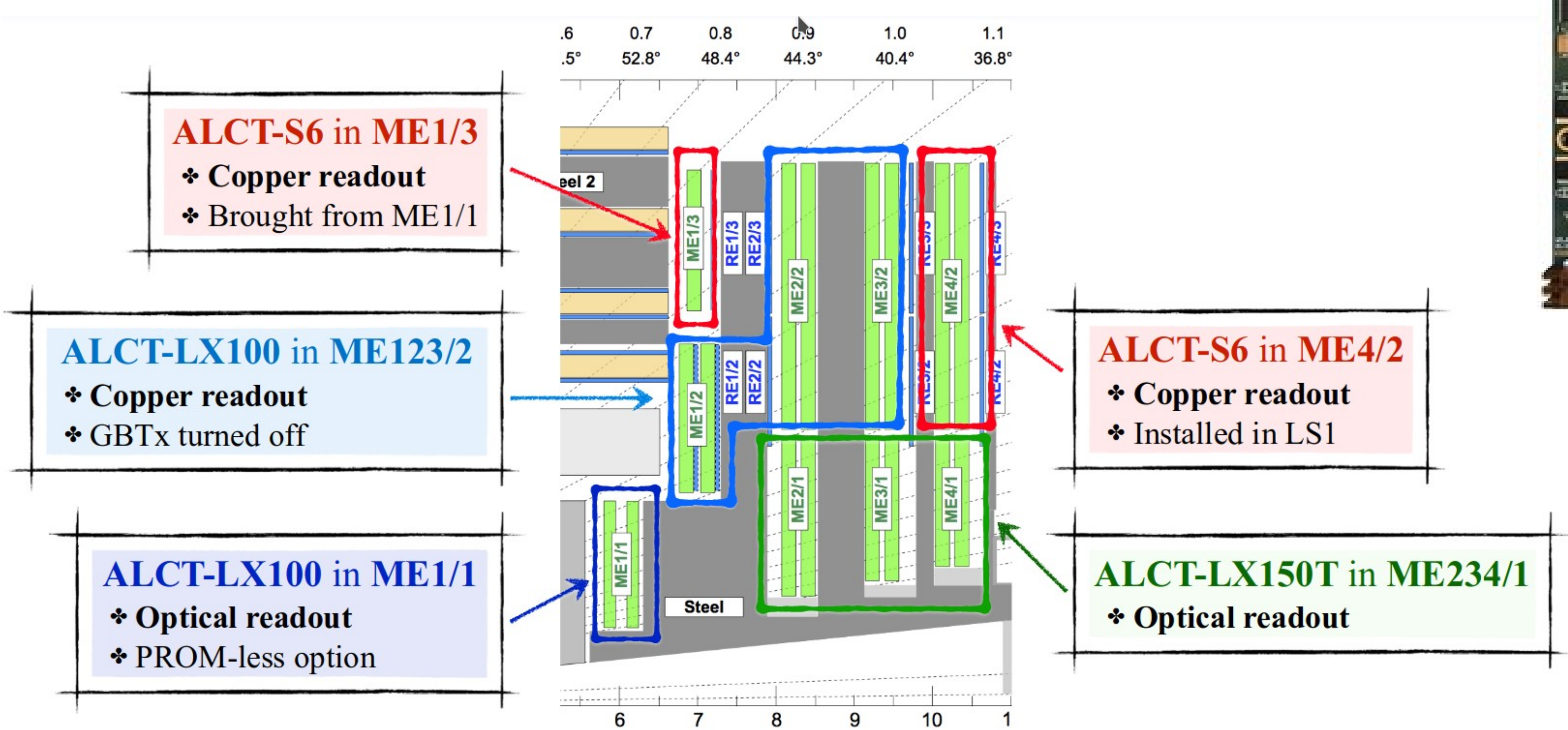


Anode Local Charged Track (ALCT) mezzanine boards

New **ALCT mezzanine** boards with optical readout and Spartan-6 instead of Virtex-E FPGA to support increased latency and larger output bandwidth

LS2



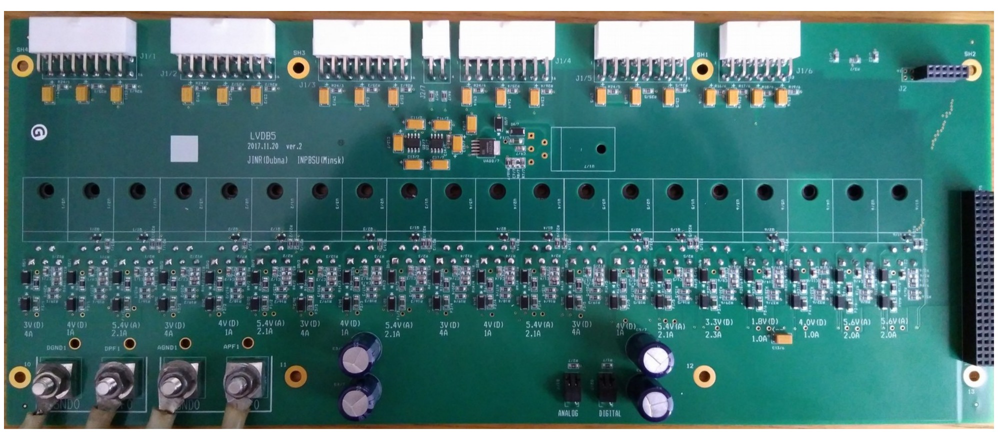


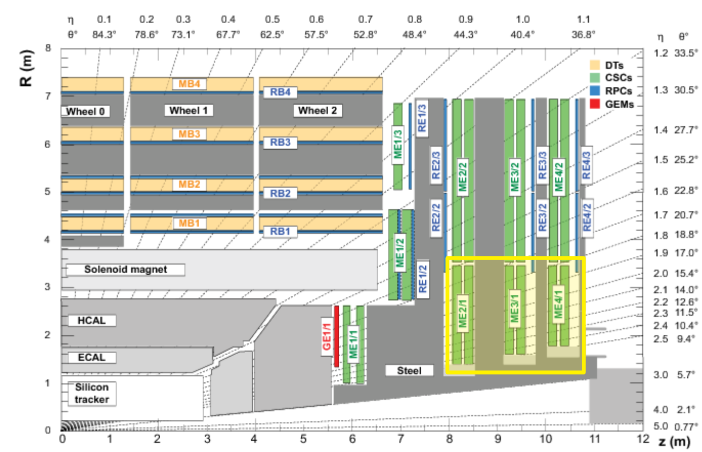
Low Voltage Distribution Board (LVDB)

New LVDB to provide increased current and appropriate voltages to the DCFEBs in inner rings of stations 2,3,4 (ME234/1)

LS2

- being installed and tested (48h burn-in test)
- LV system also upgraded to supply the necessary currents
  - additional power supplies and improved partitioning



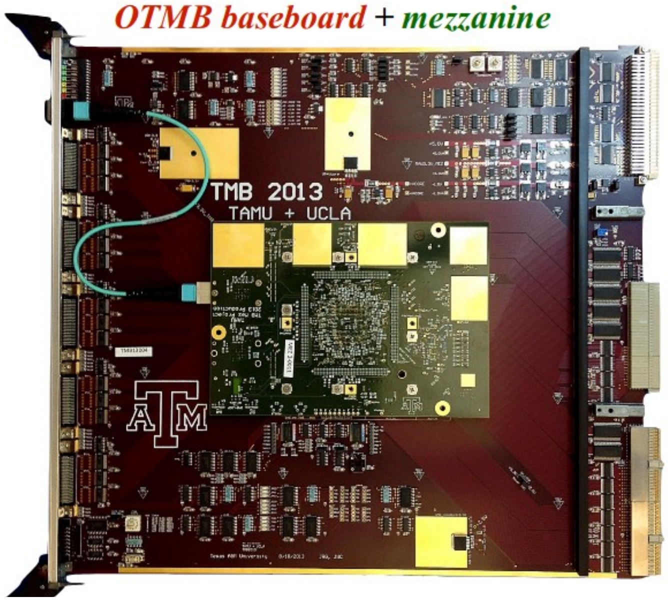


Optical Trigger Motherboard (OTMB)

Trigger Motherboard of inner rings of stations 2,3,4 (ME234/1) need to be upgraded to Optical Trigger Motherboards (OTMBs) to receive trigger data from the DCFEBs by optical fibers instead of copper cable (TMB)

LS2

- More powerful FPGA for providing increased algorithmic performance.
- New design will allow receiving trigger primitives from future GEM neighbouring muon system to form CSC+GEM "super-primitives"
- Production planned later than other boards to distribute funding profile
- Production to start this month and expected to complete in early 2020



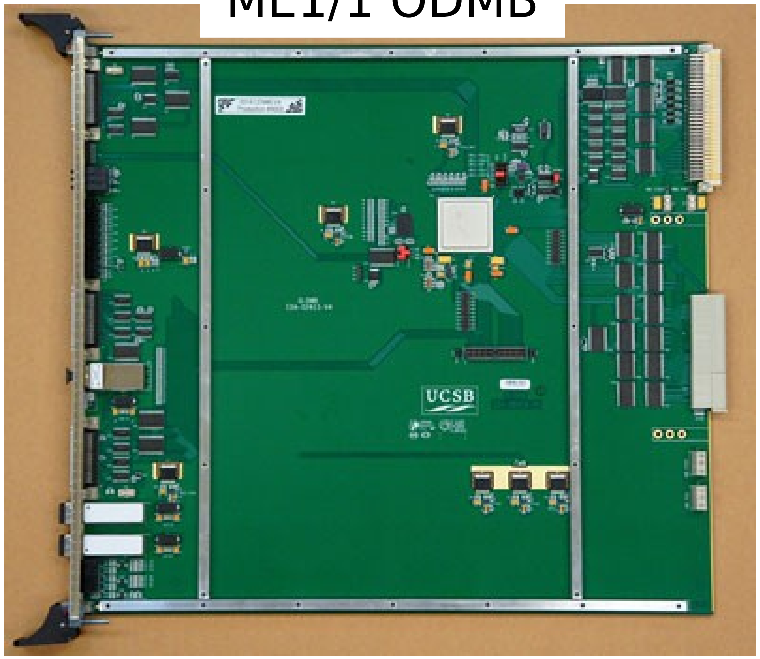
Optical Data Motherboard (ODMB) and backend

LS3

Optical Data Motherboard (ODMB) to receive data from DCFEBs through optical fibers and with larger output bandwidth

- Started designing new boards
  - baseline is ME1/1 ODMB installed in LS1
  - Artix 7 FPGA instead of Virtex 6
- Production planned for 2020-2021

ME1/1 ODMB



Backend

Replacement of backend VME crates with ATCA

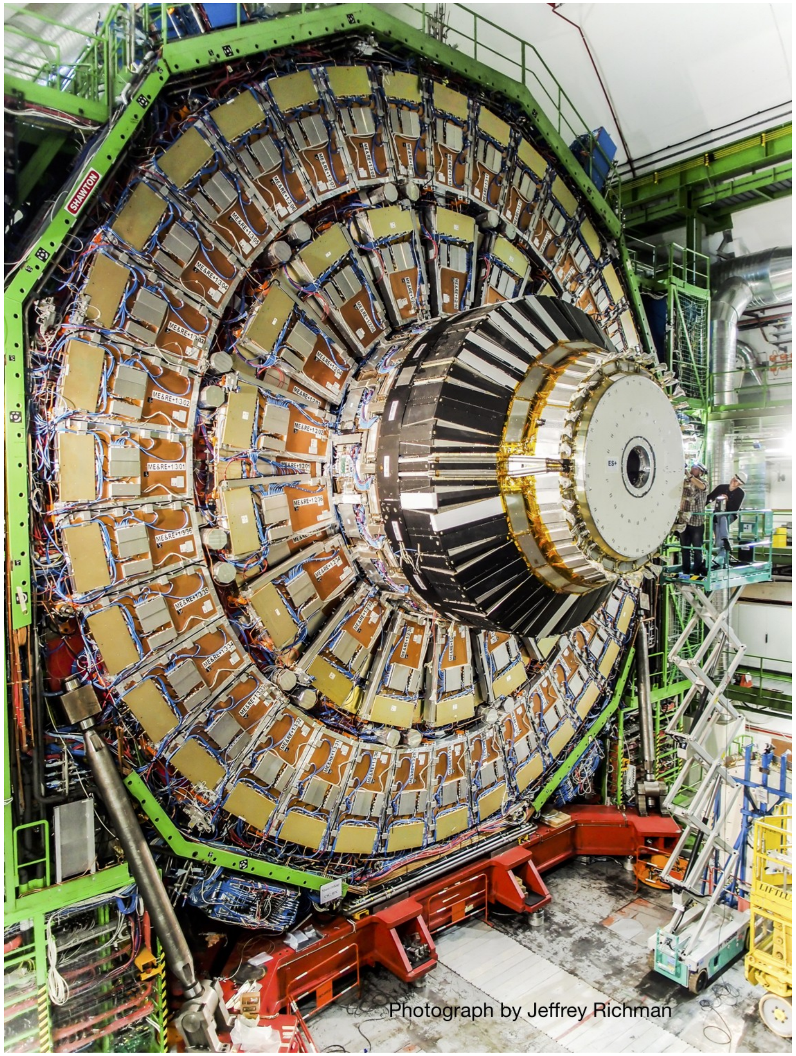
LS3

- plan to use common CMS modules
- using µTCA cards to develop firmware
- will be able to handle 900 optical links at speeds up to 6.4 Gb/s
  → total data rate of 598 Gb/s,
- total of 12 of these boards would be able to handle the CSC data rates expected at HL-LHC
- Production procurements planned to begin in 2022

LS2 upgrade: size of the project

LS2 schedule includes 15 months (Mar 2019 – Jun 2020) of continuous work to upgrade electronics of **180 CSCs** (33% of the total CSC system)

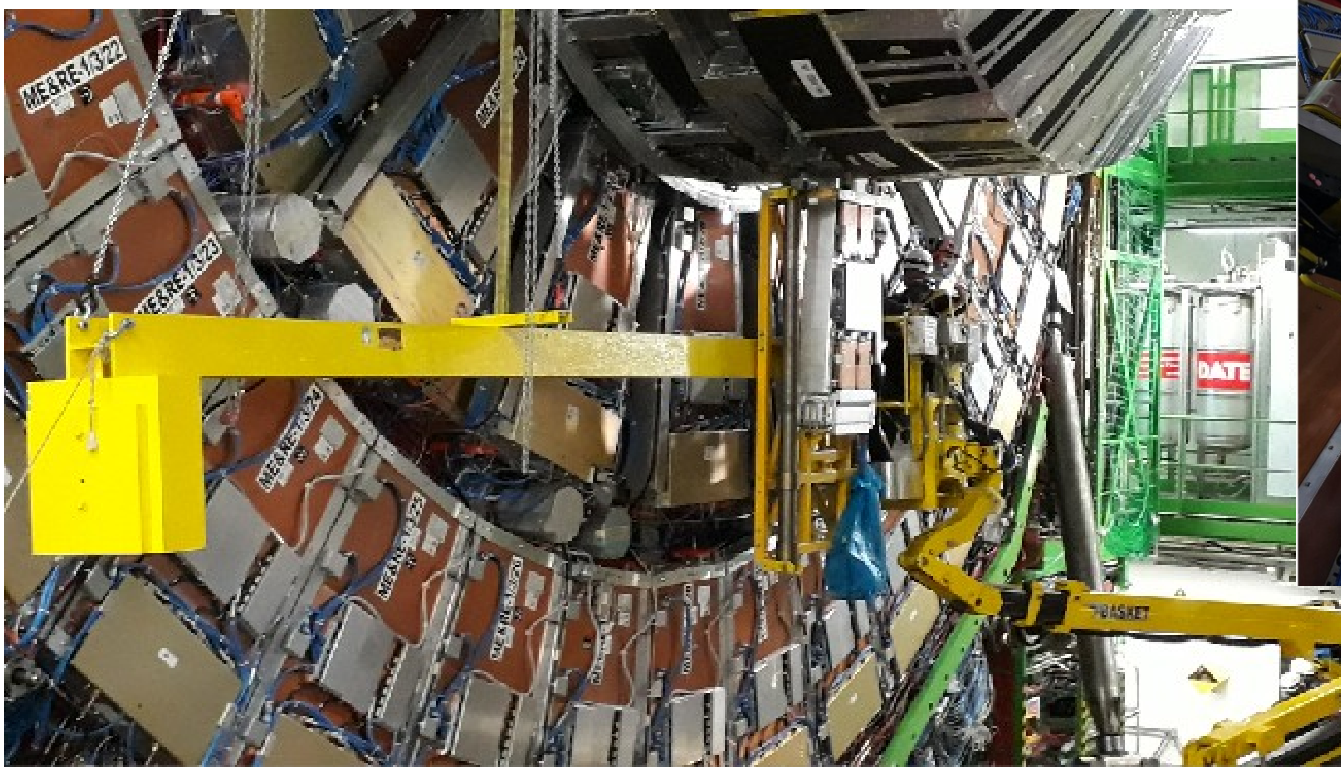
- 504 DCFEBs to replace and refurbish
- 540 CFEBs to replace
- 108 LVDBs to replace
- 468 ALCT mezzanines to replace on extracted chambers and in situ
- 108 TMBs to replace



Electronics refurbishment workflow

Chamber extraction (and reinstallation):

CSCs are extracted from the CMS apparatus and transported from underground cavern (-100m) to dedicated lab at the surface



- up to 190 kg / chamber
- up to 1.5 m x 2 m

Electronics refurbishment workflow

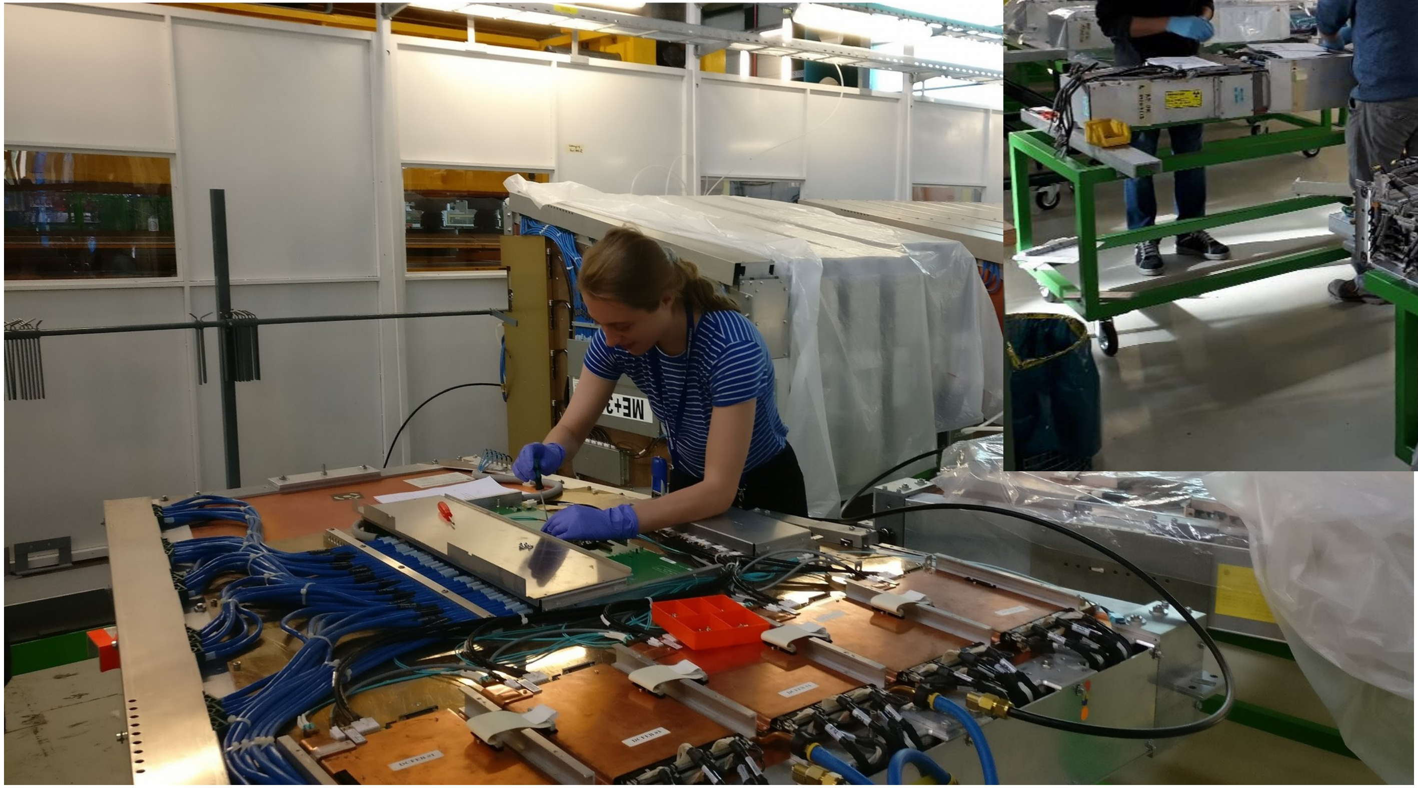
CSC lab:

- storage of chambers
- board replacement
- testing of new electronics

Electronics refurbishment workflow

Electronics replacement:

~ 20 people alternating shifts weekly to refurbish and test the chambers



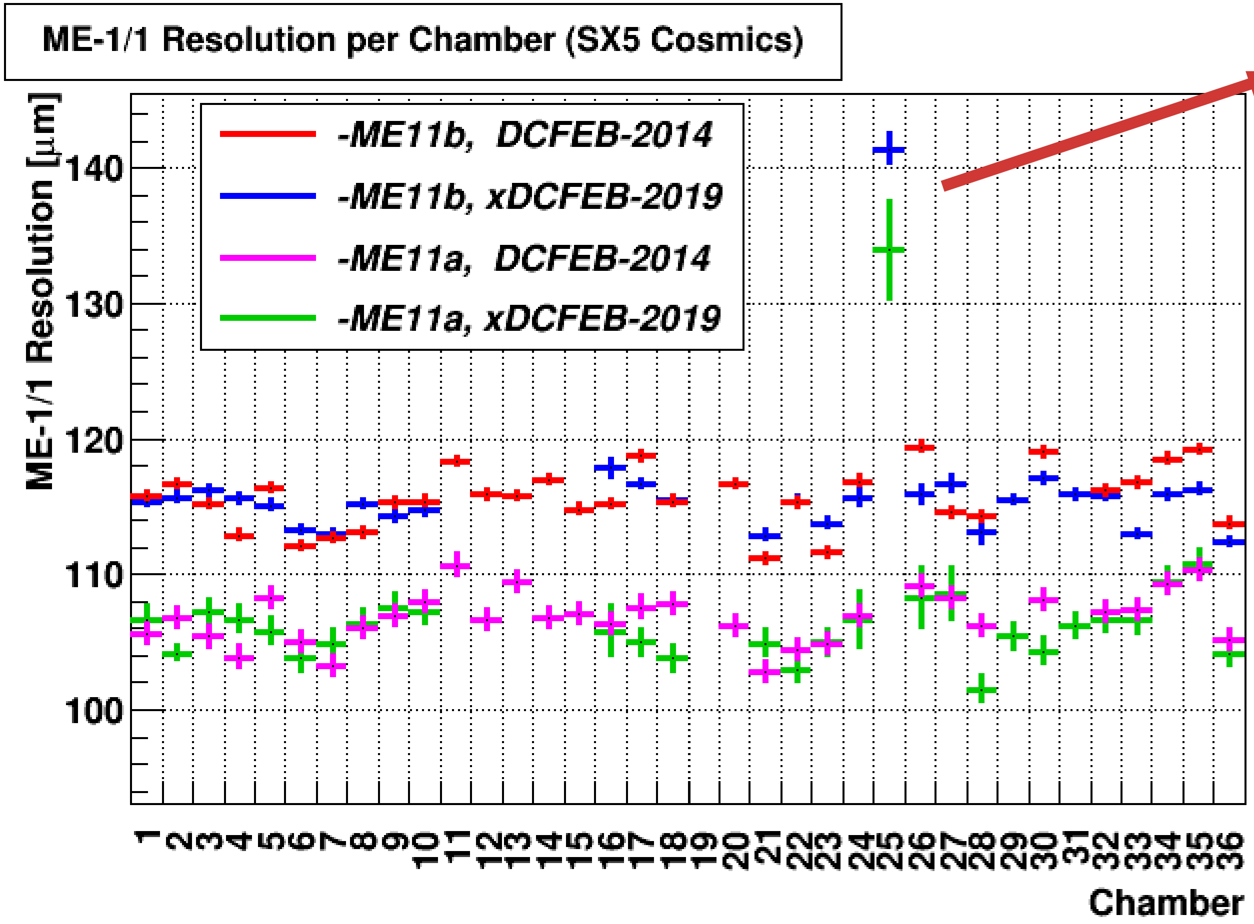
Electronics refurbishment workflow

Refurbishment of electronic boards in a specialized workshop due to the (low) activation of the boards (< 0.1 µSv/h):

- (de)soldering of components
- time-consuming radiation measurements, tracking, transport

Status of the LS2 Upgrade

First part of upgrade finished:
refurbishment of ME-1/1 chambers (DCFEB and ALCT mezzanine replacement)



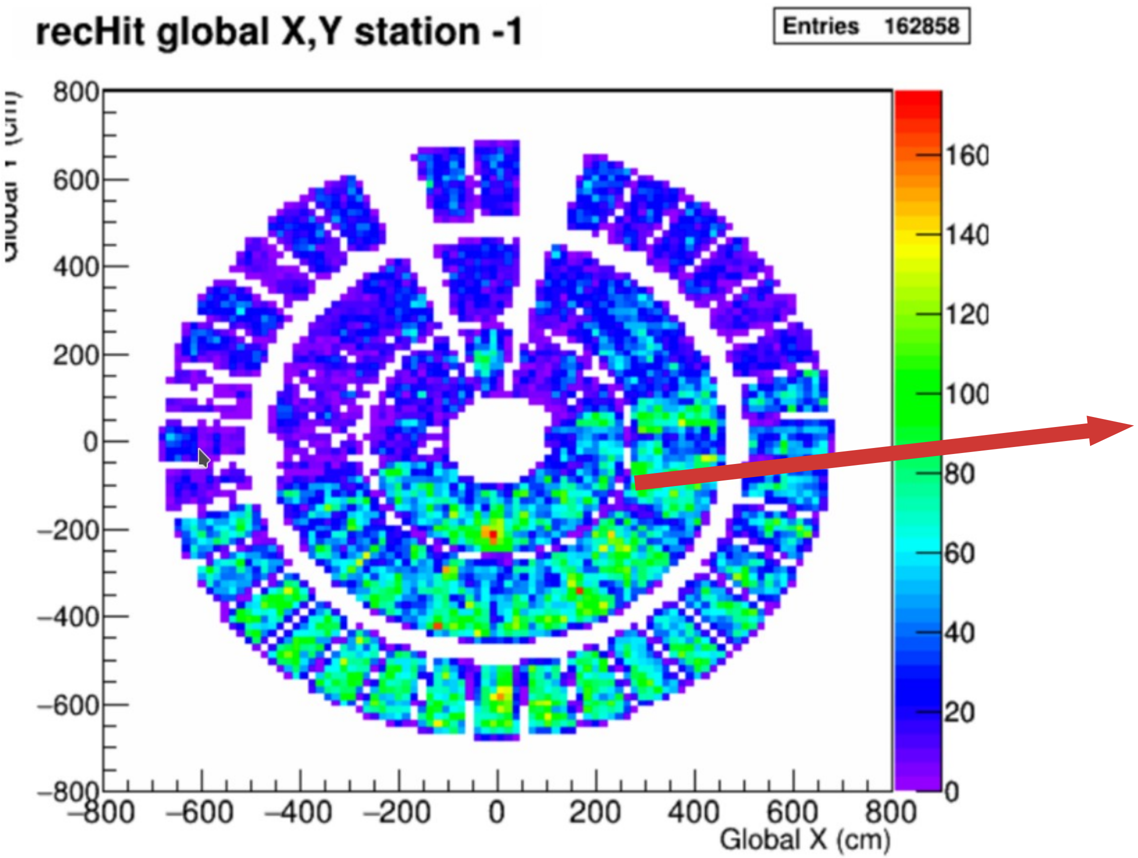
outlier due to lower gas gain at lower HV setting

Performance of ME-1/1 studied using data from cosmic runs taken during testing in lab before re-installation:

- good segment quality (mainly 6-hit segments)
- good spatial resolution, consistent with earlier cosmics data in similar conditions

Status of the LS2 Upgrade

First part of upgrade finished:
refurbishment of ME-1/1 chambers (DCFEB and ALCT mezzanine replacement)

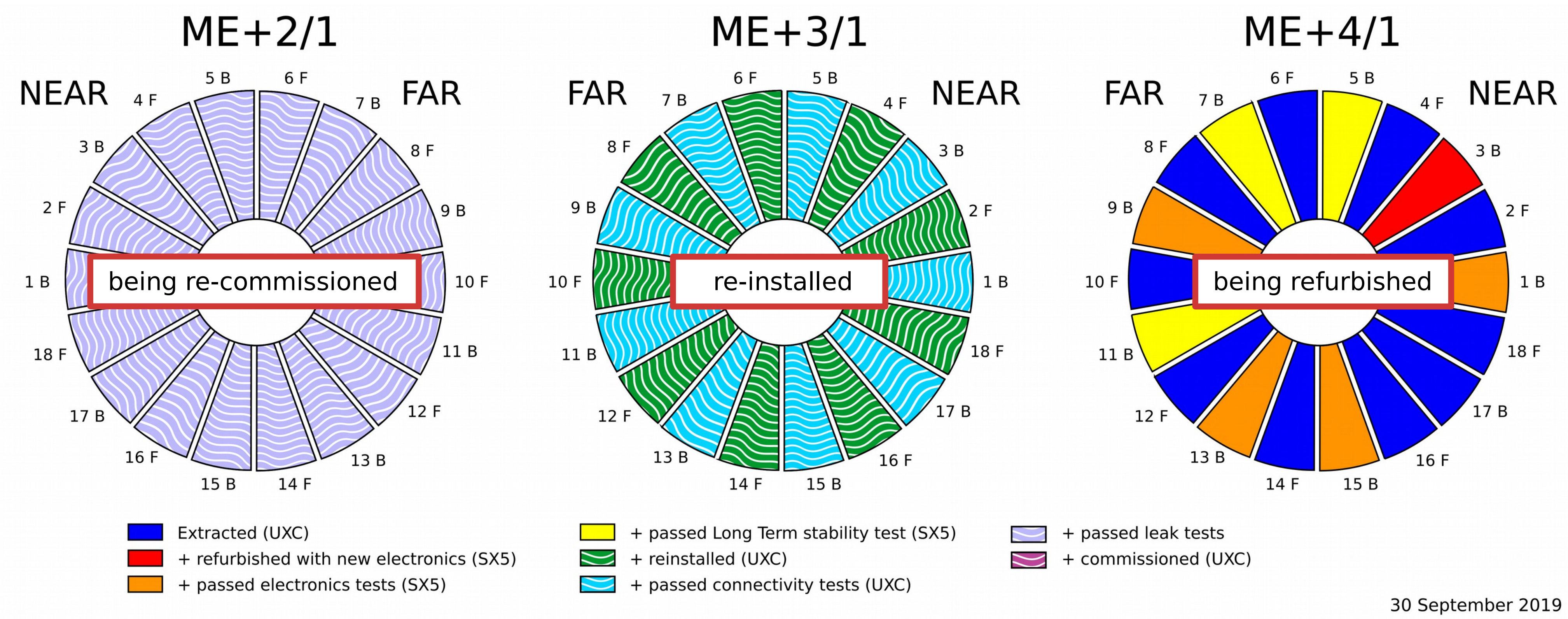


Refurbished chambers successfully participated in a run together with other subdetectors of CMS!

hit occupancy during a cosmic run, triggering on the bottom part of the detector
(most useful to get decent statistics for the central detectors, dedicated runs with top-only triggers are taken as well to illuminate the top chambers)

Status of LS2 upgrade

ME+234/1 refurbishment is ongoing



Summary

Electronics upgrade of CMS Cathode Strip Chambers is ongoing and will completed in LS3, to prepare for larger latency and higher L1 trigger rate at HL-LHC (> LS3)

- part 1/4 of LS2 upgrade (ME-1/1 chambers) already done and showing good performance
- part 2/4 (ME+234/1) is progressing on schedule
- Optical Data Motherboards and backend system will be installed in LS3
  - currently discussing items related to technical requirements, performance, components, and design

Backup

Upgrade scope

LS2

Anode Local Charged Track electronics: replace mezzanine cards to **increase latency capability and output bandwidth**

LS2

Low Voltage Distribution Boards: replace to provide voltages and currents for Digital Cathode Front End Boards

LS2

Trigger Motherboard: replace with optical Trigger Motherboard to receive Digital Cathode Front End Board trigger data, increased algorithmic power

LS2

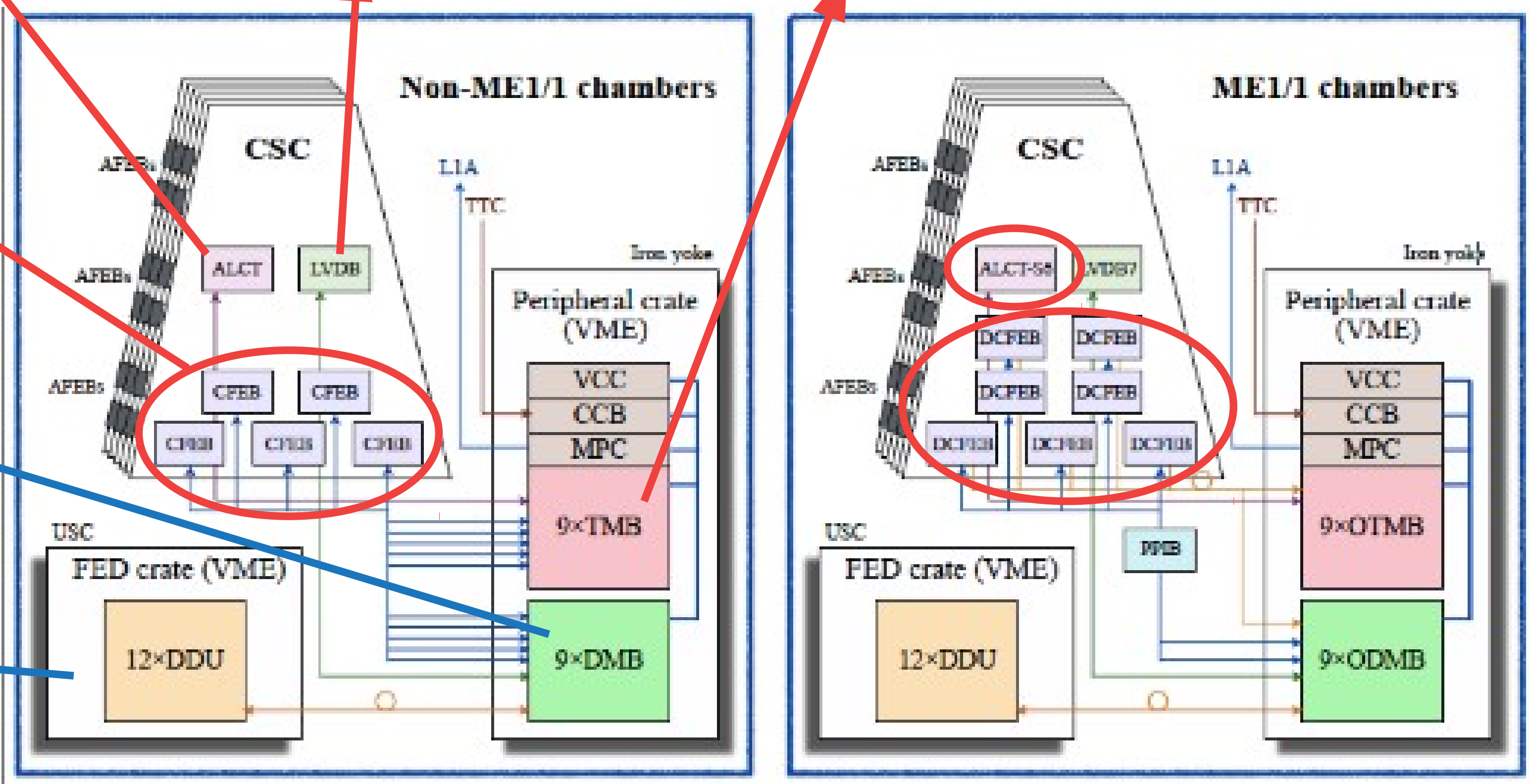
Cathode Front End Boards: replace with Digital Cathode Front End Boards with **increased latency and rate capabilities**

LS3

Data Motherboard: replace with optical Data Motherboard to receive Digital Cathode Front End Board data

LS3

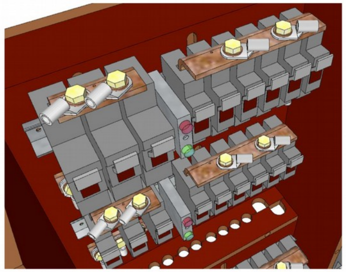
Front End Driver: **increased data volume**, number of links



Services: LV – HV - fibers

Low Voltage system is being upgraded because of increased power requirements of new DCFEBs and ALCTs:

LS2

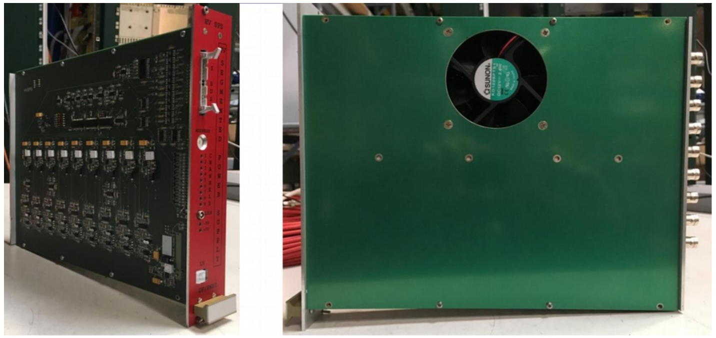


junction box

- LV Wiener Maraton system (air cooled)
- upgrade of station 2,3,4 inner rings (first endcap) ongoing

High Voltage:

- upgraded to cope with the increased chamber currents expected at HL-LHC fluxes
- station 1 inner ring: replace Caen based system with custom system (with higher current monitoring resolution) as used on other rings to have homogenous system
- tested and ready to be deployed any time



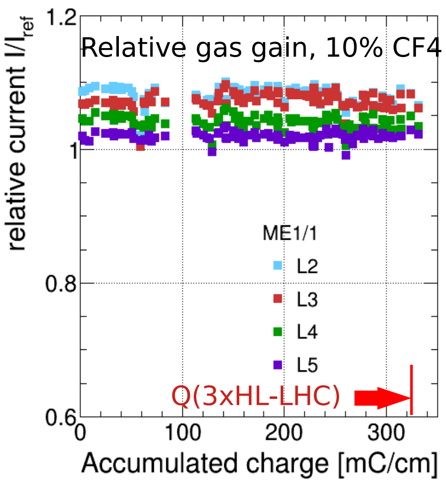
Fibers:

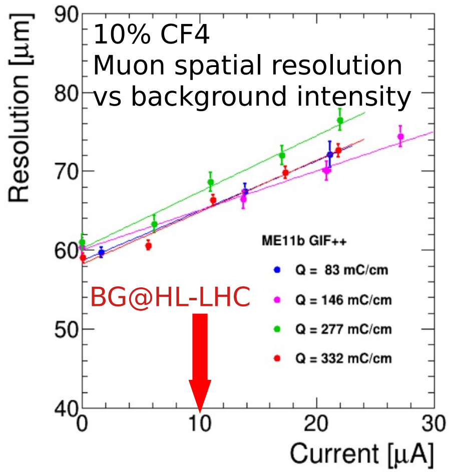
- connecting DCFEBs to OTMB (LS2) and ODBM (LS3)
- ready for installation on station 2,3,4 inner rings (first endcap)

Longevity studies and R&D to reduce CF4 consumption in CSC

Longevity of CSC at HL-LHC

2016-2018 accelerated (factor 25x LHC) irradiation campaign at GIF++ has confirmed that **CSCs operated with the standard gas mixture** Ar(40%)+CO2(50%)+CF4(10%) **survives the dose expected after 3000/fb of integrated luminosity at HL-LHC,** with a safety factor 3. CSC performances (gas gain, spatial resolution, efficiency) are very stable at the highest HL-LHC backgrounds

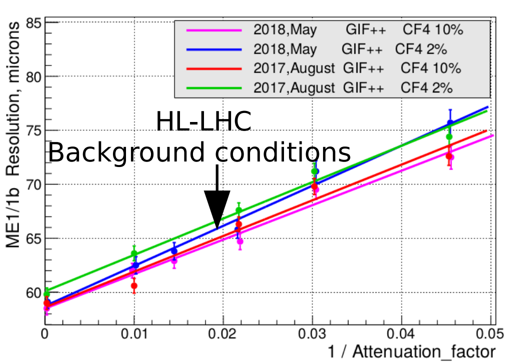


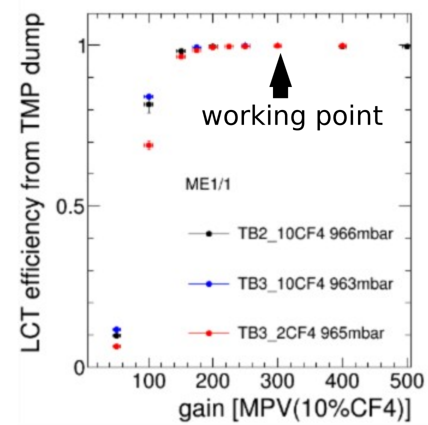


* HL-LHC: 5e34 Hz/cm2

Since 2018, we are performing irradiation and performance tests with **reduced percentages of CF4** in mixture (5% and 2%)

- full area irradiation tests at GIF++ with standard CSC
- localized irradiation at laboratories (CERN, PNPI) with CSC prototypes



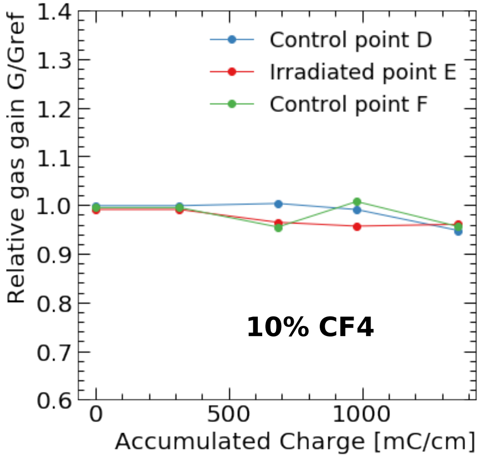


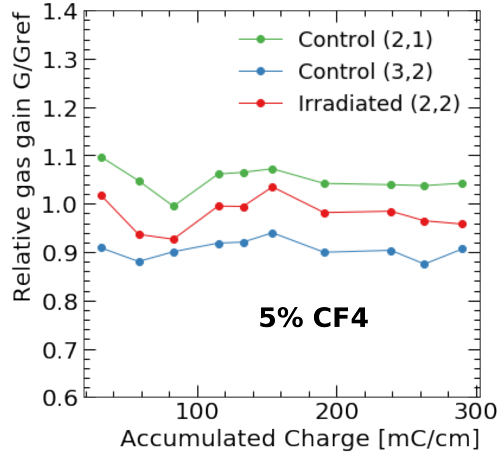
CSC muon spatial resolution as a function of the background intensity and muon trigger efficiency as a function of relative gas gain measured with 10% and 2% CF4 gas mixtures

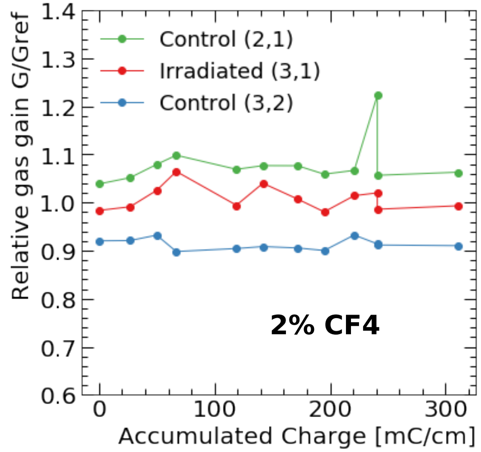
=> Reducing CF_4 content does not affect the CSC muon detection performance

Longevity studies for 10% - 5% - 2% CF_4 mixtures

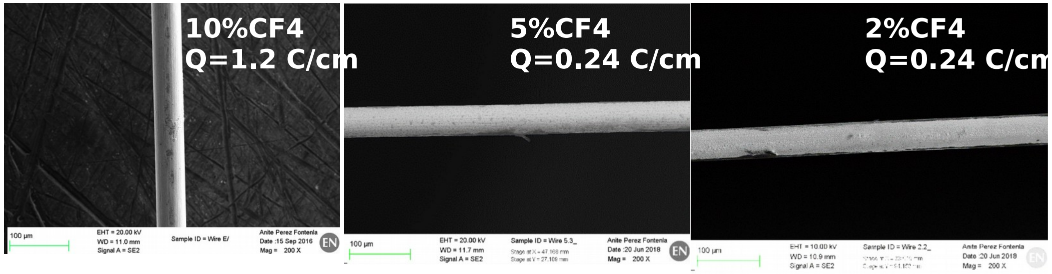
- CSC prototypes survived the large integrated dose and have showed remarkably good operation and performance stability







- Post-irradiation analyses (SEM, EDS) of material aging were performed at CERN, Belgrade, Sarov



Local aging of cathode and anode wire surface is observed, but to an extent that does not prevent stable chamber operation

- A CSC operating gas mixture with a reduced (5%) CF4 fraction seems a viable option to achieve GHG consumption reduction.

- Reducing further the CF4 fraction might not guarantee adequate CSC performance and longevity on a 20 years time scale

R&D on eco-friendly substitutes of CF_4

New gas requirements:

- allows stable CSC operation with existing read-out electronics at comparable HV working point
- guarantees same aging preventing properties as CF_4

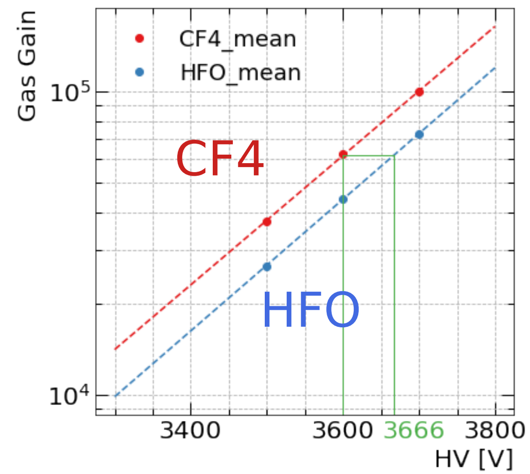
So far CSC prototypes with CF3I (GWP<1) and HFO-1234ze (GWP ~7) were investigated

- CF3I (tested in 2018): too electronegative, not suitable with proportional gas detectors
- HFO (in progress 2019): never studied for MWPC

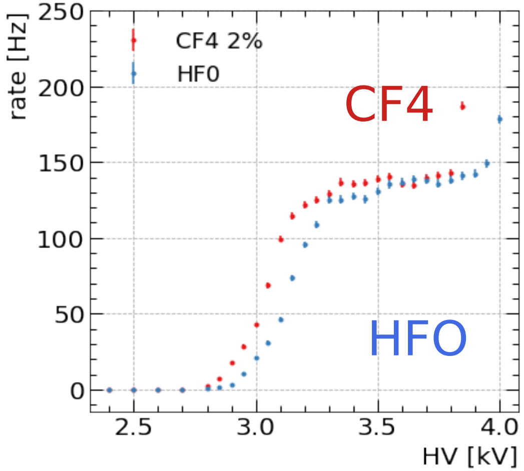
Studies with HFO: 2 prototypes under test (PNPI, CERN)

- Test operability of CSC with Ar+CO_2+HFO at different concentrations
- Characterize parameters (gas gain, working point) and performance (timing, efficiency, resolution)
- Measure aging properties

Preliminary results : CSC performance Ar/CO2/CF4 vs Ar/CO2/HFO-1234ze (40/58/2)



Absolute gas gain as a function of high voltage

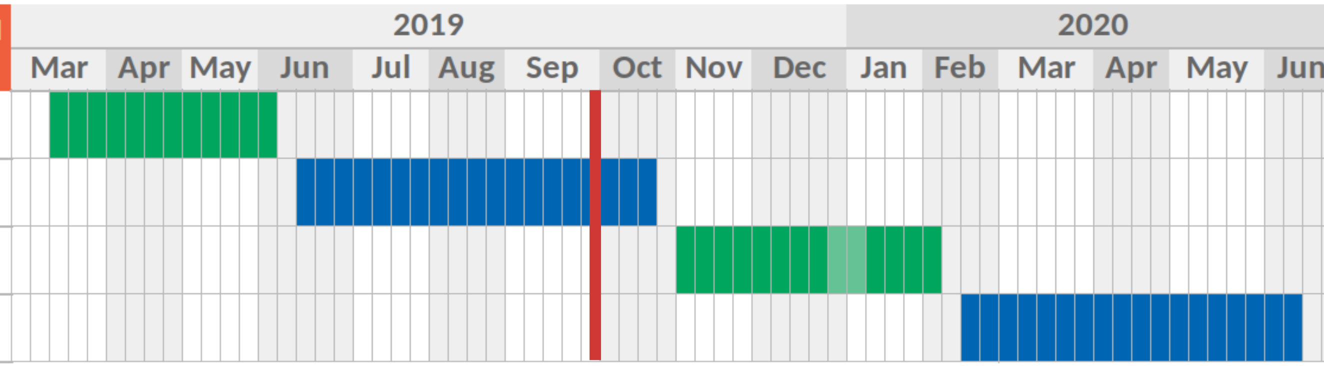


Trigger rates from a Cd source measured for a CSC prototype equipped with the standard CSC electronics.

- Very preliminary studies show reasonable gas gain and detection efficiency (rate at plateau and length of HV plateau)
- Detailed performance studies and longevity tests just started

Workflow of the LS2 upgrade

TASK NAME	START DATE	END DATE	DURATION (WEEKS)
ME-1/1	11 Mar 19	2 Jun 19	12
ME+X/1	10 Jun 19	20 Oct 19	19
ME+1/1	28 Oct 19	2 Feb 20	12
ME-X/1	10 Feb 20	14 Jun 20	18



LS2 schedule includes ~15 months (Mar 2019 – Jun 2020) of continuous work to upgrade electronics of 180 CSCs (33% of the total CSC system)

Working sequence:

- Chambers are extracted and brought to the surface into a CSC lab, classified as “RP supervised area” because of the slight chamber activation
- On-chamber electronics are replaced and new electronics are tested, including cosmic runs
- Chambers are re-installed after a 48h burn-in test
- Re-installed chambers are immediately reconnected to services, validated and commissioned using final DAQ

Experience so far

Issues encountered and solved:

- Fabrication of boards cooling covers because of long lead time for copper
- Test setup (CTP7 board and uTCA crate) and procedure to fuse GBTx parameters on xDCFEBs
- Logistics issues to rework boards (DCFEBs) with low activity level (< 0.1 µSv/h) in designated labs
  - RP measurements, tracking, and transports are time consuming
- Risks of collateral damage to ME1/1 on-chamber services (cooling) during refurbishment
  - leak detected on one of the circuits which required careful evaluation of future potential risks to CMS
    - → strategy in place to minimize short-term risks (improved procedure and water leak detection)
    - → long term mitigation: manufacture new on-chamber cooling circuits with improved design