Imperial College London

Design Challenges of the CMS High Granularity Calorimeter Level 1 Trigger

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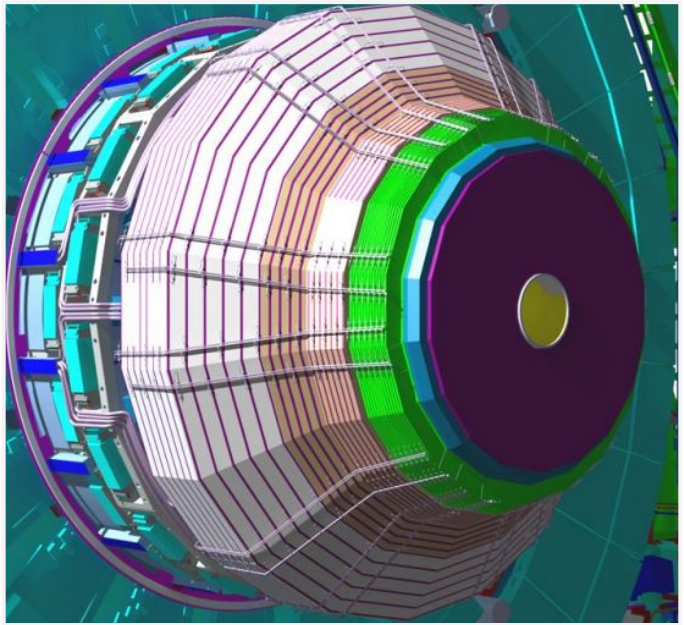
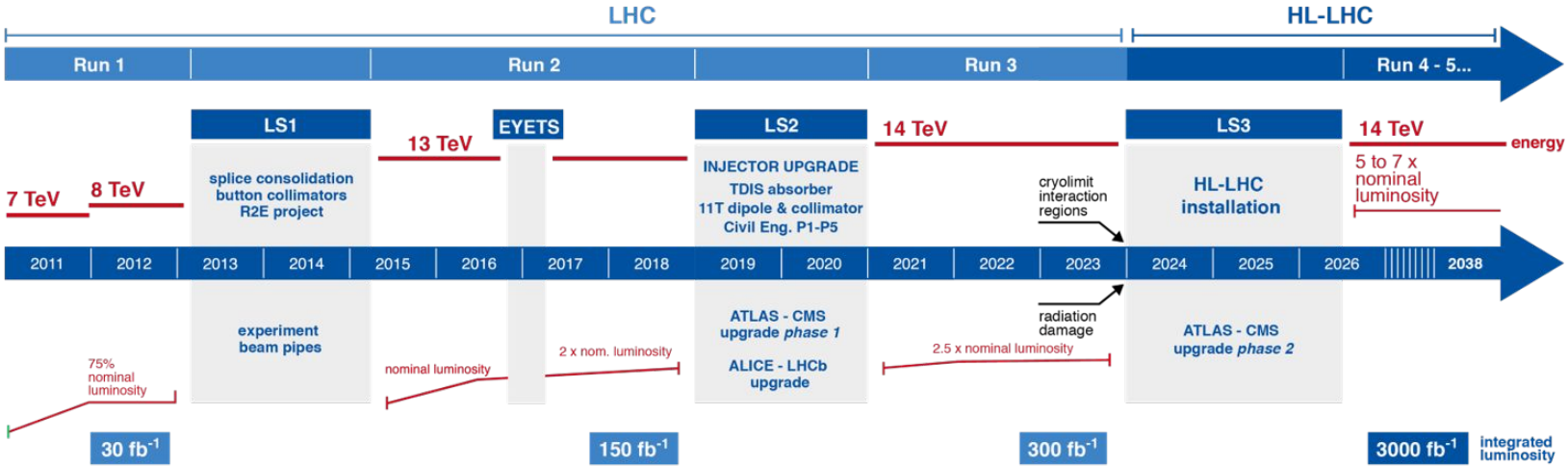


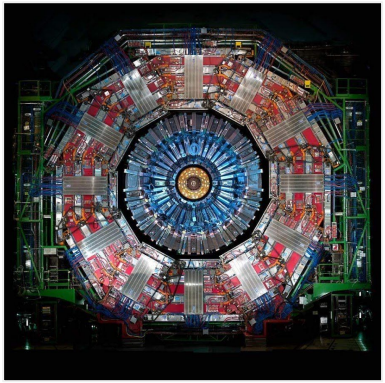
HL-LHC

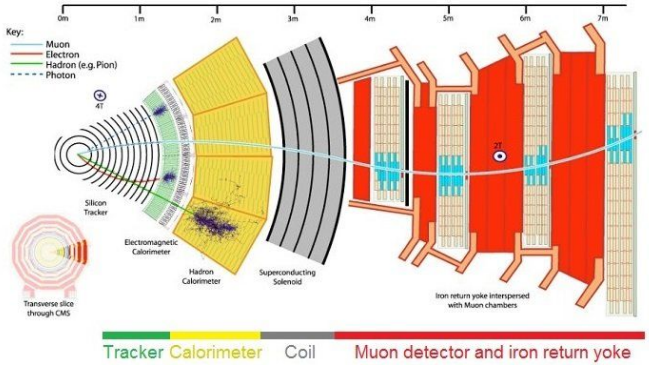
- The high luminosity large hadron collider (HL-LHC) project is a major upgrade of the current collider.
- HL-LHC will probe Nature for evidence of “new physics” (NP).
- First beam: mid-2026.
- HL-LHC luminosity increase: from ~2×10^{34} to 5-7×10^{34} cm^{-2} s^{-1}.
- Pile up (PU) increase from ~50 up to 140-200 interactions per bunch crossing (BX).

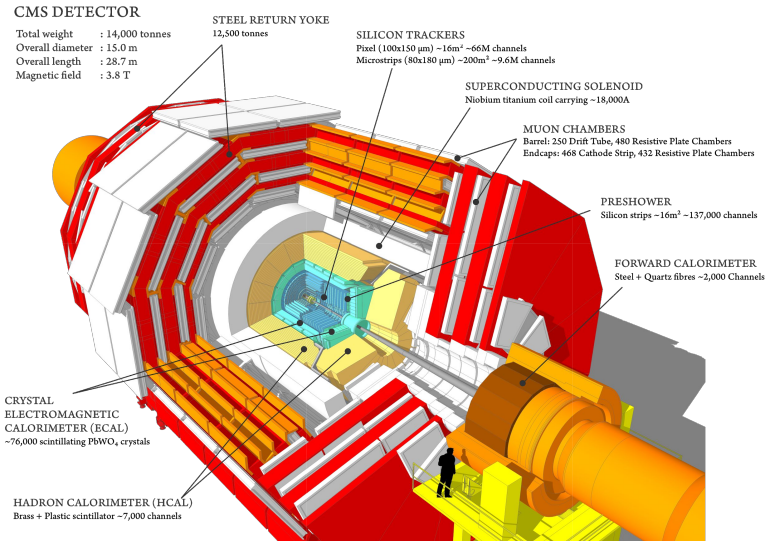


The CMS Experiment

- The compact muon solenoid (CMS) experiment is a general purpose experiment designed for a broad physics programme.
- Major CMS upgrade planned for HL-LHC.
- Main Level 1 trigger changes:
  - Rate: from 100 to 750 kHz
  - Latency: from 4 to 12.5 μs

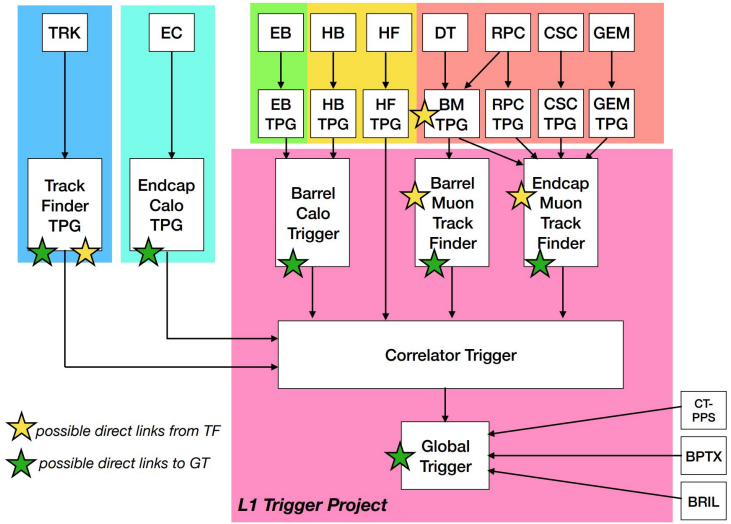


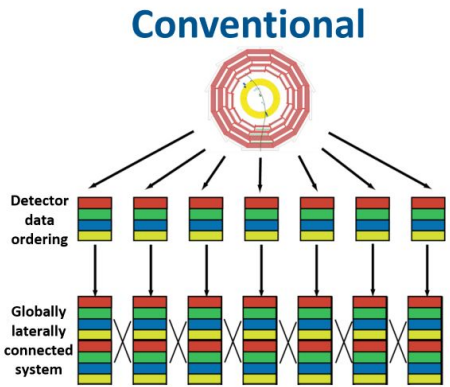


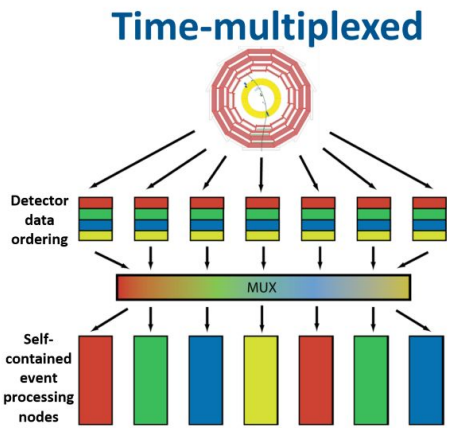


The Level 1 Trigger

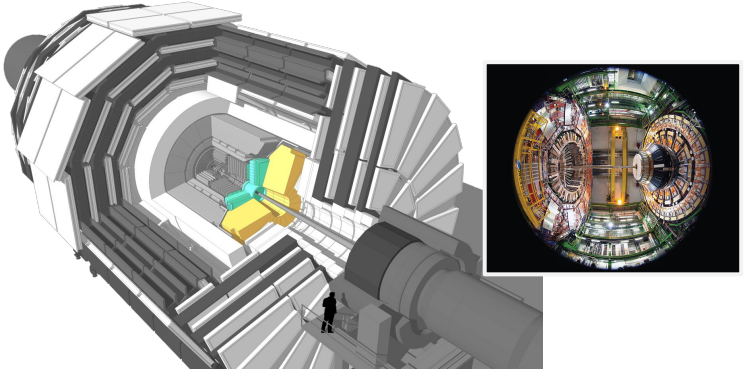
- Level 1 divided into two steps: trigger primitive generation (TPG) and correlator.
- The L1 trigger will implement a so-called time multiplex (TMUX) architecture.
- TMUX allows a boundary reduction and helps to collect data from a single bunch crossing into a single processing unit.







The HGCAL



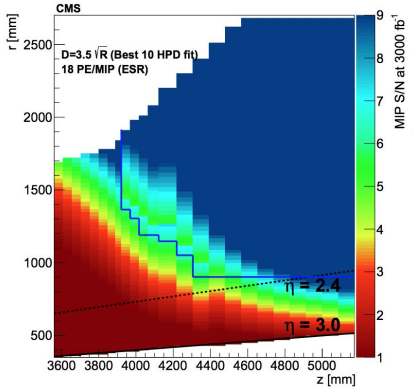
- The HGCAL has been indicated as solution to confront the increase in radiation dose and pile up (PU) for the endcap regions (TDR ‘18).
- Narrow VBF jets and jets with substructure are expected to be a signature for NP.
- Electromagnetic Section (CE-E):
  - 28 layers (Si-only)
  - CuW+Cu+Pb absorber
  - 25 X_0
  - 1.3 λ_0
- Hadronic Section (CE-H):
  - 22 layers (Si-only + Si-Scint)
  - Stainless Steel absorber
  - 8.5 λ_0

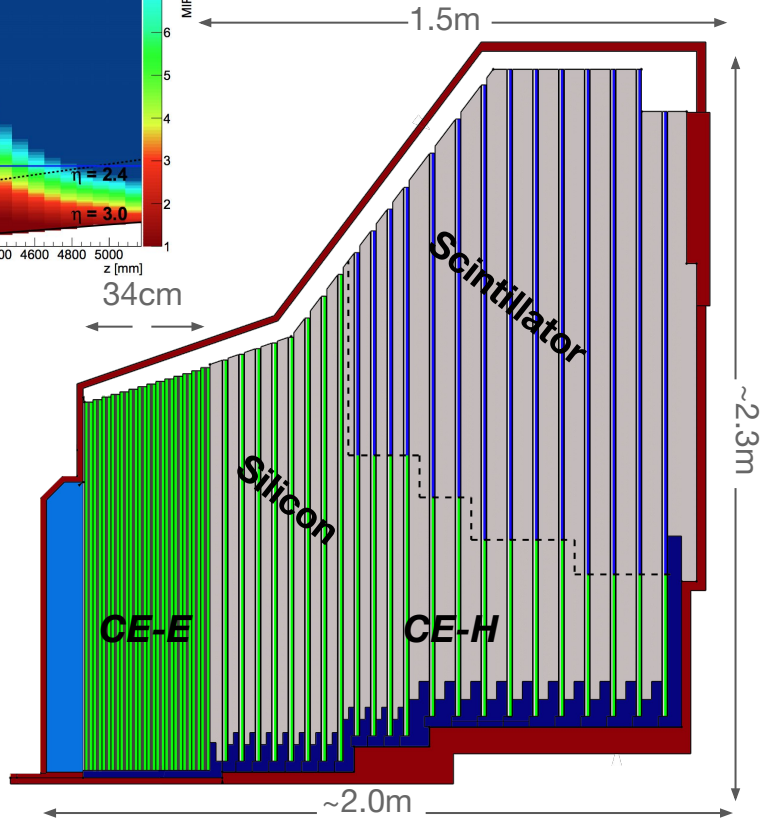
Current design (2 x EC)	*CE-E (Si)*	*CE-H (Si)*	*CE-H (Scint)*
Area (m^2)	~165	~1250	~200
Channels (k)	~2000	~2000	~200
Modules (Si/Tileboards)	~8000	~4500	~2000
Weight (t)	~20	~200	
Si-only Planes	28	8	
Si-Scint Mixed Planes	-	14	

*CERN-LHCC-2017-023.

The HGCAL

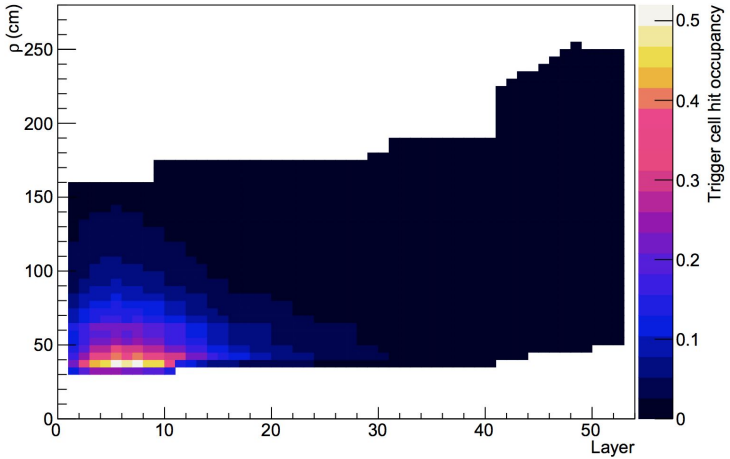
- Radiation tolerance:
  - Si-only planes in the *high* radiation region,
  - Scint+SiPM in the *low* radiation region ➛ hybrid planes in downstream half of HGCA
  - Active cooling at -30 ºC (~120 kW/endcap).
- Lateral shower confinement: dense calorimeter absorber.
- Adjacent shower separation: fine lateral granularity (two cell sizes 0.5 and 1.2 cm^2).
- PU rejection, PID and energy resolution: fine longitudinal granularity (50 layers).
- PU energy rejection: good time resolution (25 ps).

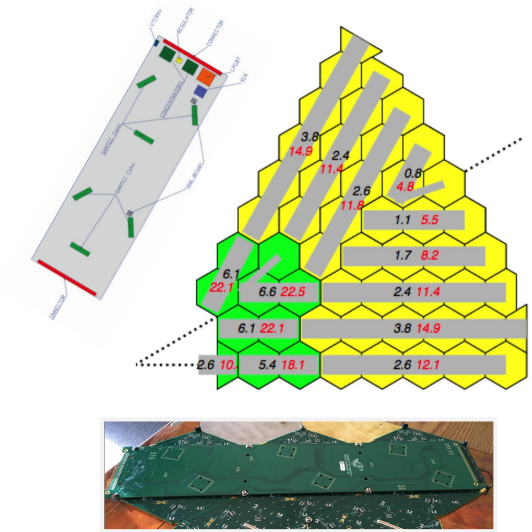


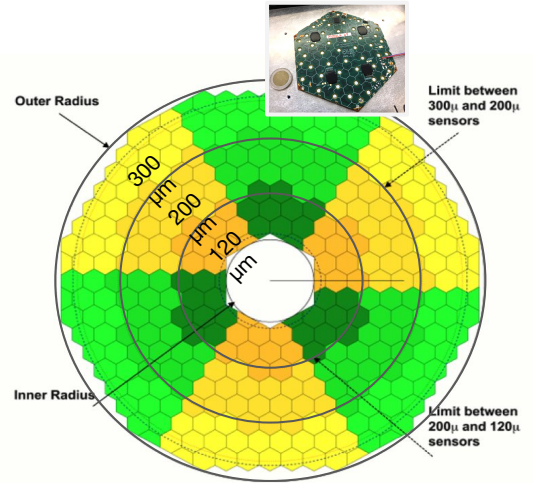


HGCAL Electronics Structure

- Silicon wafers and scintillator tiles hosted by motherboards.
- Motherboards provide all the connectivity to the back-end.
- Hi bandwidth variability in r and z.
- The number of elements per motherboard is variable in order to adapt to the region occupancy.



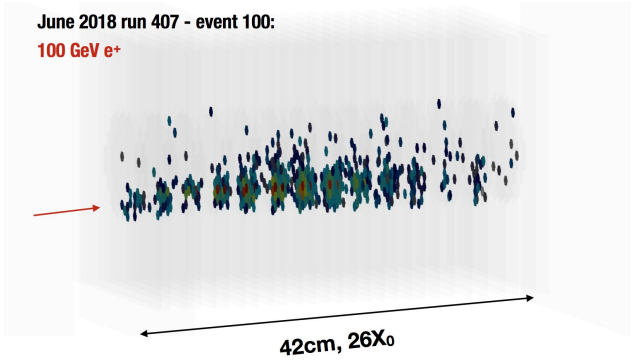


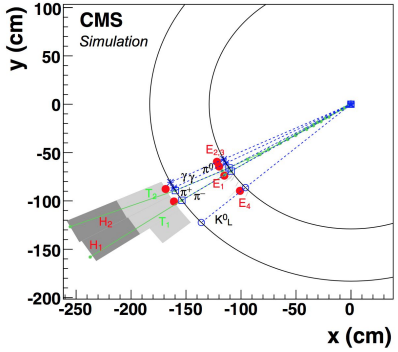


Physics Motivation for HGCAL Trigger

- Trigger capabilities in the forward region will be a key feature of the CMS detector during its Phase-2.
- The HGCAL will generate trigger primitives (TP) relying on its high granularity.
- TP will be a set of 3D clusters for each bunch crossing.
- These clusters will be combined with the other TPs from other detectors in the central Level 1 trigger to implement particle flow algorithms at trigger level.

Real event (test beam)





Particle flow example event

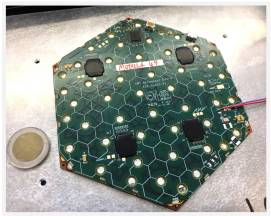
From the Front End Electronics to the TPG

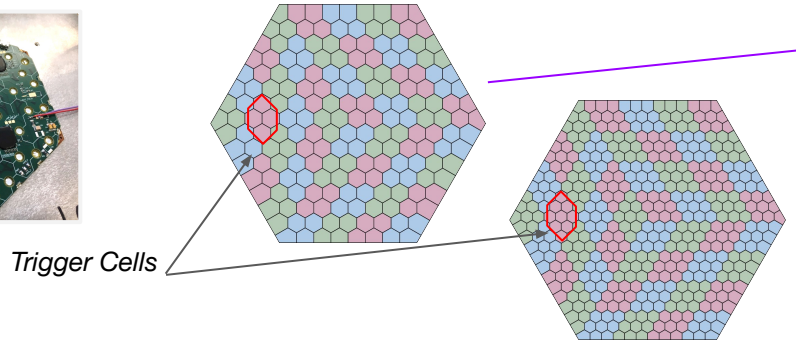
- The trigger primitive generator (TPG) will receive data from the front-end (FE) electronics via 100 m long fiber bundles.
- Links will be implemented via the radiation-hard low power gigabit transceiver (lpGBT*), that is part of the CERN ‘versatile link+’ project (VL+).
- Each link will implement a FEC5 protocol over a 10 Gpbs link speed (8.96 Gpbs usable for data transmission).
- Trigger data will be sent to the TPG with a latency of 50 BX (1.25 μs) and a window of 12 BX.

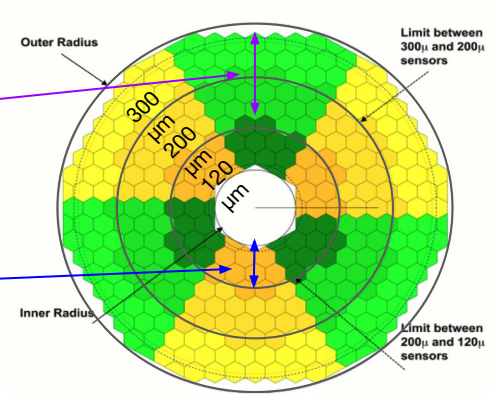
*https://espace.cern.ch/GBT-Project/LpGBT/Specifications/LpGbtxSpecifications.pdf

The HGCAL Trigger Primitive Generator

- Bandwidth is an expensive element of the system.
- There will be O(10000) links @10 Gbps (~100 Tbps) from the FE to the TPG.
- Required bandwidth per wafer varies by more than one order of magnitude over different regions.
- Balancing bandwidth minimization and physics requirements has been carefully studied.

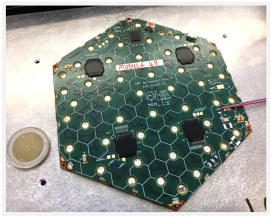


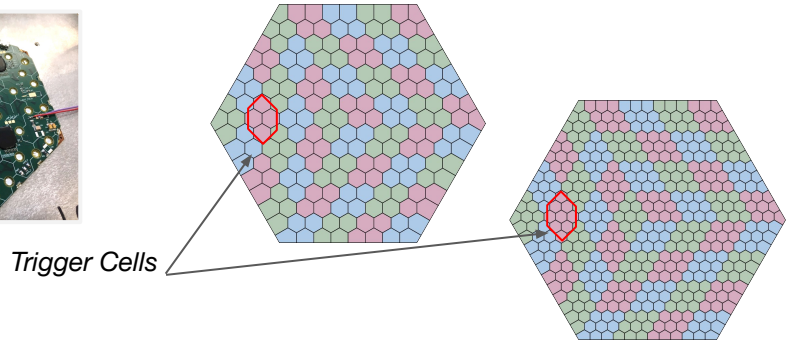


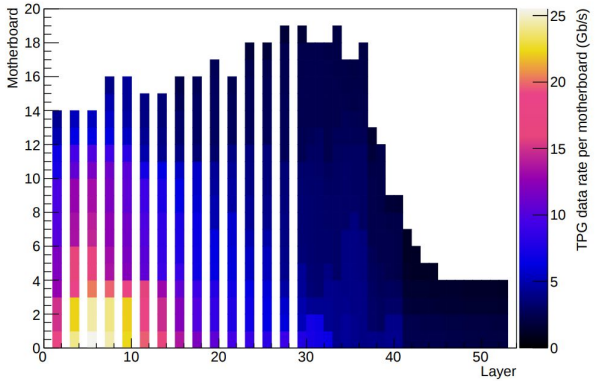


The Bandwidth Challenge

- In order to reduce the bandwidth to the TPG:
  - The electromagnetic region is readout every other layer.
  - The data are read out at reduced granularity (9 or 4 times coarser, radius dependent).
  - No timing cell information is readout.
  - Threshold applied in FE to limit number of trigger cells read out.
  - FE buffering and variable data volume → possible overflows.

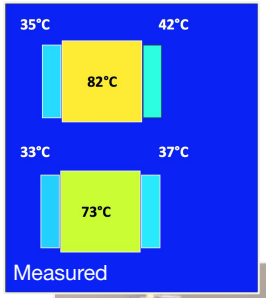


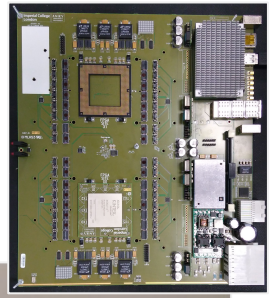


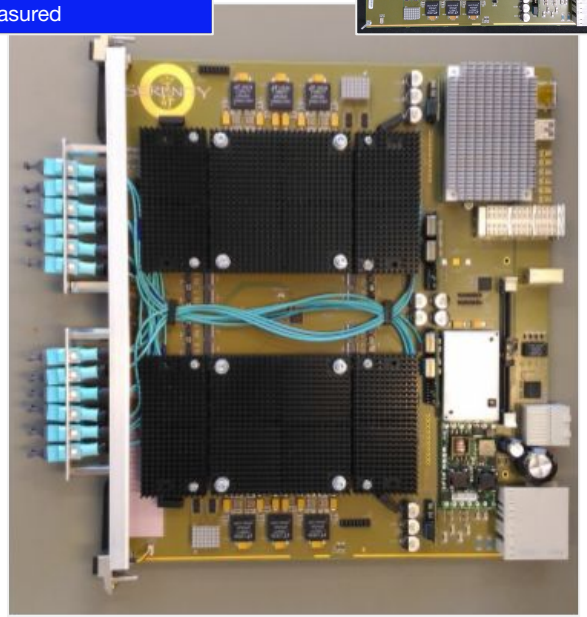


The Serenity Platform

- ATCA standard.
- Generic motherboard common to other subsystems.
  - Exchangeable FPGAs on daughterboards ➛ versatile + cost reduction.
  - Up to 72 in and 72 out links (link speed up to 28 Gpbs).
  - Optical links are implemented using FireFly™ Micro Flyover System™ (Samtec).
- Board control is provided by an industry standard COM Express mounted directly on-board running CentOS 7.
- Wide commissioning campaign started to ensure reliability and system robustness:
  - Temperature stress.
  - Optical modules reliability.
  - Ageing tests.

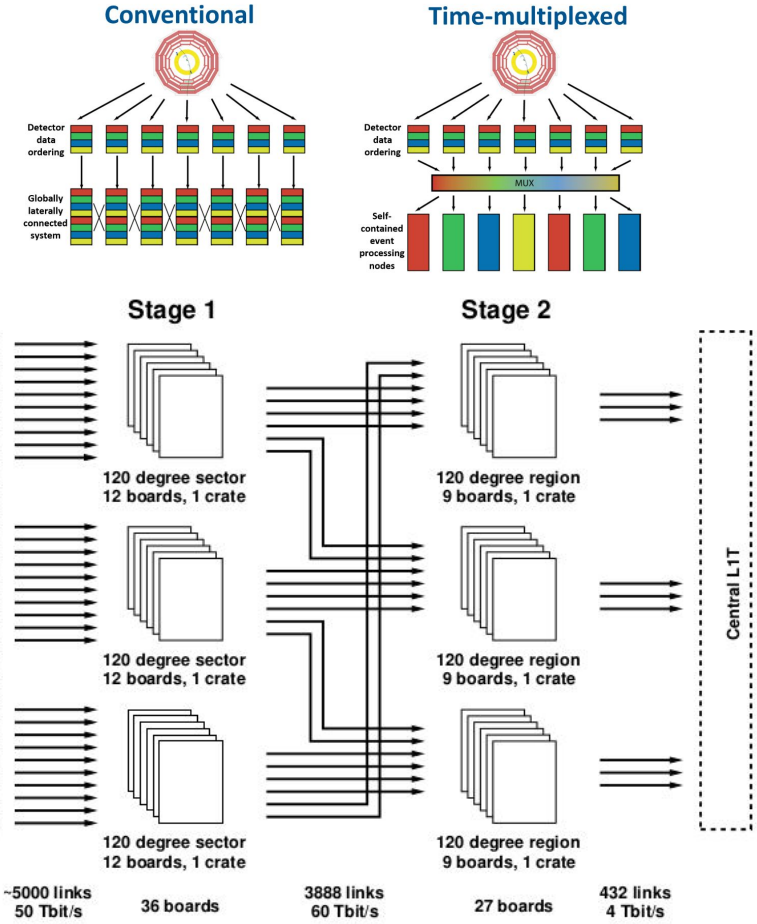






The HGCAL Level 1 Trigger

- TPG design will use a two stage design.
- The TPG will implement time-multiplex (TMUX) architecture.
- Every Stage 2 FPGA will receive data from a wide region (120º) of the detector and will have a TMUX-period to process them (currently 18 BX).
- TMUX reduces the number of region boundaries which would need prohibitive duplicated data bandwidth.



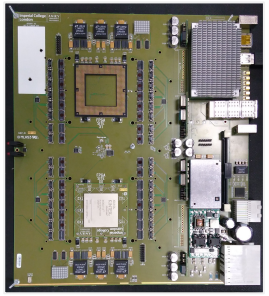
Latencies

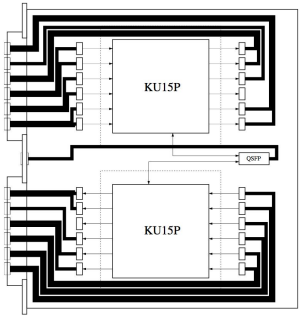
- The latency is a major constraint for the system.
- Total latency for a trigger decision is limited by the on detector data buffers: 12.5 μs.
- This is includes the whole path from collision to trigger signal distribution to the FE.
- TPG will need to deliver the primitives to the central Level 1 trigger within 5 μs.
- Require latency for Stage 1 + Stage 2 ≦ 2.825 μs (113 BX).

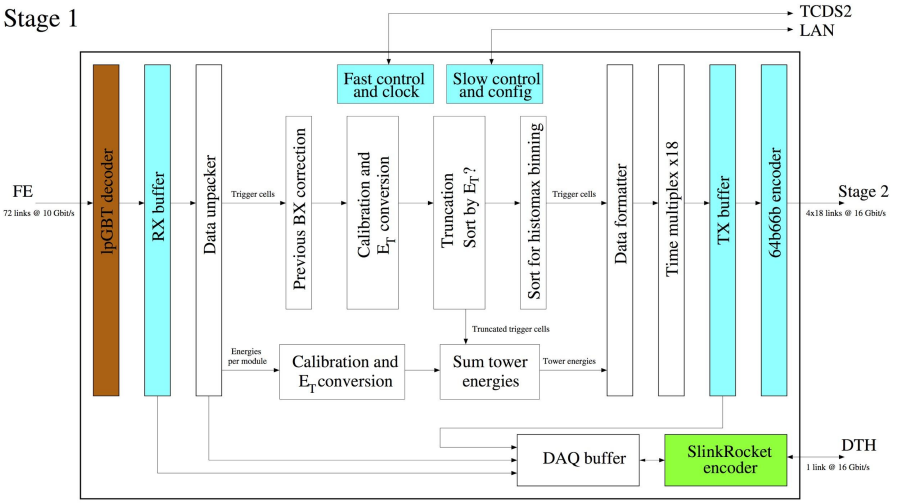
Location	Component	Latency (ns / BX)
On detector	FE ASIC (HGCROC)	400 / 16
	Concentrator ASIC	575 / 23
	SerDes to TPG	600 / 24
Off detector	SerDes to Stage 2	150 / 6
	Stage 2 TMUX	450 / 18
	Serdes to central L1T	150 / 6
	Stage 1 + Stage 2	≦ **2825 / 113**
Total		5000 / 200

TPG Stage 1

- This stage provides:
  - Calibration is applied.
  - Corrections due to high charge deposit on previous BX are also implemented.
  - TMUX is implemented (x18 BX).
- Mounting Xintex KU15P FPGAs daughter cards (DC):
  - 72 links from the FE electronics
  - 54 links to each Stage 2 FPGA: 3 links to each Stage 2 board.
  - Firmware core provided by the Serenity community and 3rd parties (colored).
  - HGCAL specific firmware needs implementation.

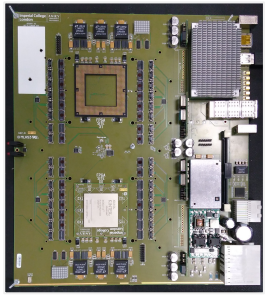


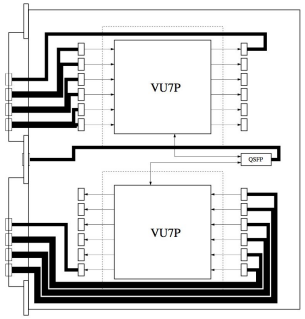


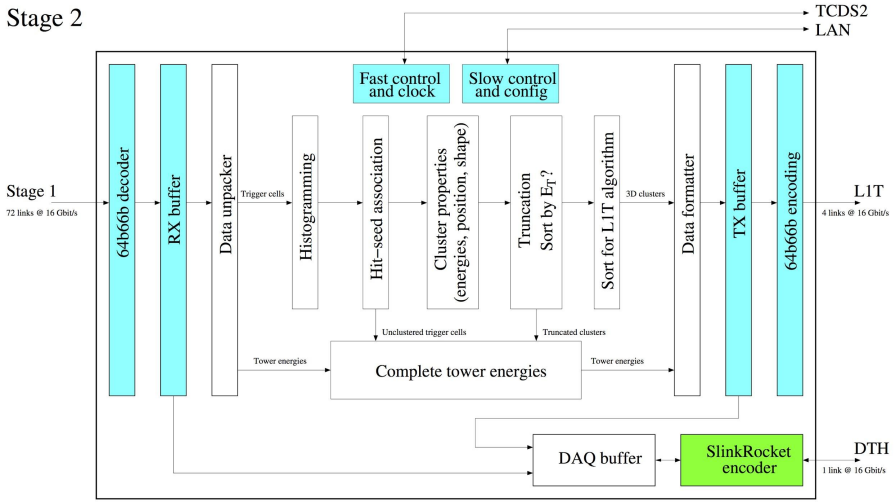


TPG Stage 2

- The Stage 2 main goal is to generate the trigger primitives from the calibrated high granularity trigger cells.
- Mounting Xilinx VU7P FPGAs DC → more logic than those mounted on Stage 1.
- Each FPGA is collecting and processing data from a 120° detector sector and for all layers.
- The TMUX ensures that each processing FPGA will deal with data from the same BX for the whole TMUX period of 18 BX (450 ns).
- Collecting all the data into a single FPGA is a design choice made in order to keep the system flexible for possible future algorithm evolution.

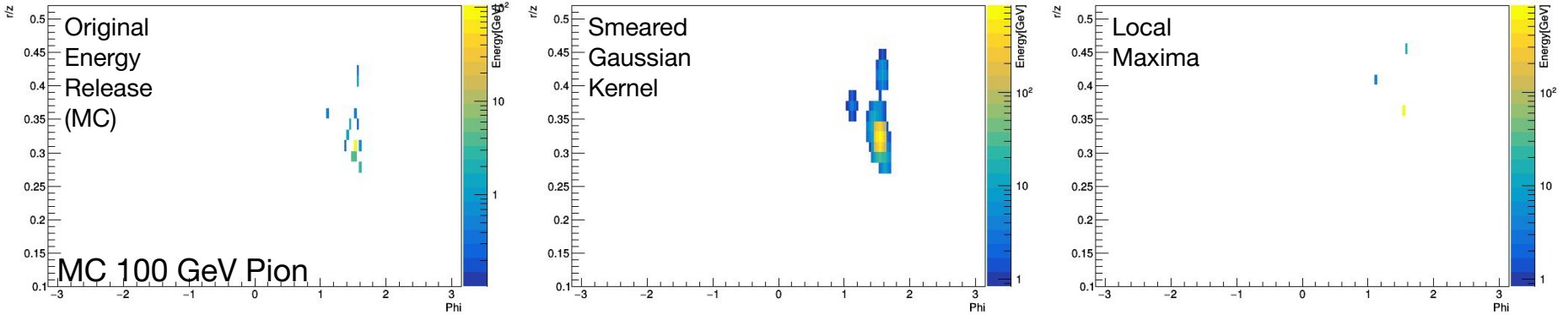






Stage 2 Current Baseline Algorithm

- In order to minimise the latency the algorithm is fully pipelined.
- The Stage 2 Algorithm is made of two main steps.
  - *Step1*: 3D clusters are seeded using the whole dataset. Seeds are build from a projective histogram. Each bin is the energy sum of all the trigger cells whose coordinates are within the bin. Seeds are defined by local maxima after Gaussian smearing.
  - *Step 2*: clusters are built around each seed. The trigger cells are compared with all the seeds and added to the cluster if falling within a programmable radius.



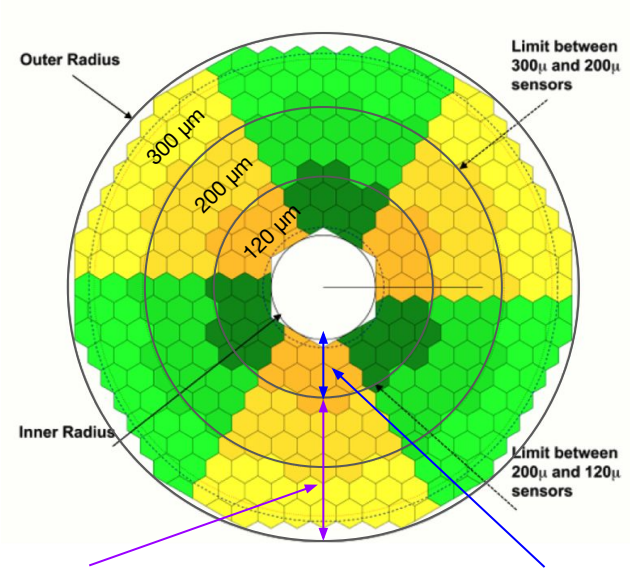
Conclusions

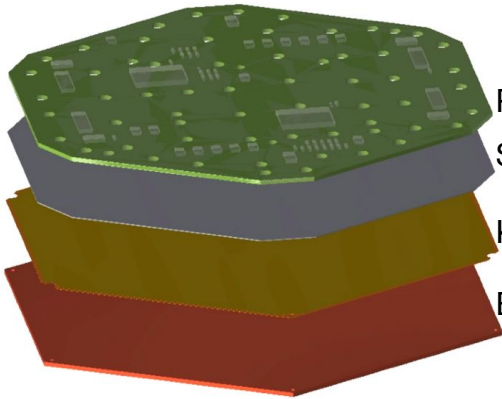
- The combined increase in detector granularity and LHC luminosity have set new challenges for the trigger processor of the novel High Granularity Calorimeter.
- A careful study of the trigger path and algorithms is underway.
- Tailored resources have been an important factor in order to reduce costs and allow a more uniform use of the bandwidth and FPGA logic.
- The current baseline for both hardware and firmware has been presented.
- The first release of the hardware is currently under test.
- The firmware implementation of both Stage 1 and Stage 2 has started.

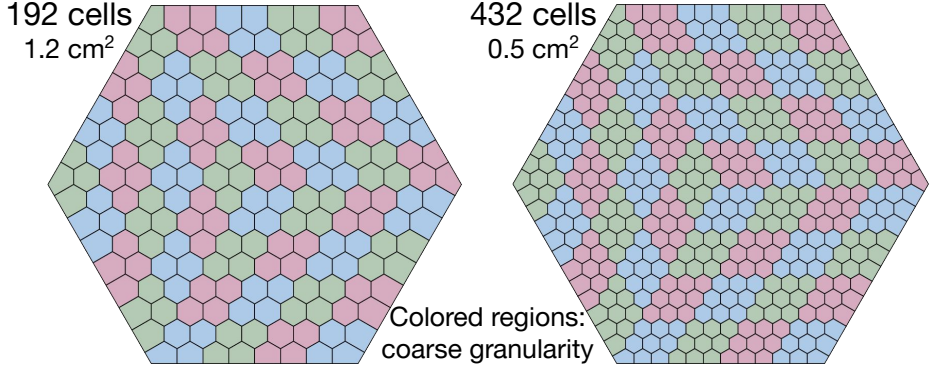
Backup

Silicon Modules

- Basic hexagonal blocks from 8'' diameter silicon wafers.
- Sensor's *thickness* and *active cell size* are η dependent: radiation damage minimization, better shower separation in the high occupancy region.

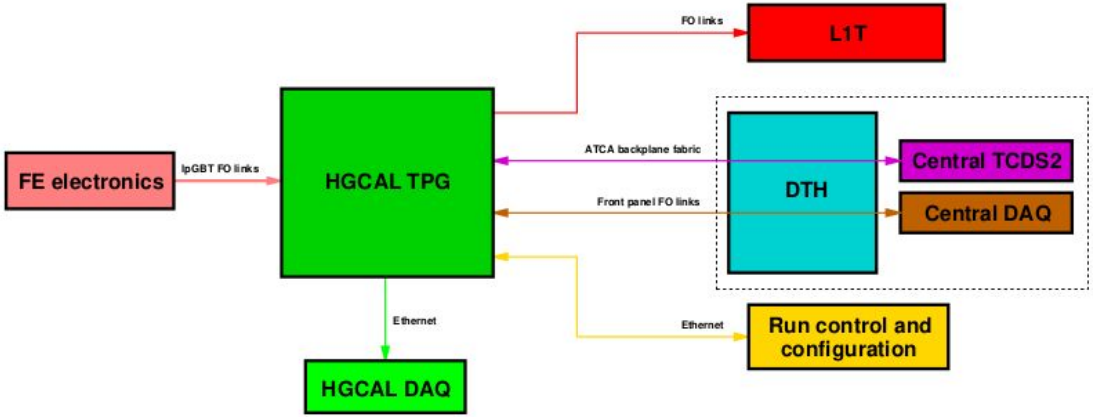






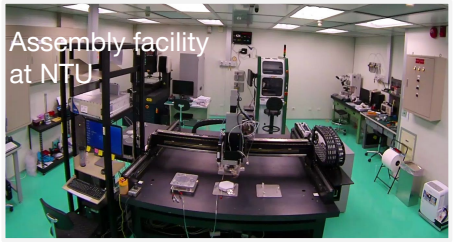
The HGCAL Whole Picture

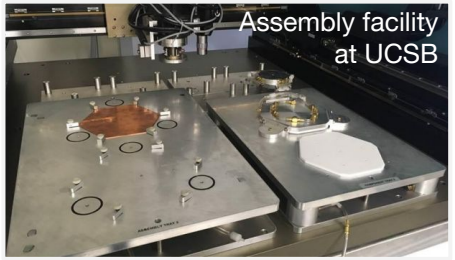
- HGCAL TPG will have different interfaces towards several subsystems.
- In parallel to the main path FE→TPG→L1T we do need to:
  - Interact with the DAQ in order to
  - Send debug data to the central DAQ and receive timing information from the TCDS.
  - Get control and configuration data.

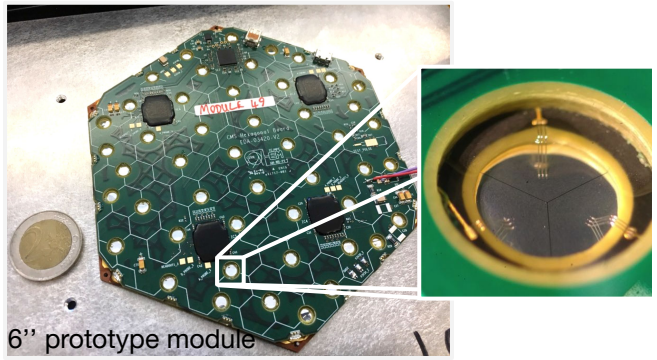


Silicon Modules

- Preparation for full scale production undergoing at the Module Assembly Centres:
  - China (Beijing IHEP),
  - India (Mumbai BARC),
  - Taiwan (Chungli NCU/Taipei NTU),
  - USA (Carnegie-Mellon, Texas Tech., UCSB).
  - ~100 modules produced for test beam purposes.
- Sensors wire bonded to PCB through large holes.
- Thermo-mechanical studies are performed in order to ensure robustness during repeated thermal cycles (-30 to +40 °C).

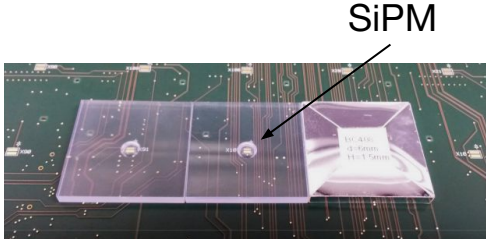


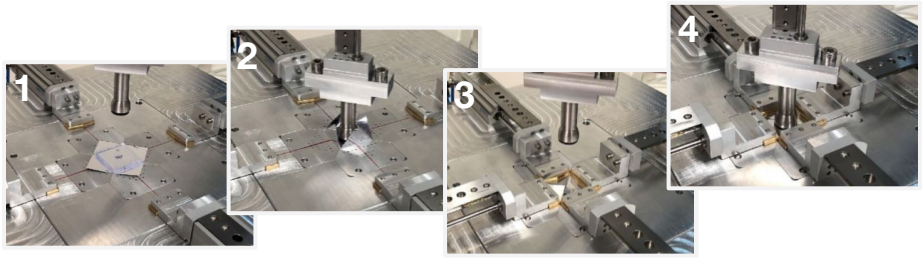




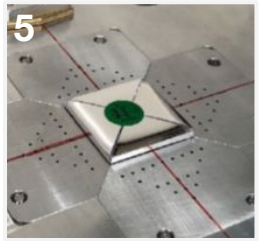
Scintillator Modules

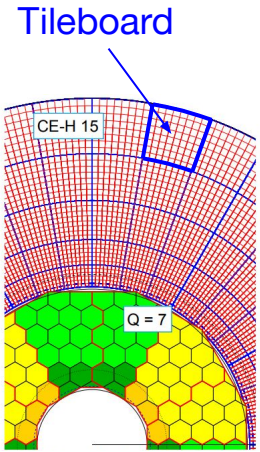
- Plastic scintillator tiles arranged in r-ϕ grid.
- Tile surface varies from 4 to 32 cm^2 (from small to large r).
- Readout is performed by on-tile SiPM.
- Tiles grouped in tileboards with max dimension of 45×41 cm^2.
- Tile Assembly Centres:
  - US (FNAL)
  - Germany (DESY)

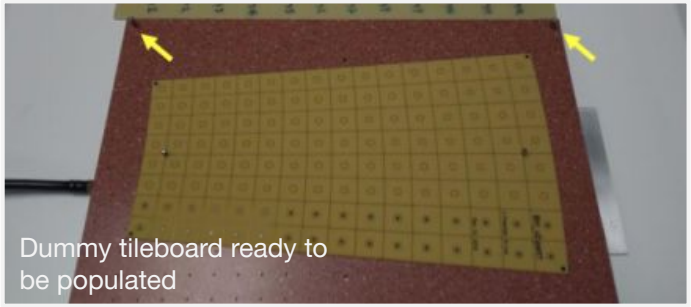




1. Tile+Foil placement
2. Foil creased
3. Foil folded on top of tile
4. Foil securely wrapping tile
5. Wrapped tile

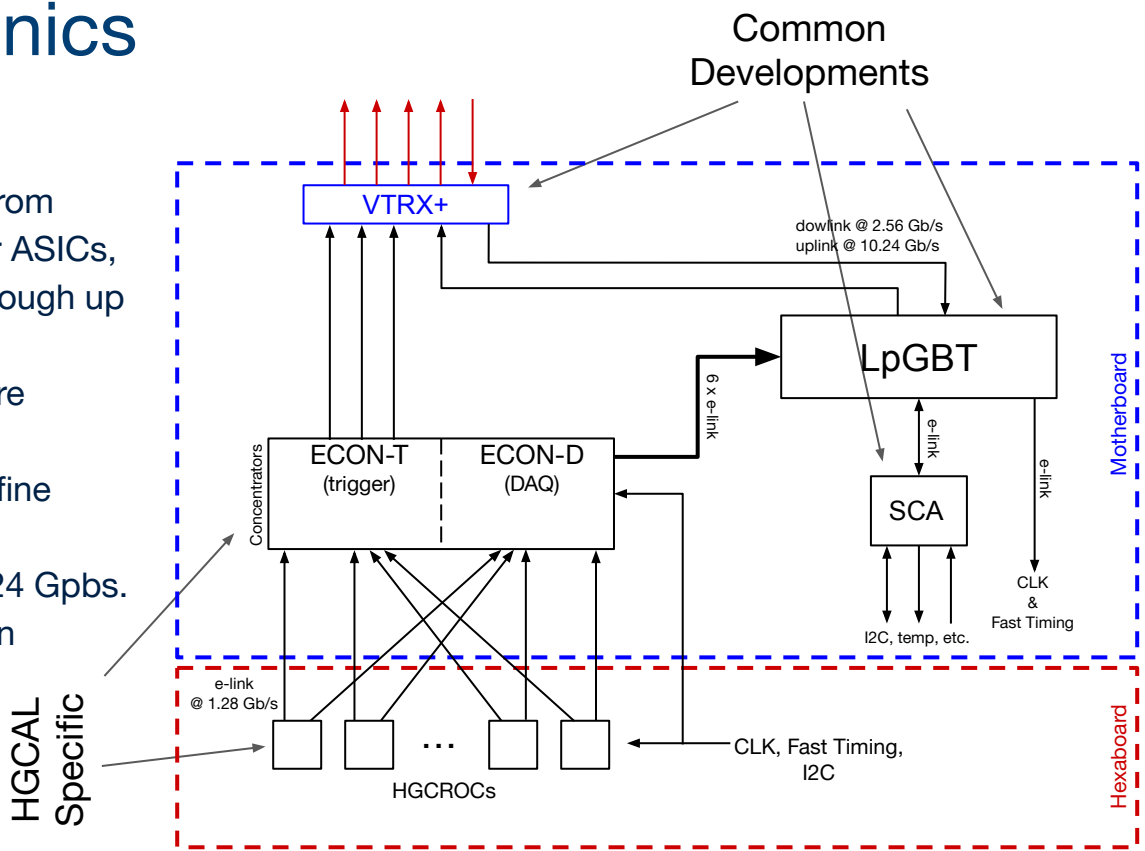






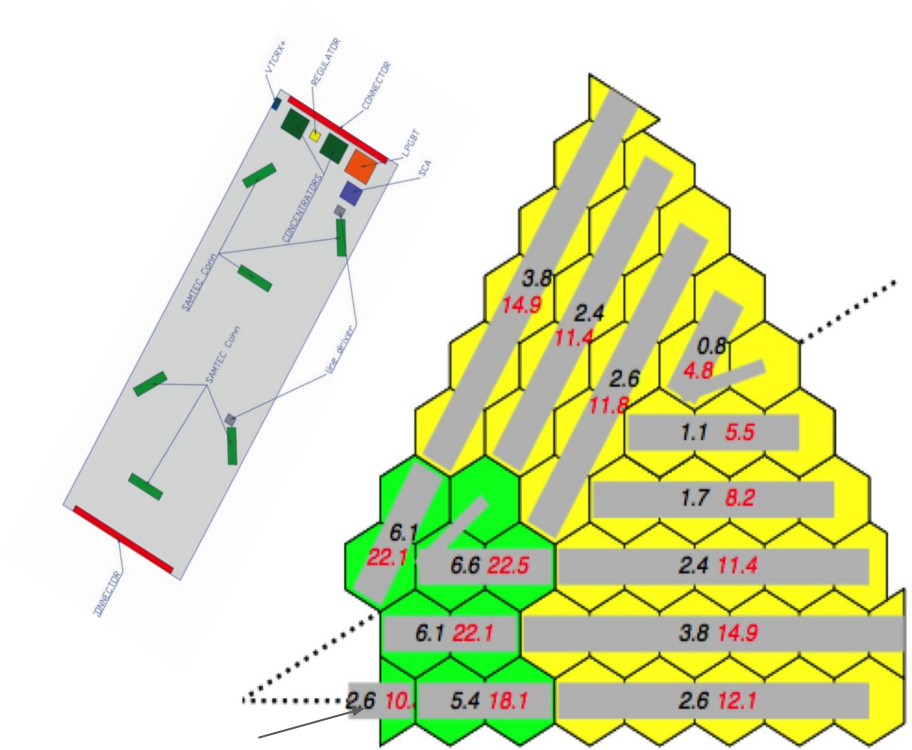
On-detector Electronics

- Bunch Crossing synchronous data from hexaboards are sent to concentrator ASICs, mounted on ‘motherboard’ PCB, through up to 36 e-links at 1.28 Gbps.
- ECON-T will select trigger data before transmitting to the Back-End.
- ECON-D will send zero suppressed fine granularity data to DAQ.
- DAQ path sent via lpGBT link at 10.24 Gpbs.
- *lpGBT*, *VTRX+* and *SCA* are common developments.



Motherboard

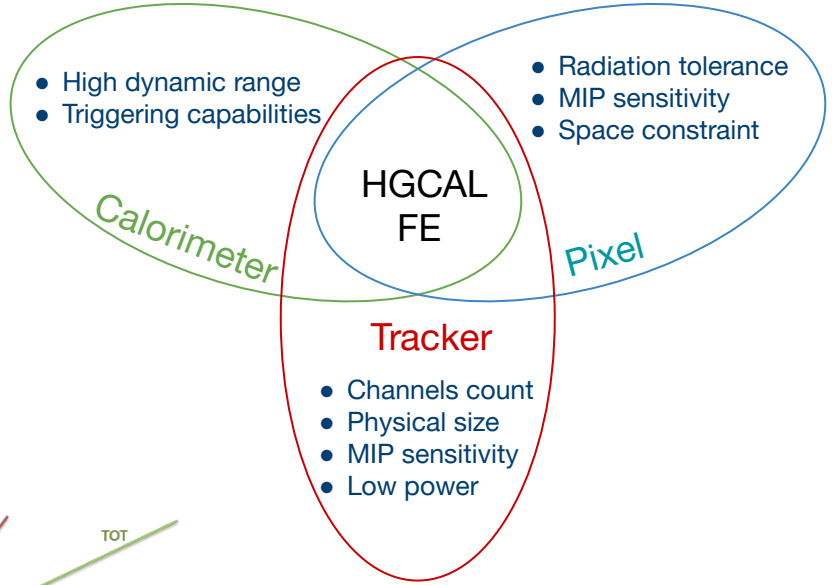
- Motherboards will host the ECONs and the transceivers to the off-detector electronics.
- Bandwidth to off-detector electronics is highly cost constrained.
- Up to 3 ×10 Gbps links to the off-detector electronics:
  - 1 for DAQ
  - Up to 3 for Trigger
- Geometry needs optimization to minimise link count.

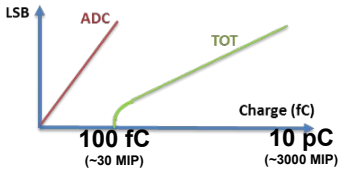


Average Bandwidth for data and trigger (in Gbs)

Front End Electronics: HGCROC ASIC

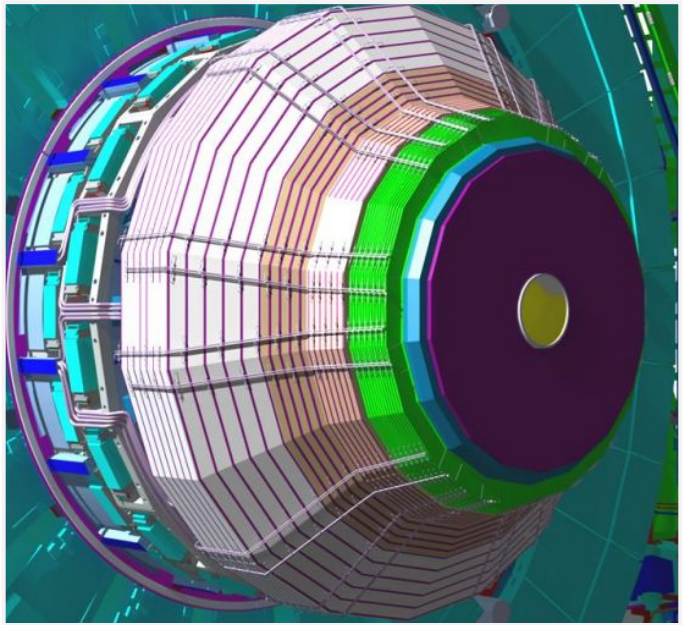
- Two different input stages for Si and Scint.
- Final version of the final HGROC chip expected in early-2021.
- High dynamic range: from 0.2 fC to 10 pC.
- 10-bit ADC + ToT (12-bit TDC).
- ToA:
  - Available for deposits above 10-15 fC,
  - 10-bit TDC, step < 25ps range up to 25 ns,
  - Precision for hit ≤100 ps, and ~30 ps for showers.
- Low power: ≤ 15 mW/channel.
- High radiation environment: up to 2 MGy and a fluence of 10^{16}.
- Technology: CMOS 130 nm.





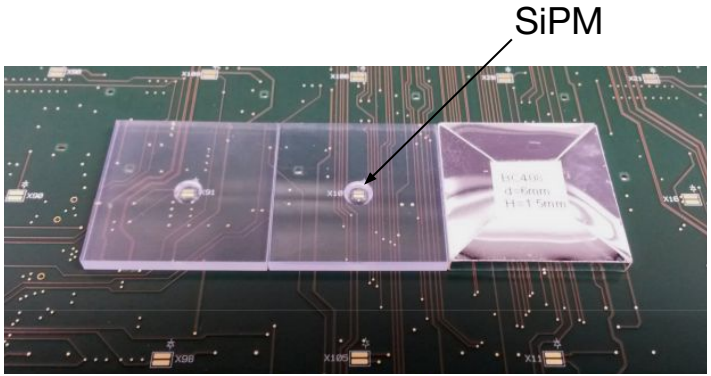
The HGCAL Roadmap

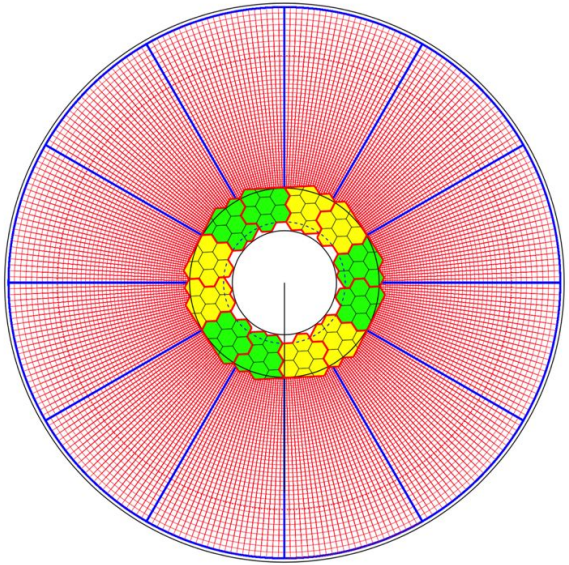
- HGCAL adopted by CMS in 2015.
- First prototype modules produced and tested in 2016.
- TDR submitted in 2017 and approved in 2018.
- Mass construction due to start ~2021.
- Installation foreseen during LS3 (2024-2025), for operation in Run4 (starting in 2026).



Scintillator Modules

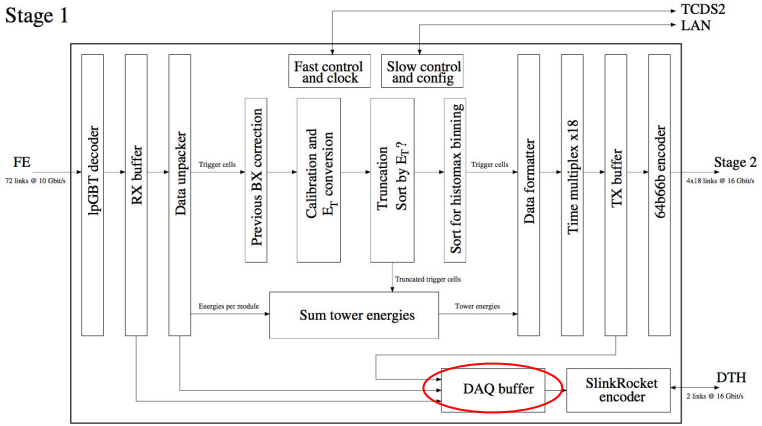
- Plastic scintillator tiles arranged in r-ϕ grid.
- Tile surface varies from 4 to 32 cm^2 (from small to large r).
- Readout is performed by on-tile SiPM.
- Tiles grouped in tileboards with max dimension of 45×41 cm^2.

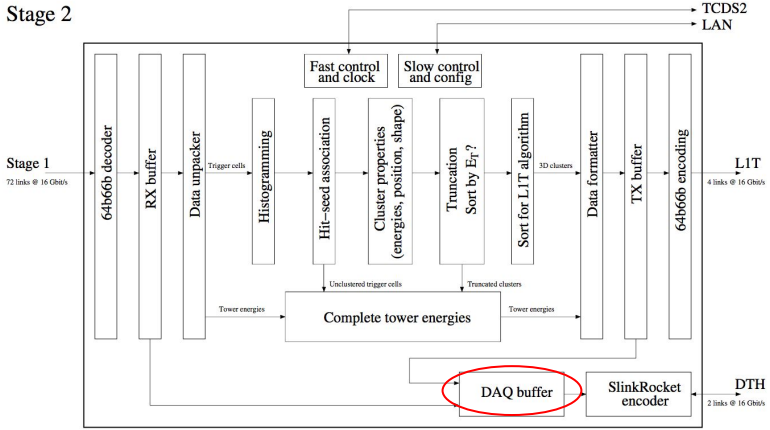




TPG Monitoring

- In order to monitor the trigger quality we have foreseen a debug path.
- Dowscaled trigger data (1kHz???) are sent to the central DAQ where they are processed offline and compared to the actuall trigger decision.





CMS

CMS DETECTOR

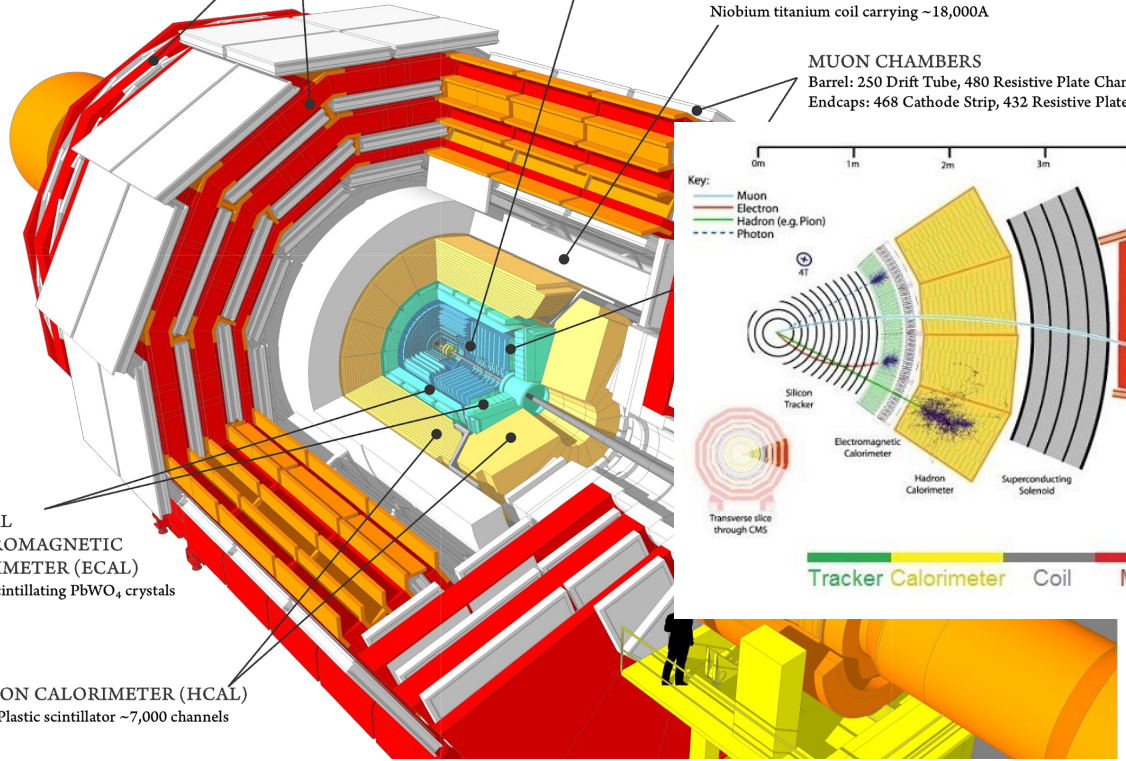
Total weight : 14,000 tonnes
Overall diameter : 15.0 m
Overall length : 28.7 m
Magnetic field : 3.8 T

STEEL RETURN YOKE
12,500 tonnes

SILICON TRACKERS
Pixel (100x150 μm) ~16m² ~66M channels
Microstrips (80x180 μm) ~200m² ~9.6M channels

SUPERCONDUCTING SOLENOID
Niobium titanium coil carrying ~18,000A

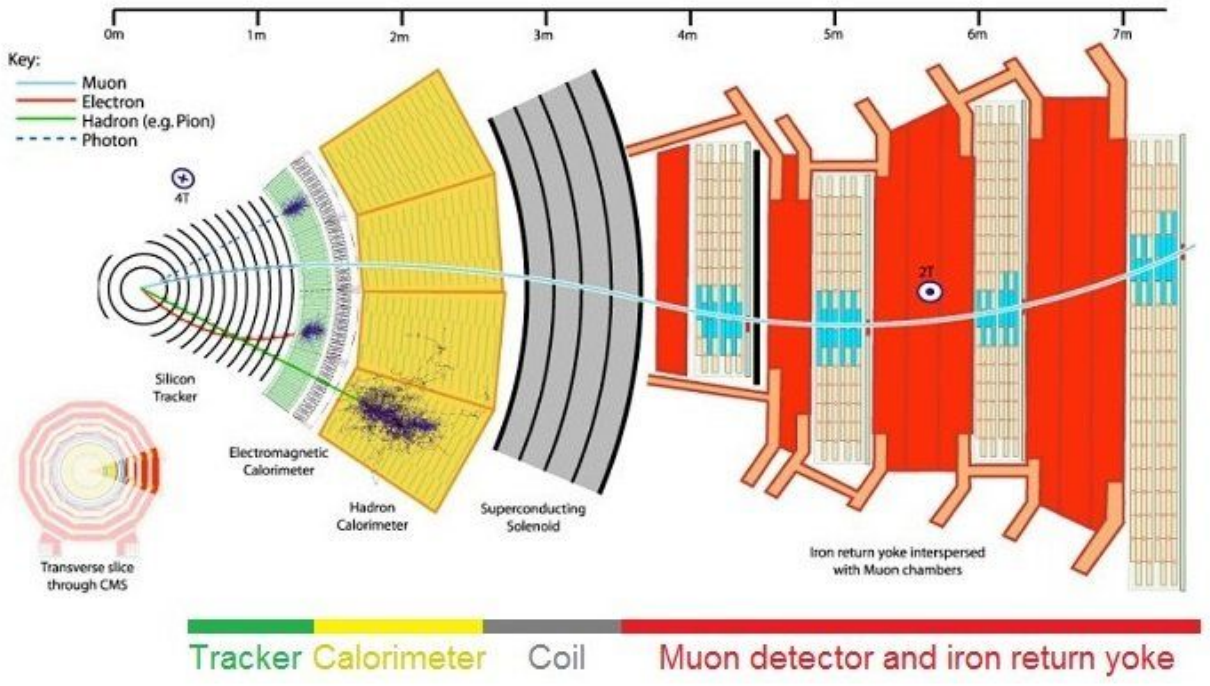
MUON CHAMBERS
Barrel: 250 Drift Tube, 480 Resistive Plate Chambers
Endcaps: 468 Cathode Strip, 432 Resistive Plate Chambers



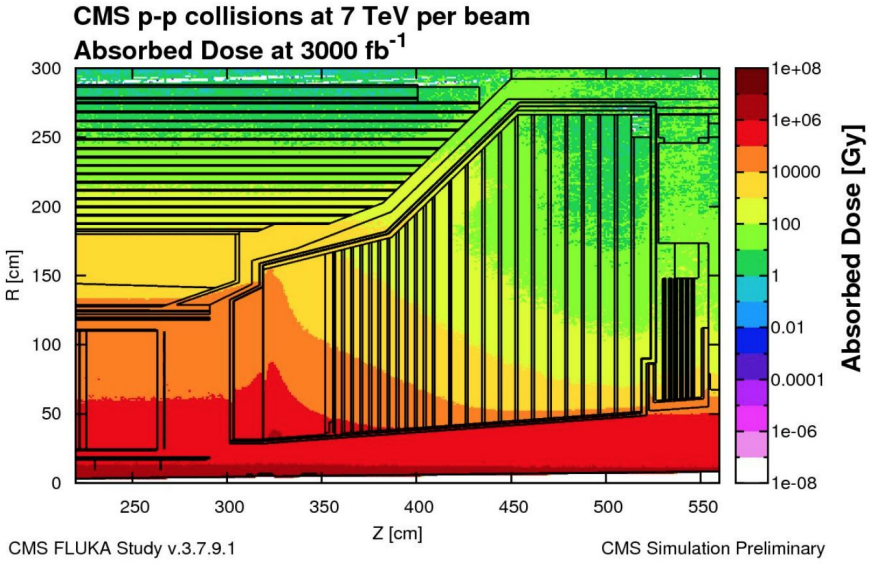
CRYSTAL ELECTROMAGNETIC CALORIMETER (ECAL)
~76,000 scintillating $PbWO_4$ crystals

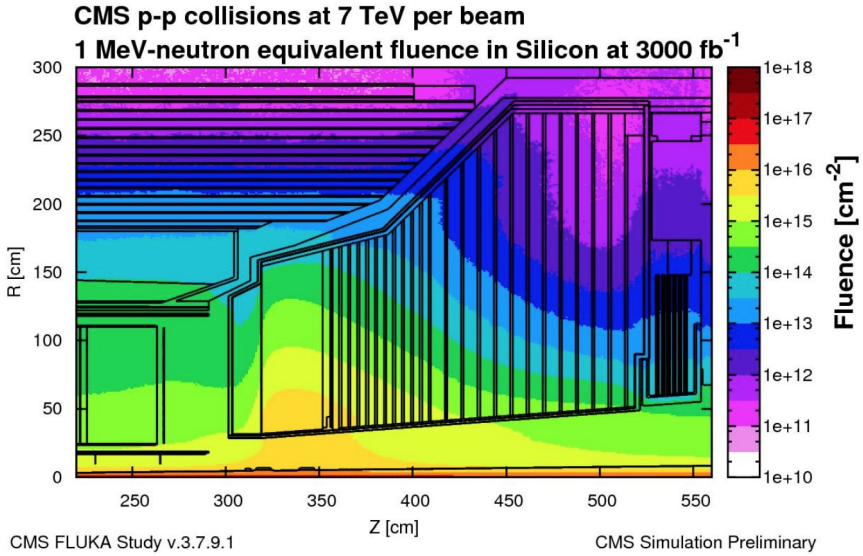
HADRON CALORIMETER (HCAL)
Brass + Plastic scintillator ~7,000 channels

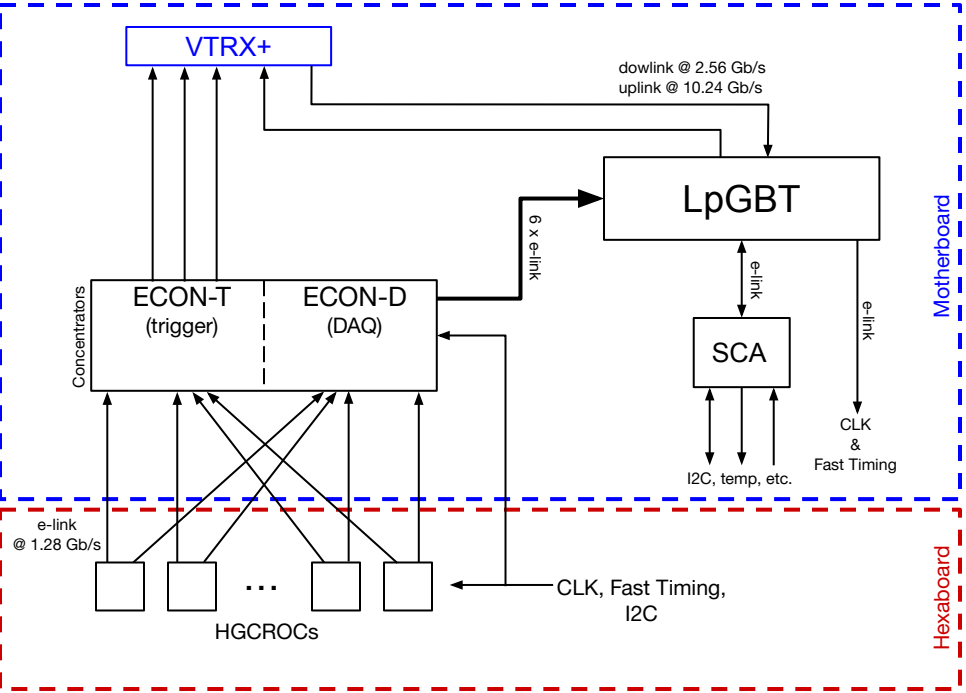
CMS


0m
1m
2m
3m
4m
5m
6m
7m
Key:
Muon
Electron
Hadron (e.g. Pion)
Photon
4T
2T
Silicon Tracker
Electromagnetic Calorimeter
Hadron Calorimeter
Superconducting Solenoid
Iron return yoke interspersed with Muon chambers
Transverse slice through CMS
Tracker
Calorimeter
Coil
Muon detector and iron return yoke

Radiation Levels in HGCAL Region






VTRX+
dowlink @ 2.56 Gb/s
uplink @ 10.24 Gb/s
LpGBT
6 x e-link
e-link
e-link
Concentrators
ECON-T
(trigger)
ECON-D
(DAQ)
SCA
CLK
&
Fast Timing
I2C, temp, etc.
Motherboard
e-link
@ 1.28 Gb/s
CLK, Fast Timing,
I2C
HGCROCs
Hexaboard