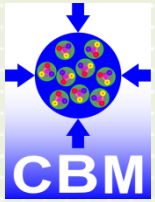


Front-End Electronics for BM@N STS, characterization and quality assurance

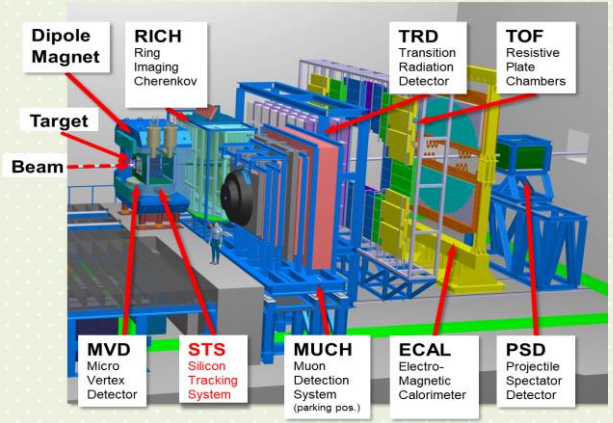
Mikhail Shitenkov
for the CBM-STS group

NEC'2019, 30 September 2019 to 4 October 2019,
Montenegro, Budva, Becici

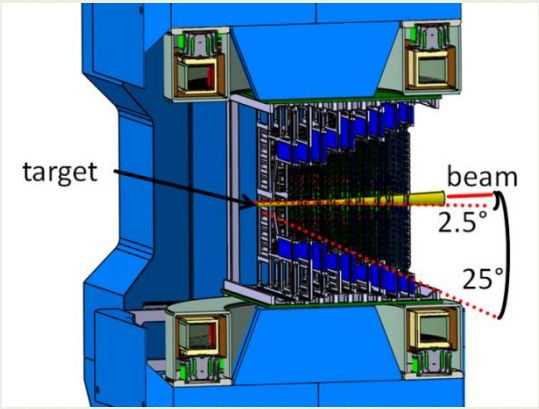
OUTLINE

- Silicon Tracking System of CBM and BM@N experiment
- Front-End Electronics for BM@N STS
- Front-End Electronics characterization and calibration
- Module assembly at JINR
- Tests of the modules
- Summary

Silicon Tracking System of CBM Experiment



CBM experiment at FAIR



STS inside Dipole Manet

Central CBM detector: charged-particle tracking + momentum measurement

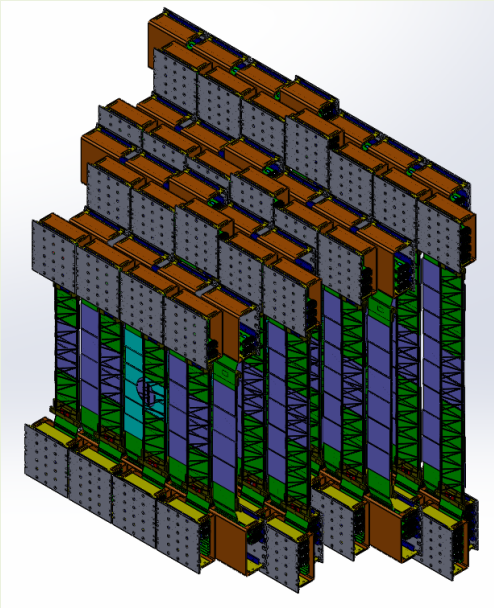
Challenges:

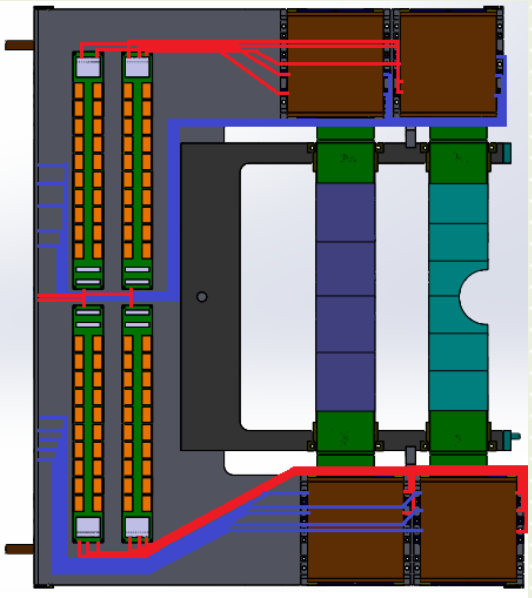
- Up to ~700 charged particles per heavy ion collision
- $10^5 – 10^7$ heavy-ion collisions per second

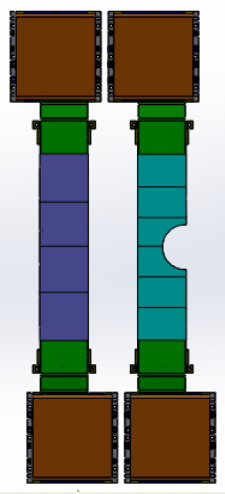
Technical solutions:

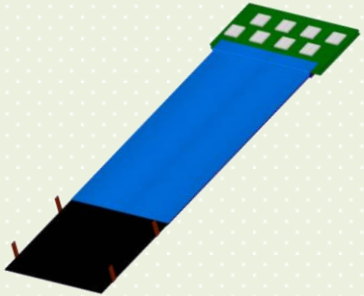
- **8 tracking stations, ≈ 4 m² total area, 896 detector modules, 106 ladders**
- *double-sided silicon microstrip sensors*
  - *hit spatial resolution ≈25 μm*
  - *material budget per tracking station: ≈0.3% – 2% X_0*
  - *radiation tolerance up to 1 × 10^{14} n/cm² (1 MeV equivalent)*
- self-triggering electronics, time-stamp resolution ≈ 5 ns
- low-mass detector modules/ladders

Layout of BM@N STS









4 Stations are based on CBM-type modules with double-sided microstrip silicon sensors

16 Mechanical quarter-Units

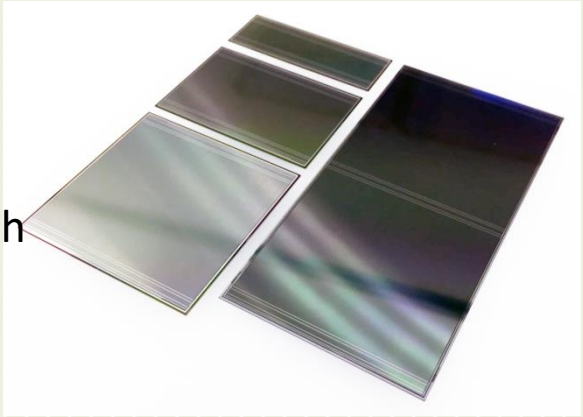
34 Ladders

292 Modules

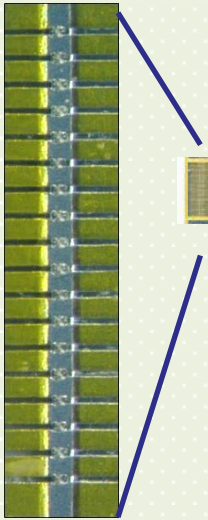
Number of channels: ~600k, Power consumption: ~15 kW

Sensors and micro-cables

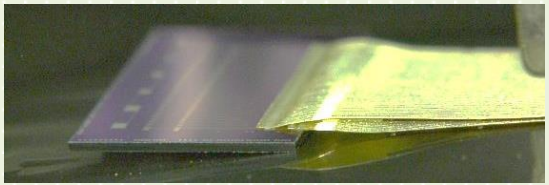
- double-sided
- Thickness is 300 µm
- 1024 strips of 58 µm pitch
- Stereo angle 7.5°
- 2 variants/strip lengths



6.2 x 6.2 cm²
4.2 x 6.2 cm²



signal layer: *64 Al lines of 116 µm pitch, 14 µm thick on 10 µm polyimide*



tab-bonding of 2 signal layers to All pads on ASIC and sensor

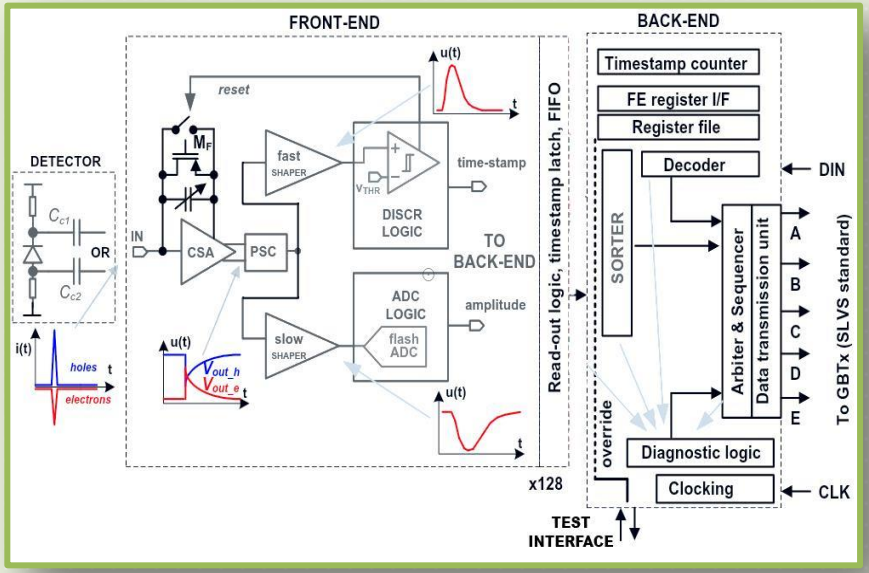
trace capacitance 0.45 pF/cm

trace lengths 5 - 55 cm

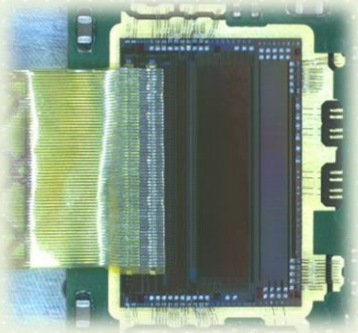
Front-end Readout ASIC

Front-end electronics is based on STS/MUCH XYTER ASIC

- 128 channels
- Self-triggered readout
- 5 bit ADC, time resolution < 8 ns
- Shaping time 80-120 ns (Slow Shaper for Amp.)
- Noise performance: <1500 ENC at 30 pF input load
- Switchable dynamic range (up to 120 fQ) and gain (Can be used for GEM detectors)
- Back-end interface : 5 e-link per ASIC with AC coupling



Block diagram of the architecture of the STS/MUCH XYTER



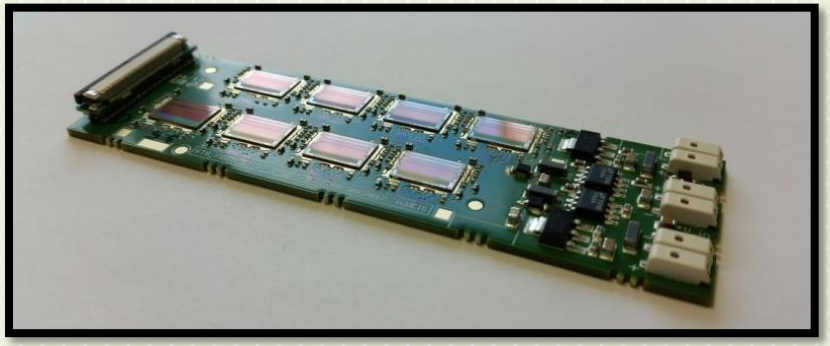
STS/MUCH XYTER on board with microcable

**developed by K.Kasinski, AGH*

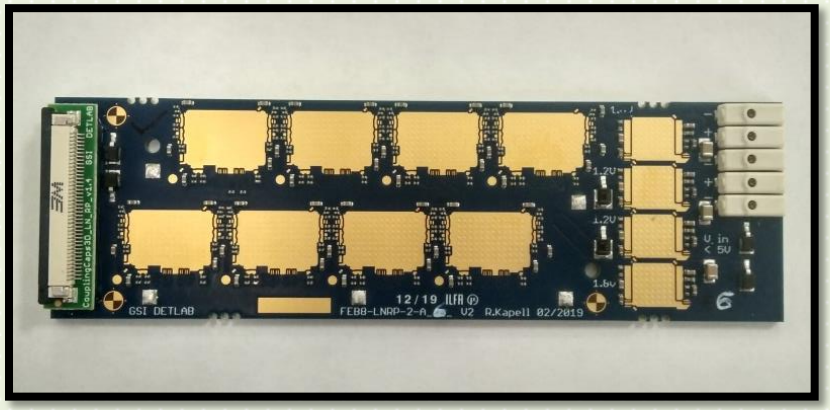
Front-end Board

Feature :

- Board size: 101.5 mm*30.6 mm
- 8 STS/MUCH-XYTER
- Bonding of cables with sensors
- Bonding of chip on Board wire1 elink per ASIC – 10 layers
- The use of components of the minimum available size
- 3D installation of AC decoupling capacitors on signal lines
- Energy consumption: 12W per charge.

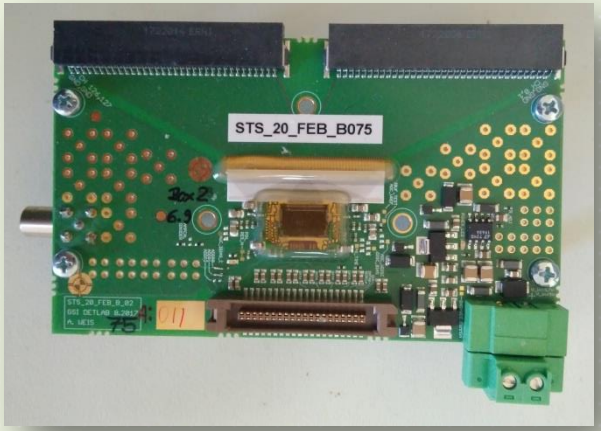


Front-End Board with 8 ASICs (v. 1.0)

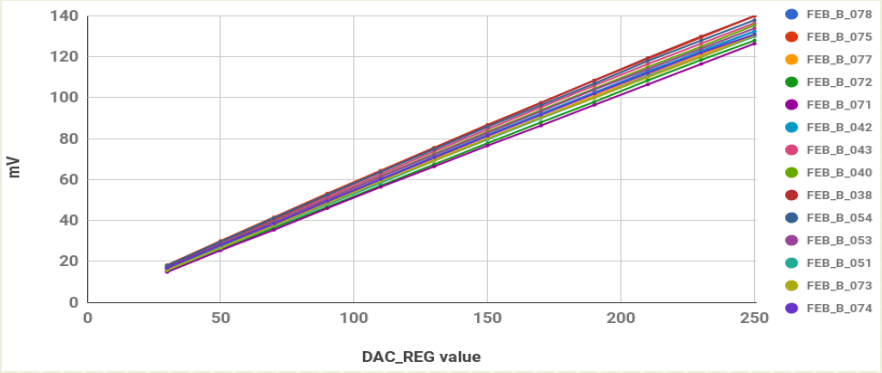


Front-End Board with SCL regulator (v. 2.0)

Characterization of the internal DAC in the ASIC STS/MUCH-XYTER

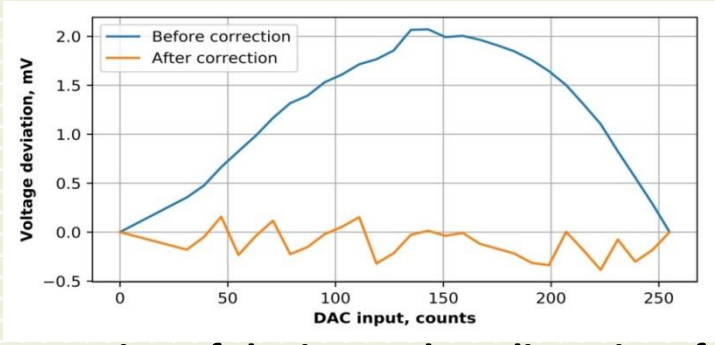


Front-End Board with 1 ASIC and ERNI connector



Inverse transfer function of the DAC for different ASIC

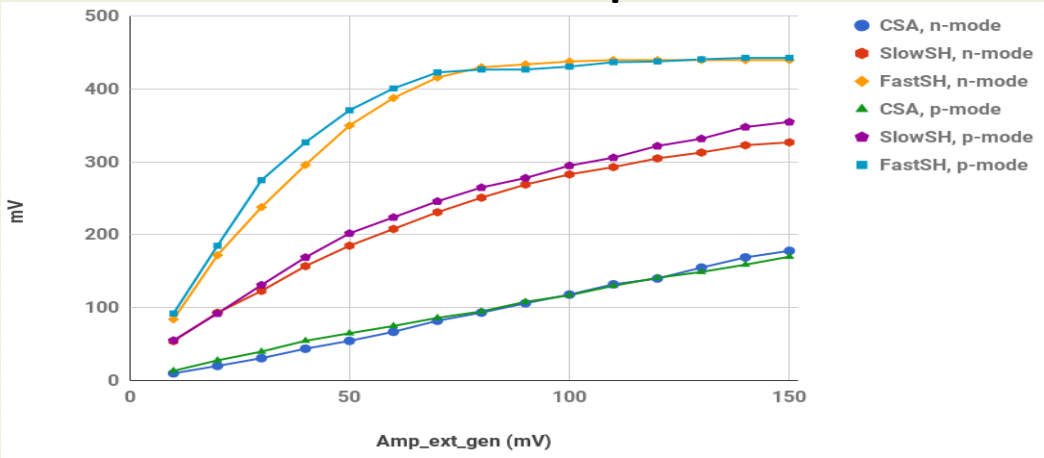
- Variance slope of the transfer characteristics = 3%
- $\mathrm{INL} = 1.3\%$



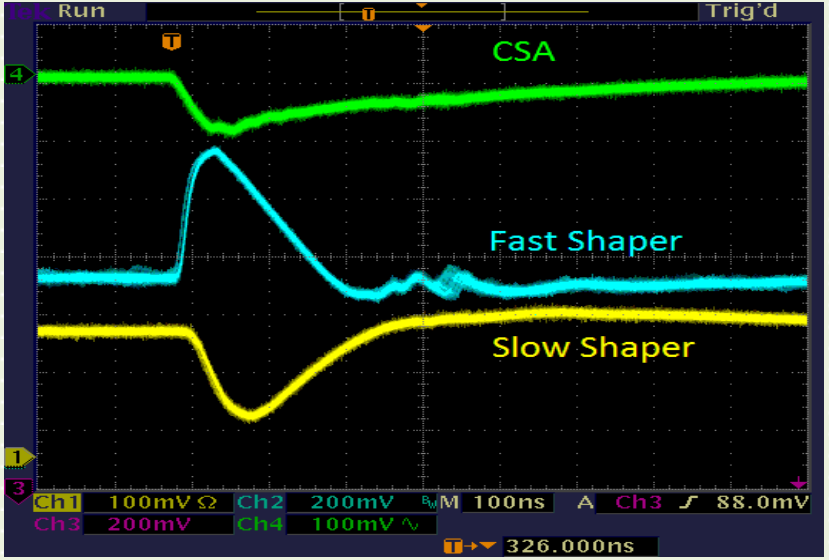
Compensation of the integral nonlinearity of the transfer characteristic

Study of the analog part

Transfer characteristics of the CSA, fast and slow shaper



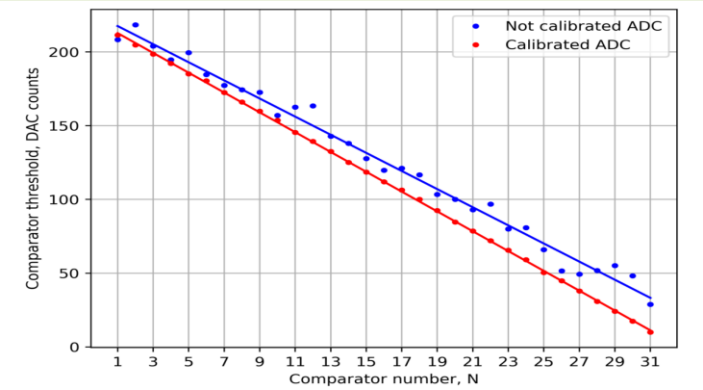
Oscillograms of analog outputs



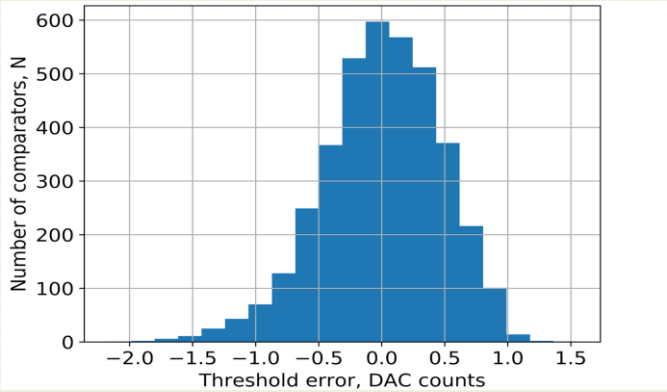
Gain in the range 0÷5 *fC*

Name	N-mode	P-mode
CSA	12.3±0.1 mV/fC	11.0±0.1 mV/fC
Slow shaper	32.6±1 mV/fC	37.1±0.7 mV/fC
Fast shaper	65.6±3.8 mV/fC	69.9±5.6 mV/fC

Calibration of in-channel ADC



Inverse transfer function of the ADC



Distribution of values of integral nonlinearity

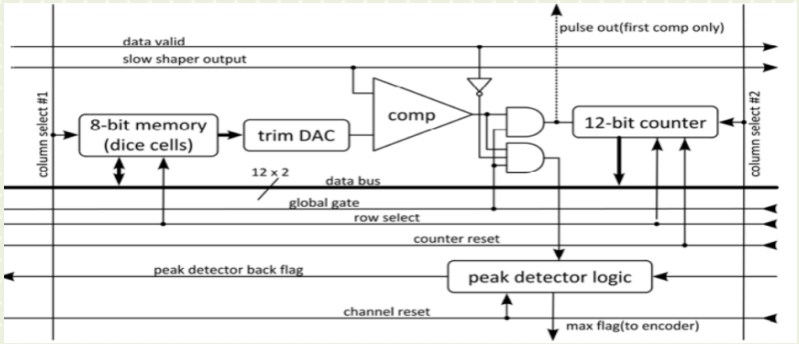


Diagram of the signal amplitude shaping unit

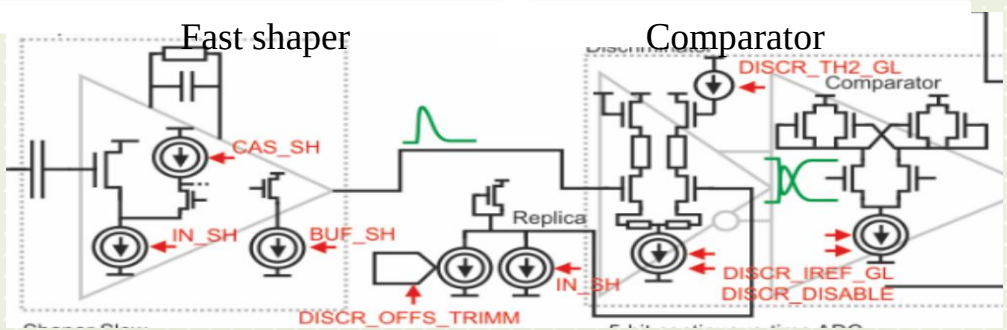
INL= 2.3%

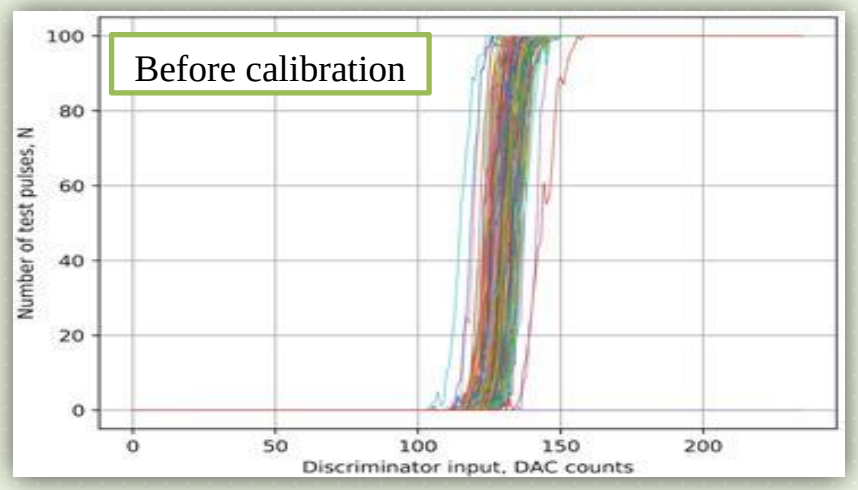
σ_{ch}= 2%

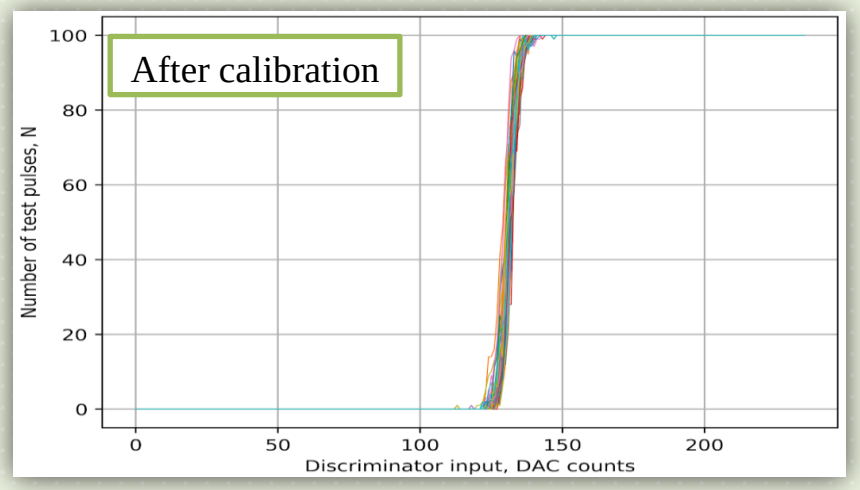
Calibrating Comparators in the fast signal path

$$\sigma_{before} = 4{,}5\ DAC\ counters$$

$$\sigma_{after} = 0{,}8\ DAC\ counters$$

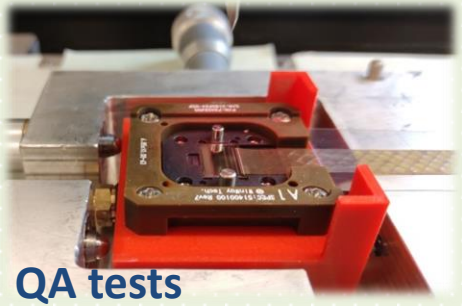




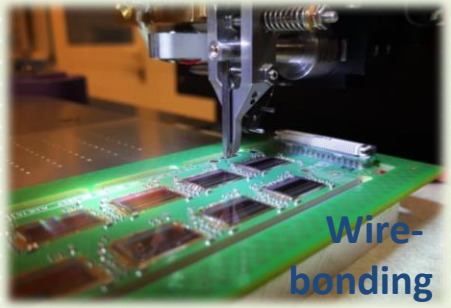


S-curves of thresholds of the Comparators on different channels

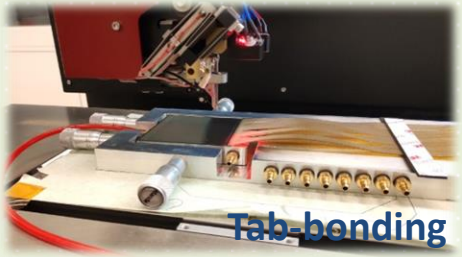
Module assembly at JINR



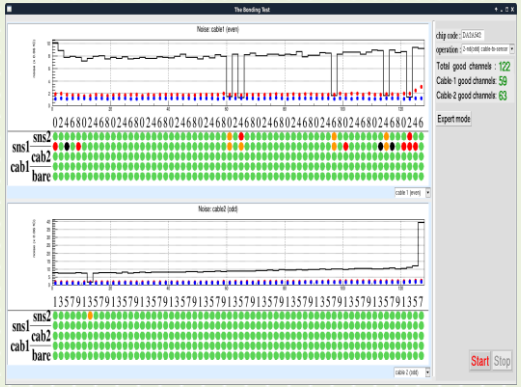
QA tests



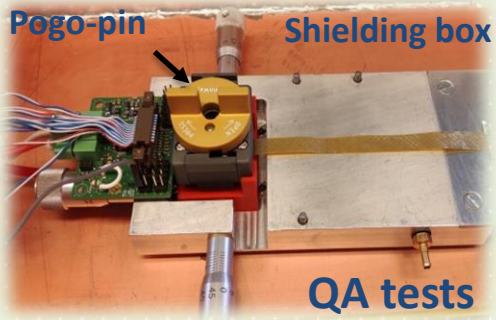
Wire-bonding



Tab-bonding



GUI of the bonding-test software (**A. Kolozhvari, JINR*)



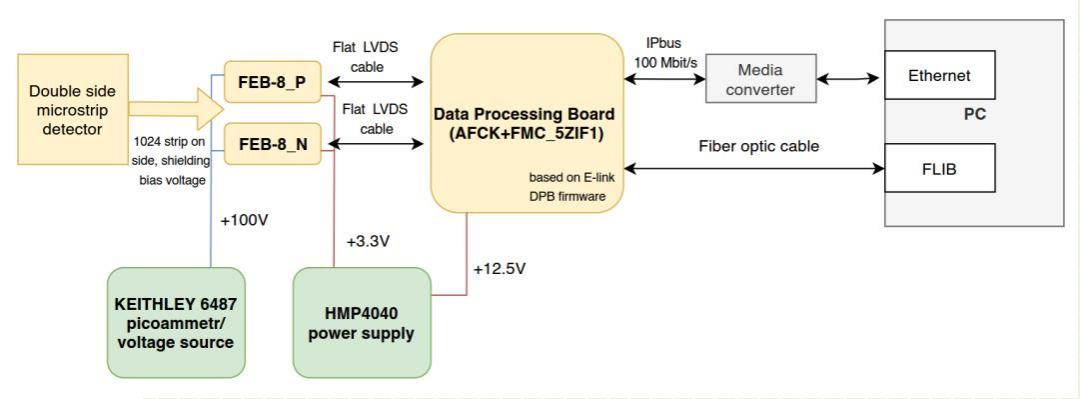
- Two clean rooms are equipped for the module assembly
- Full set of jigs was developed
- Quality Assurance procedures for bonding tests were developed and tested
- First modules have already assembled and tested

Assembled module

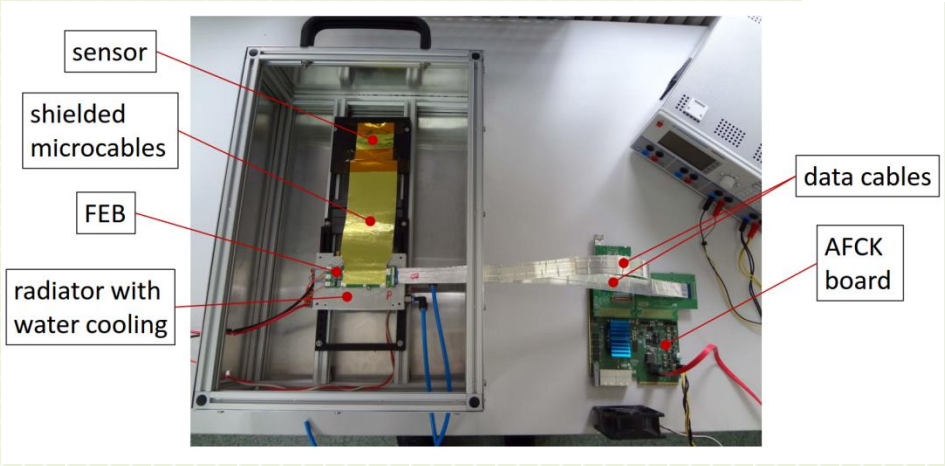
Readout chain for the tests of the modules

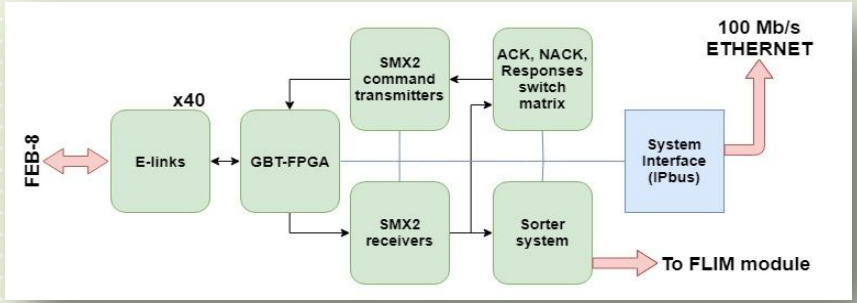
Functionality:

- E-link synchronization
- Read/write ASIC registers
- SMX2 synchronization
- Transmit data to FLIM
- Transmit data to IPbus



Block diagram of the readout system



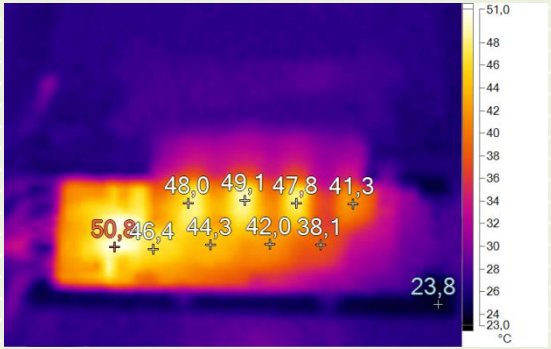


Block diagram of the modified E-link based DPB firmware

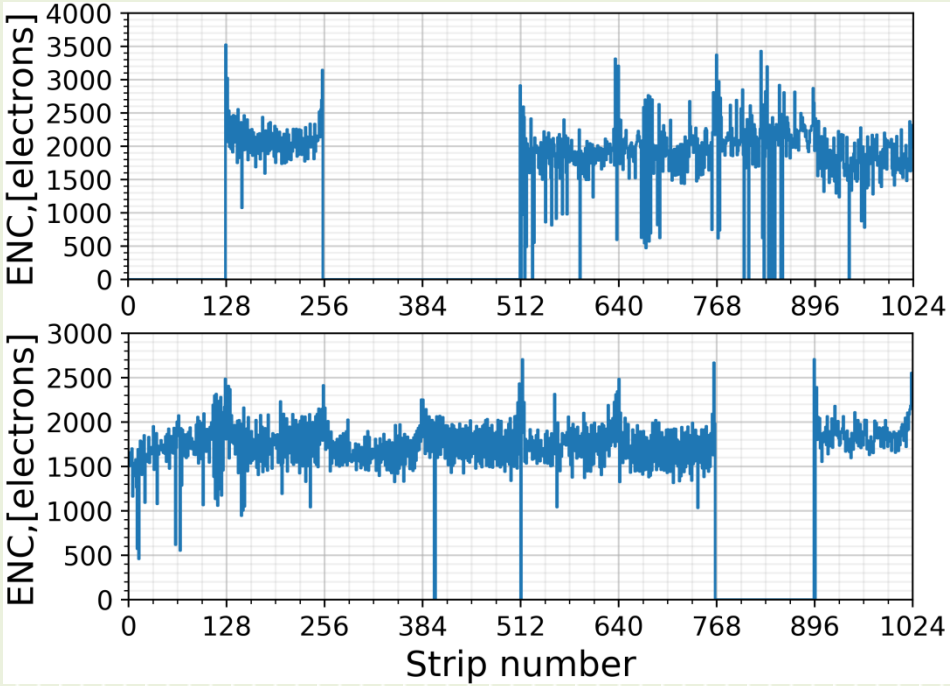
Tests of the modules

Detailed studies undergoing

- Functional tests
- Noise investigations
- Signal integrity
- Gain distribution
- Tests with radioactive source

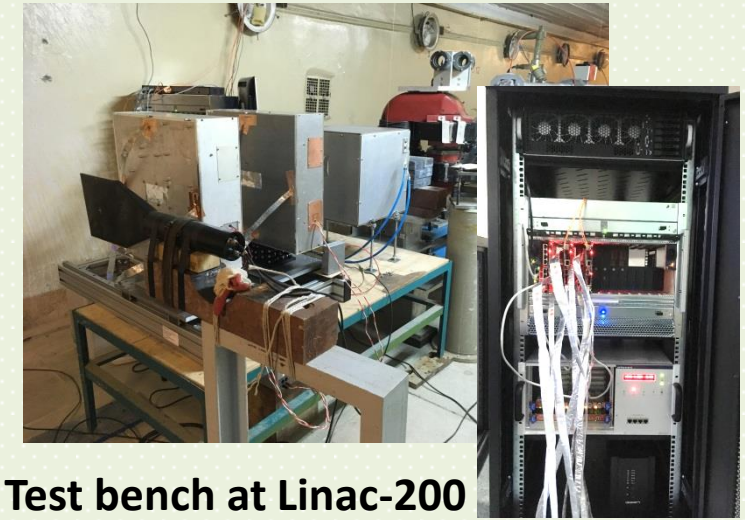


Temperature distribution on the FEB8

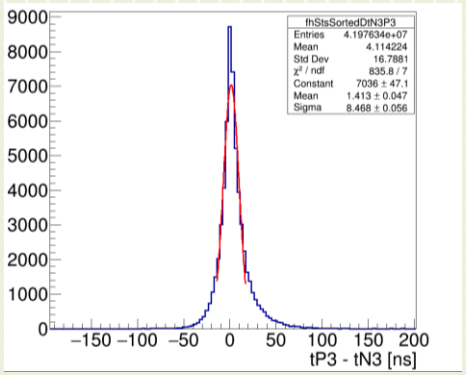


Noise per channel

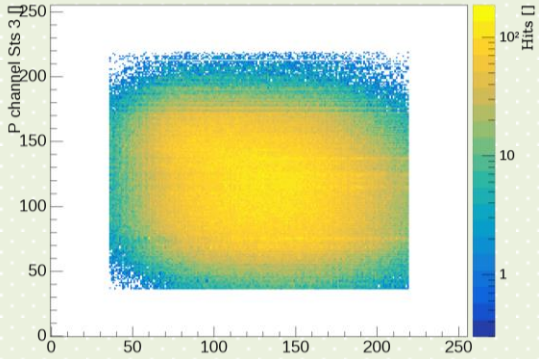
Tests of the DAQ system at Linac-200 (JINR LNP)



Test bench at Linac-200



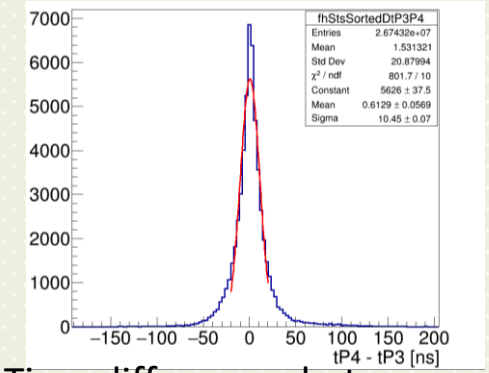
Time differences between hits on N and P sides of the sensor



Beam profile in the first station

Main goals of the beam test:

- To test readout electronics:
  - New STS/MUCH-XYTER ASICs
  - Time Synchronization system
  - DAQ System
- Data collection in two modes:
  - Free streaming and with a time reference to the trigger signal



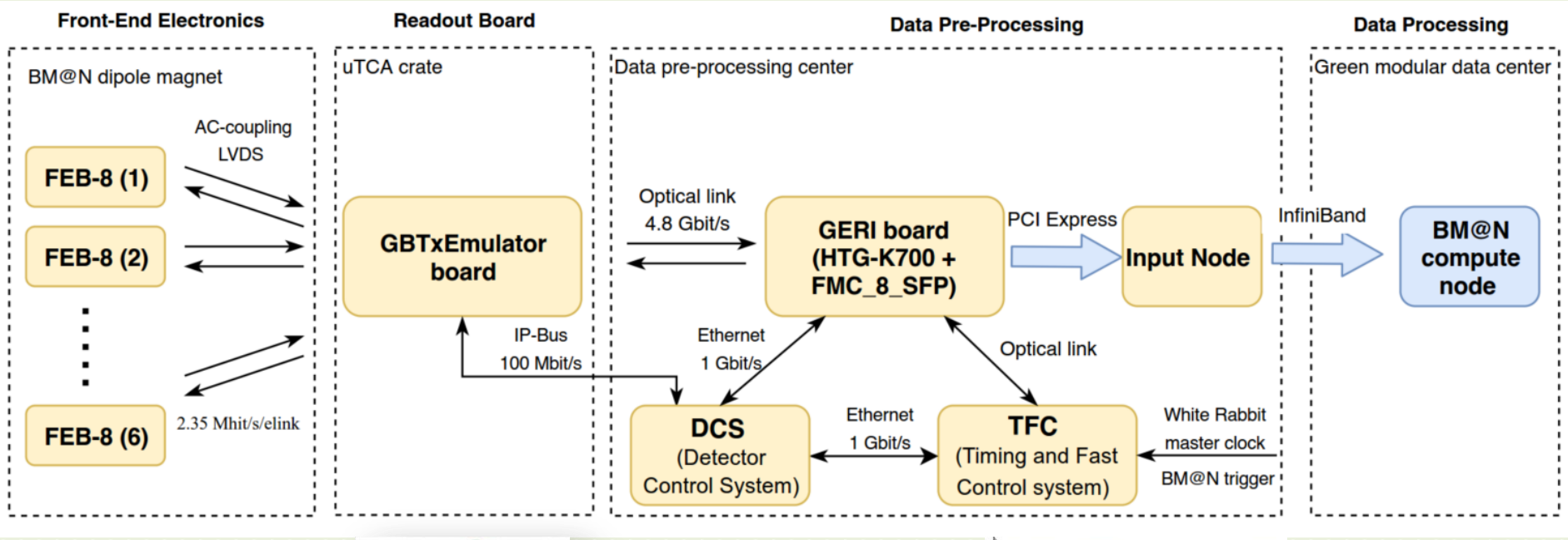
Time differences between hits on two sensors

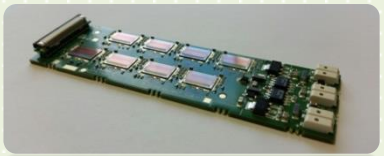
Summary

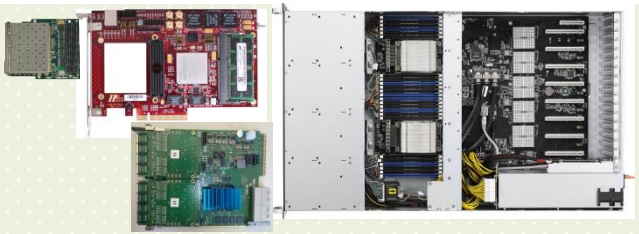
1. Test bench have been developed
   - Developed software for PC
   - Created a firmware for the FPGA on the Data Processing Board (AFCK)
2. STS/MUCH-XYTER characterization and calibration have been carried out
   - Testing the STS-HCTSP data transfer protocol
   - Calibration and characterization of the ASIC
3. The method of testing the quality of assembly of modules is developed
   - Per-channel measurement of noise characteristics
   - Calibration of the ASIC
4. Launch tests of the DAQ system have been performed


Thank you for your attention !

DAQ system of BM@N STS





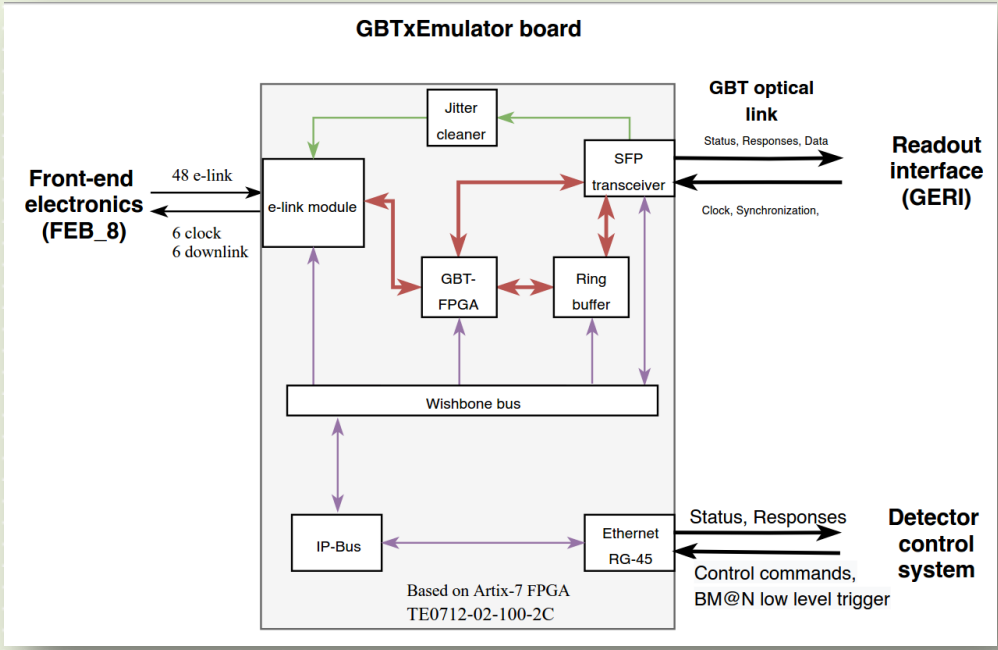


GBTxEmulator board

Provide interface between the Front-End Electronics and the Data Processing board
Feature:

- XYLINX FPGA (Artix-7)
- The project is in the stage of completion of development and functional tests
- 4.8 Gb/s link optical links connecting with the GERI
- 100 Mb/s IPbus interface for control
- E-Link interface:
  - 48 E-Links
  - 6 downlink E-Links + 6 downlink clocks
  - 80 MHz E-Link clock

Trenz TE0712-02-100-2C



Block diagram of the architecture of the GBTxEmulator

**developed by W. Zabołotny, WUT*