

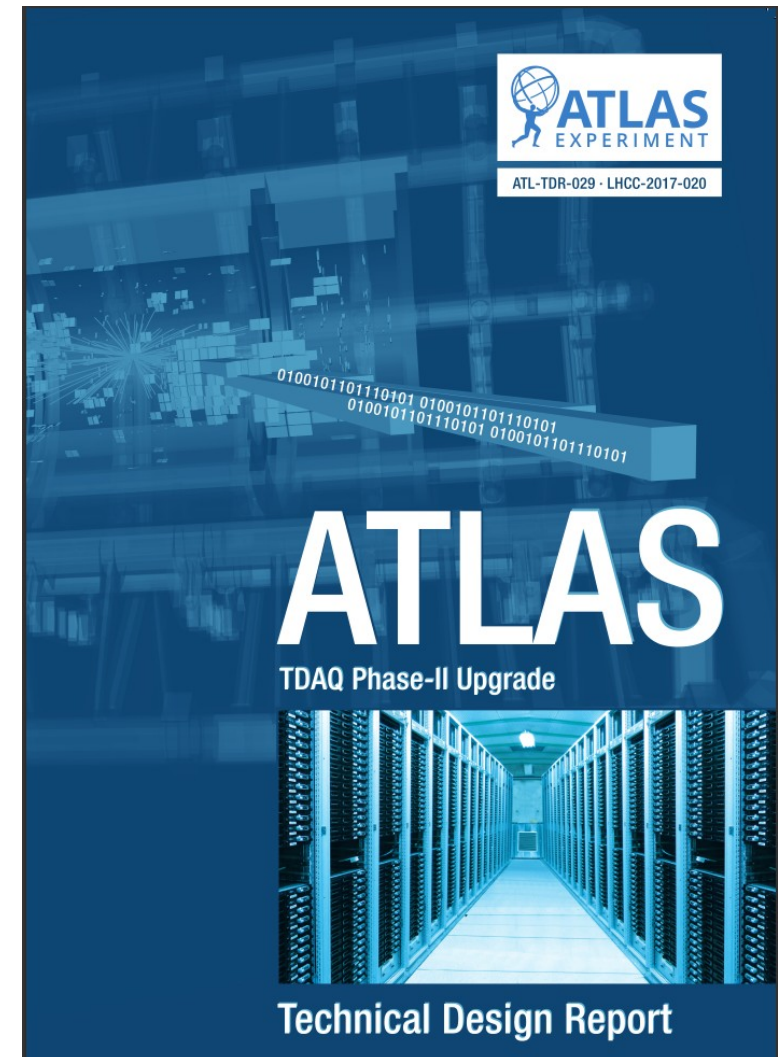


ATLAS Trigger and Data Acquisition Upgrades for the High Luminosity LHC

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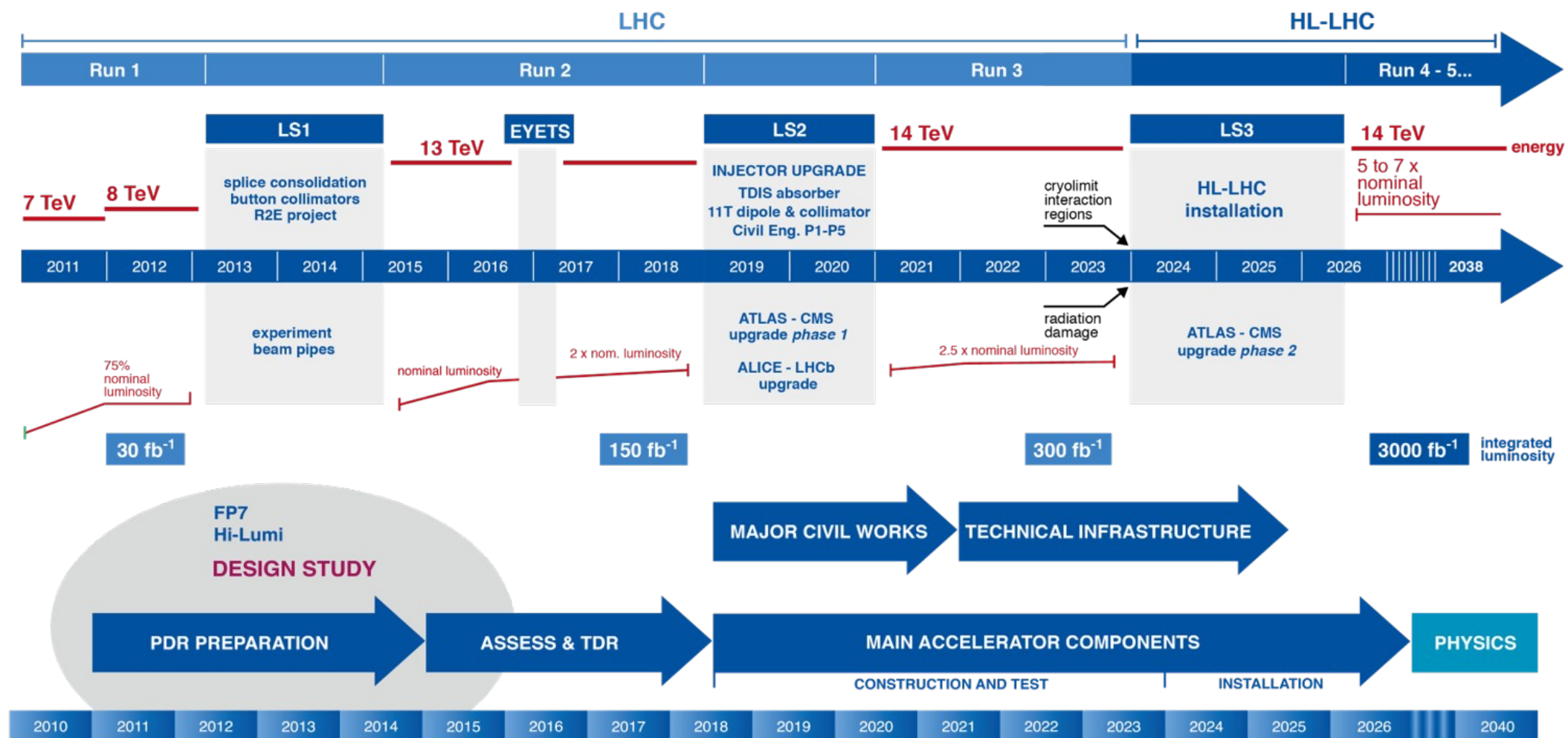
on behalf of
ATLAS Collaboration

- HL-LHC Overview
- Physics Motivations & Challenges
- ATLAS Phase-II TDAQ Architecture
- TDAQ Sub-Systems
- Outlook

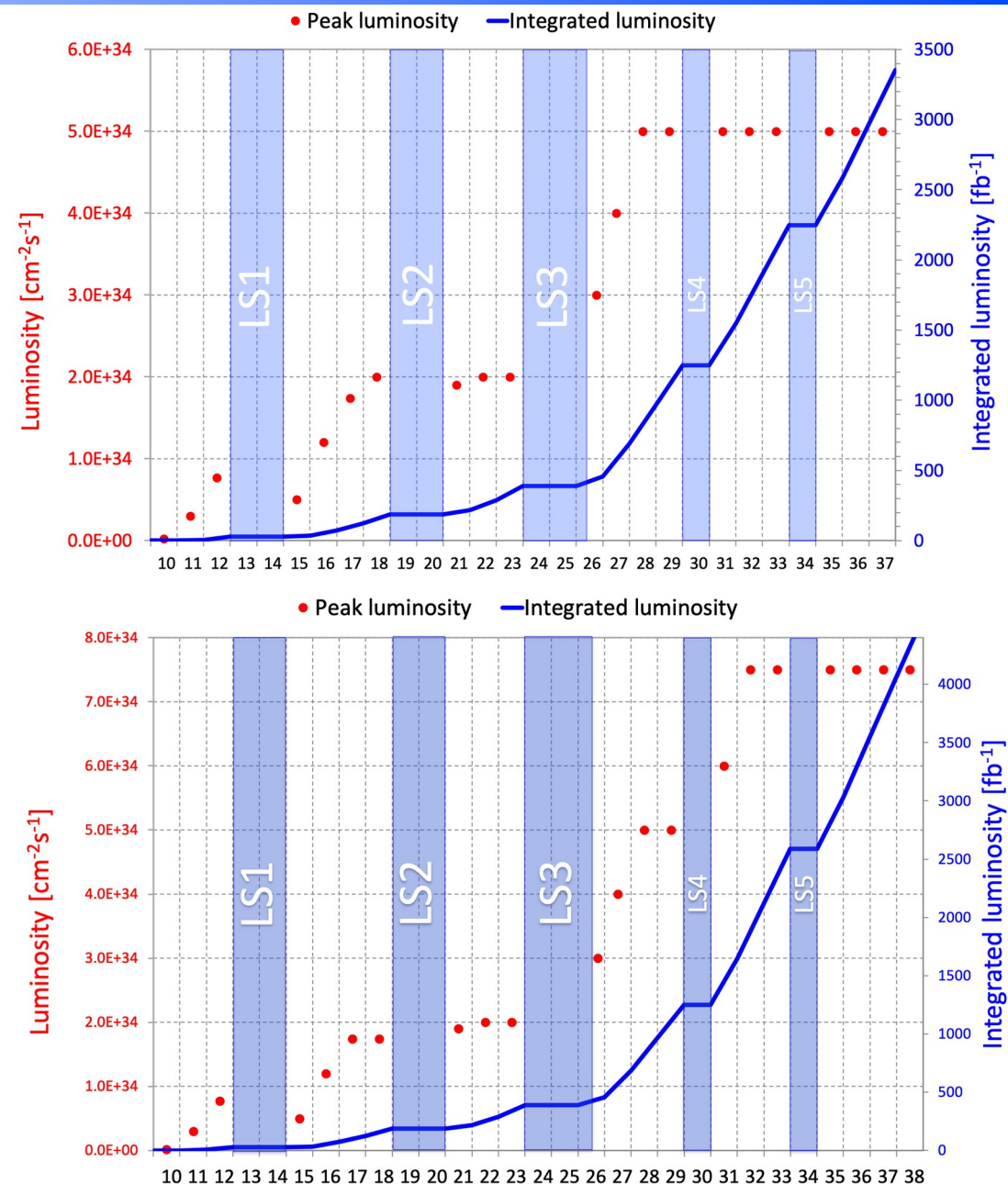


ATLAS Collaboration
Technical Design Report for the Phase-II Upgrade of
the ATLAS TDAQ System
<https://cds.cern.ch/record/2285584>

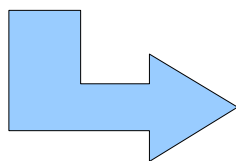
LHC / HL-LHC Plan



- HL-LHC programme aims at a total integrated luminosity of at least 3000 fb⁻¹
 - ten-fold increase wrt Run 1/2/3 aggregate
- Corresponding increase in peak instantaneous luminosity
 - $\mathcal{L} \sim 5 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ (ultimate $7.5 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$)
 - achieved mainly via pileup $\langle \mu \rangle$: 140 (ultimate 200)
- For reference Run 3 operation point:
 - $\mathcal{L} \sim 2 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ - $\langle \mu \rangle \sim 50$



- The challenging and broad HL-LHC programme requires trigger thresholds comparable with the current ones, e.g.:
 - electroweak scale requires low p_T leptons
 - searches for new physics with low Δm
 - HH measurements requires low p_T jets /b-jets
- At fixed threshold, trigger rates scale with peak luminosity
 - worsened by pileup environment

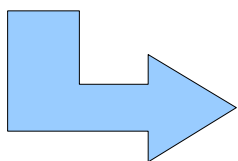


Major increase in readout and recording rates

| Trigger Selection offline threshold (GeV) | Run 1 | Run 2 | HL-LHC |
|---|--------|--------|---------------|
| Isolated single e | 25 | 27 | 22 |
| Isolated single μ | 25 | 27 | 20 |
| Di- γ | 25, 25 | 25, 25 | 25, 25 |
| Di- τ | 40, 30 | 40, 30 | 40, 30 |
| Four-jet w/ b-jets | 45 | 45 | 65 |
| H_T | 700 | 700 | 375 |
| MET | 150 | 200 | 200 |

| | Run 3 | Phase II |
|----------------------|-------|----------|
| Readout rate (MHz) | 0.1 | 1 (4) |
| Recording rate (kHz) | 1.5 | 10 |

- High-granularity to cope with pileup
 - both for readout and trigger
 - complete replacement of inner detector \rightarrow ITk

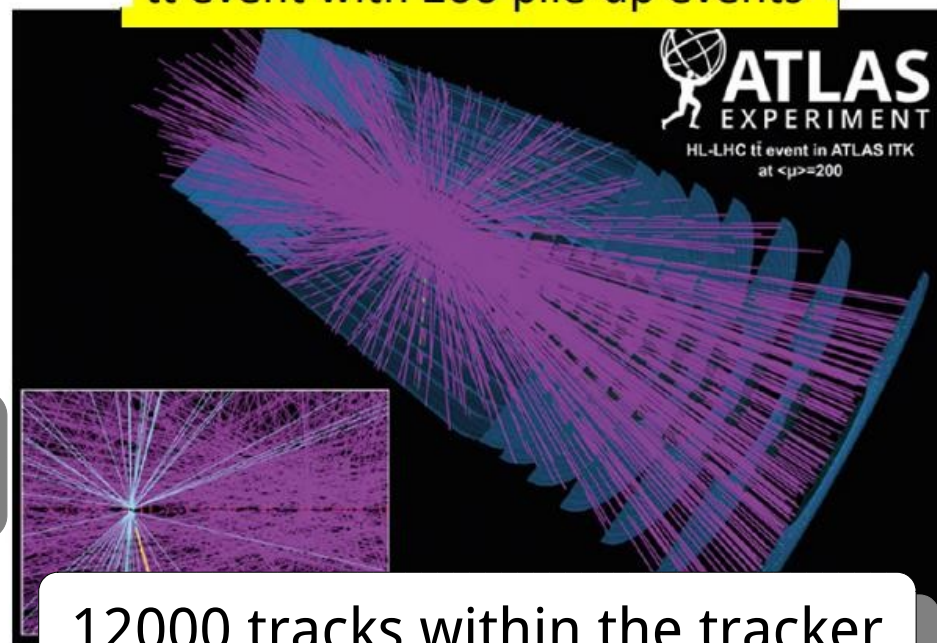


Larger event size

- Higher readout rate needs overhaul of detector front-end electronics

- occasion to increase first level-trigger latency
 - *currently limited by on-detector buffer depths*
- adopt unified readout link technology
 - *GBT/Versatile*

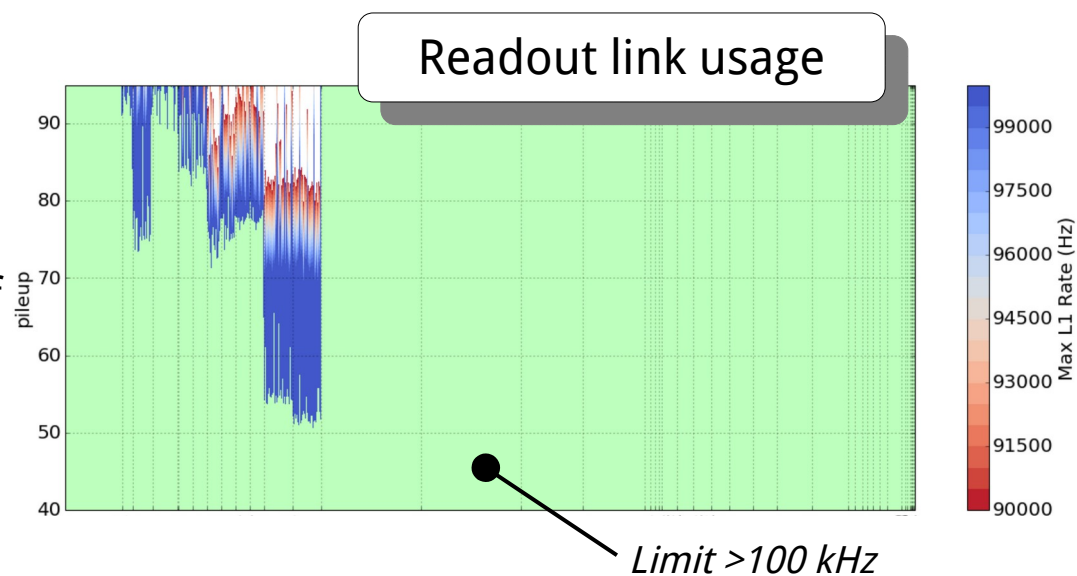
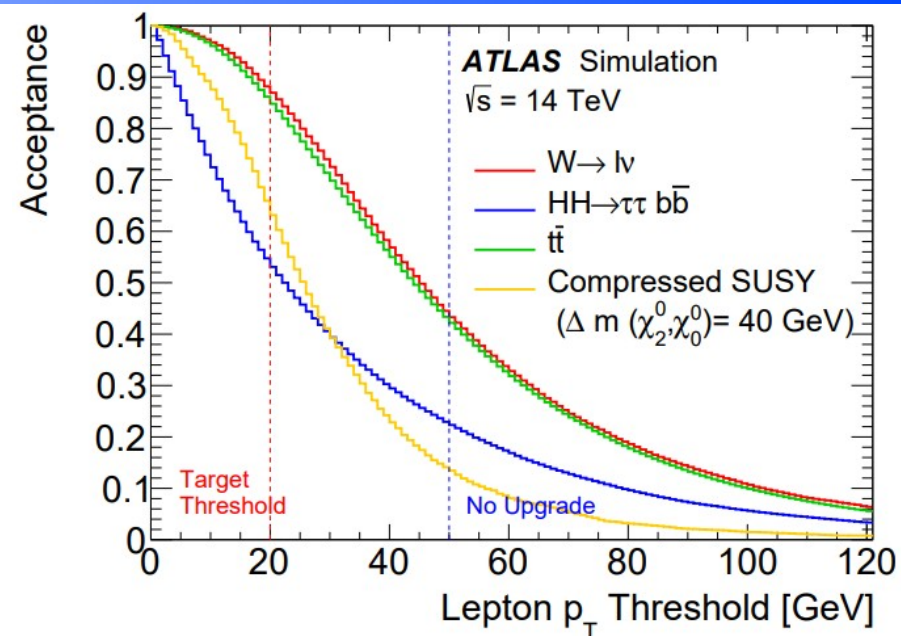
$t\bar{t}$ event with 200 pile-up events



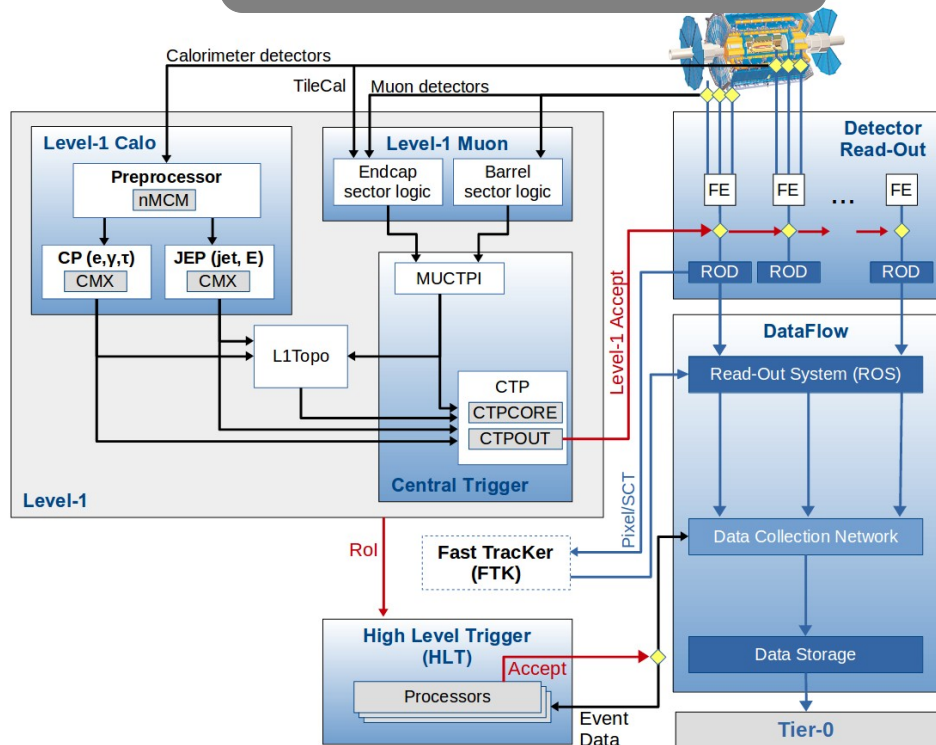
12000 tracks within the tracker

| | Run 3 | Phase II |
|---|-------|----------|
| First-level trigger latency (μs) | 2.5 | 10 |
| Event size (MB) | 2.5 | >5 |

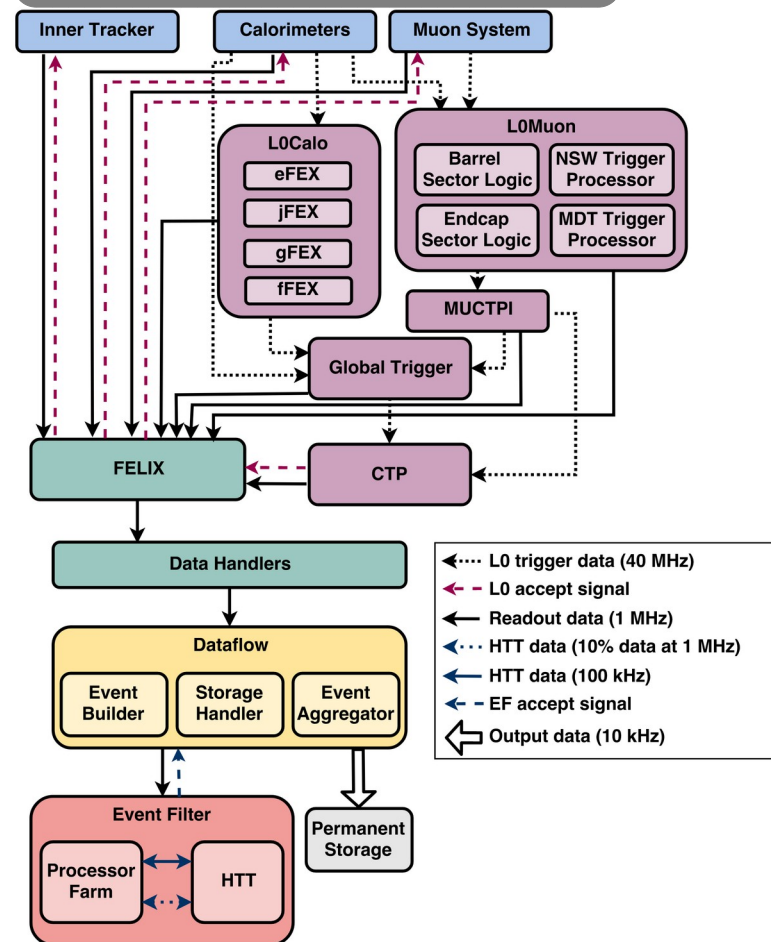
- ATLAS TDAQ requires a major overhaul to cope with the Phase-II conditions and requirements
- Existing system limited in every aspect
 - trigger and timing distribution
 - capabilities of the first-level trigger
 - readout and dataflow bandwidth
- Phase-II TDAQ design is not a revolution
 - scale implementation to Phase-II requirements
 - learn lessons from previous runs
 - take advantage of last 10+ years of technology evolution
 - apply solutions specific to the HL-LHC challenges



Run 2 ATLAS TDAQ



Phase-II ATLAS TDAQ

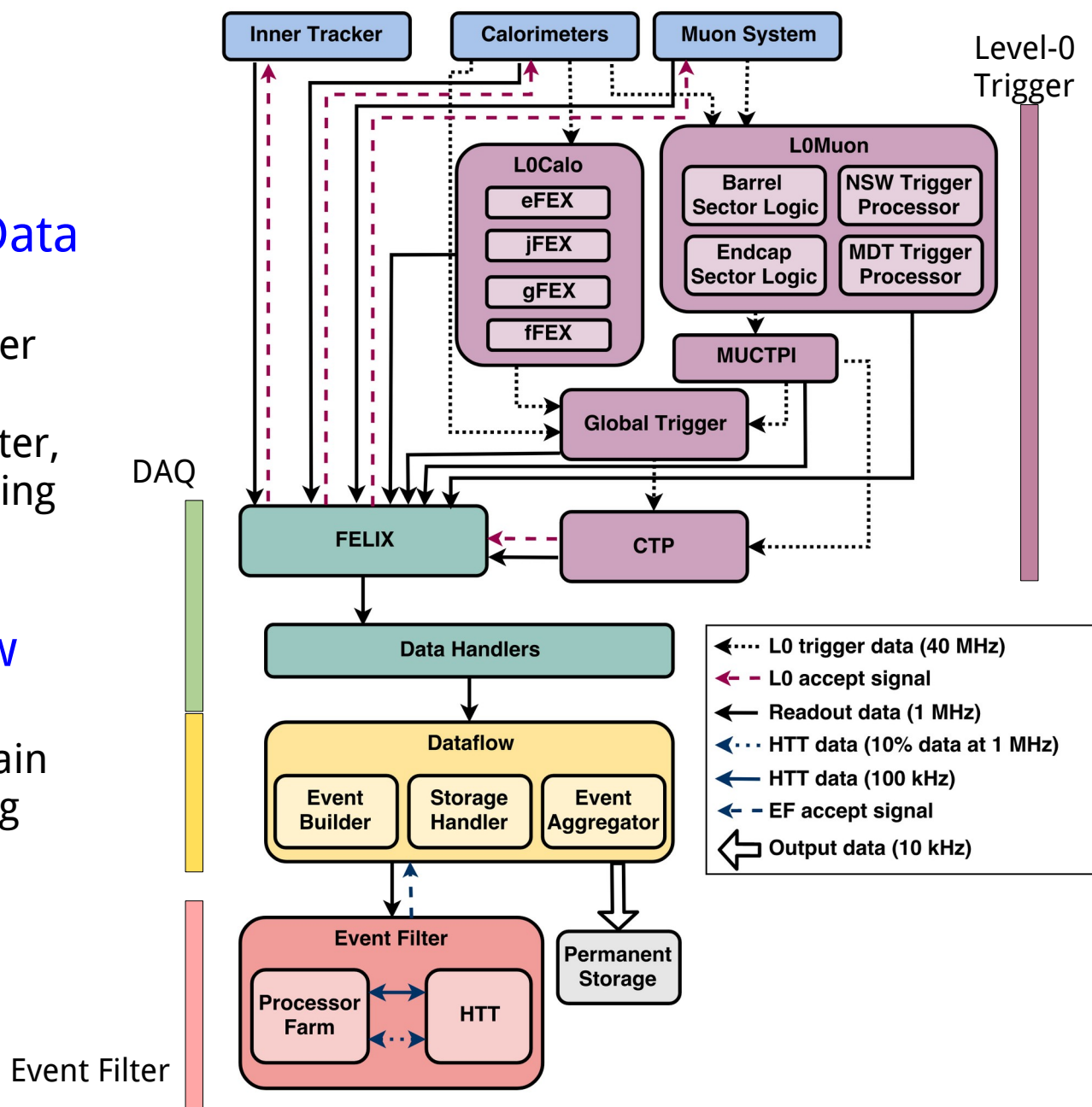


- Two-Level Trigger and Data Acquisition System

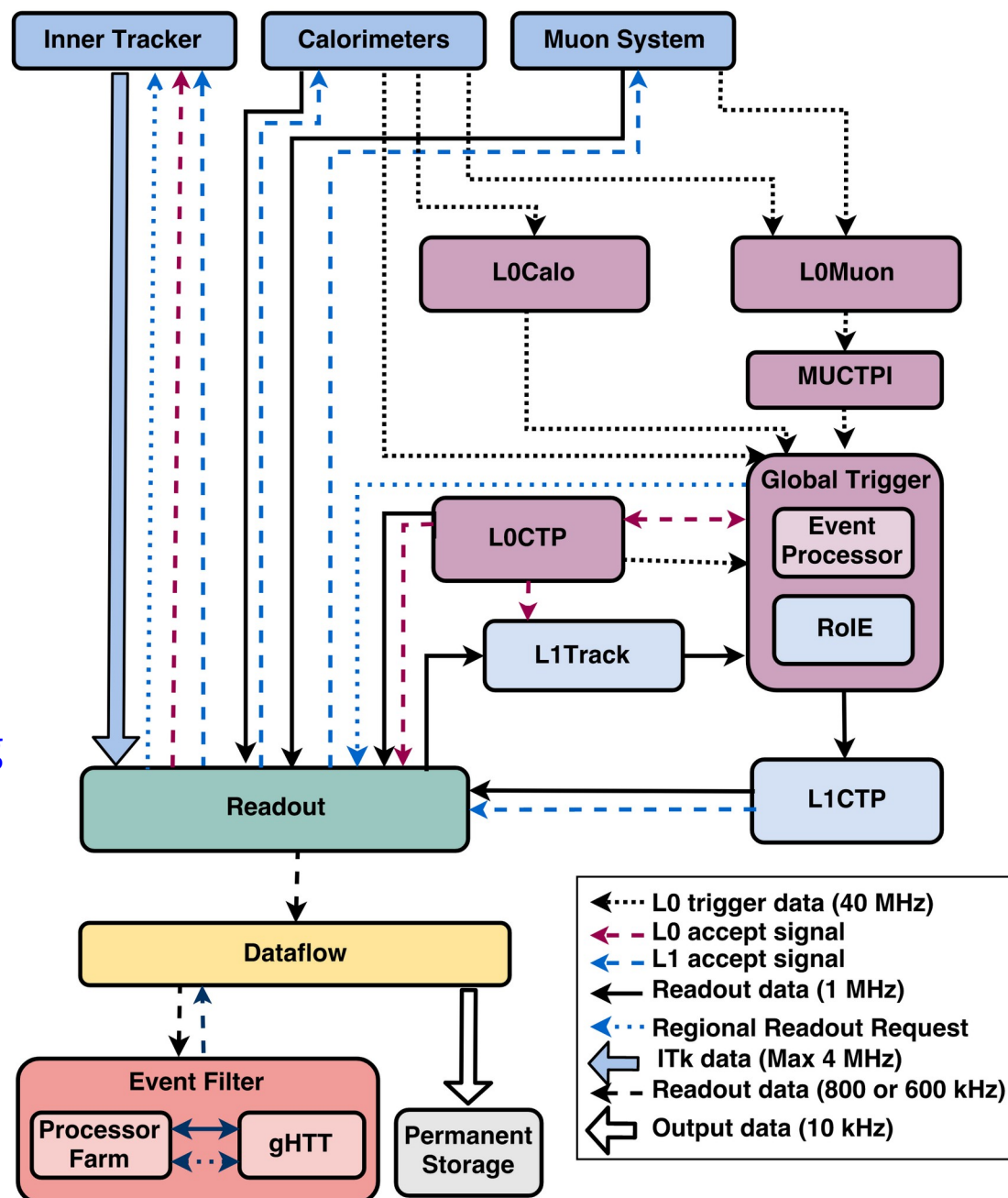
- hardware-based L0 trigger system
- software-based Event Filter, aided by dedicated tracking accelerator

- Storage-based data-flow infrastructure

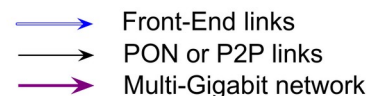
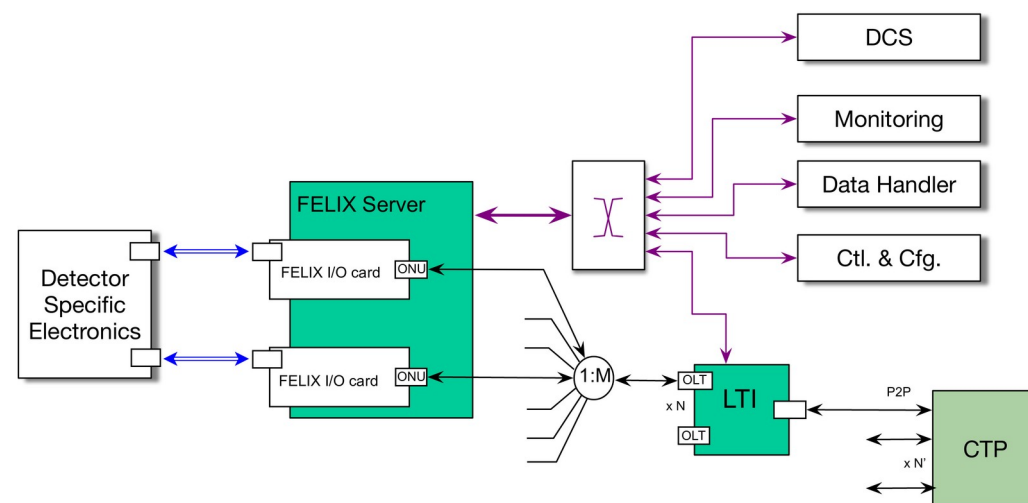
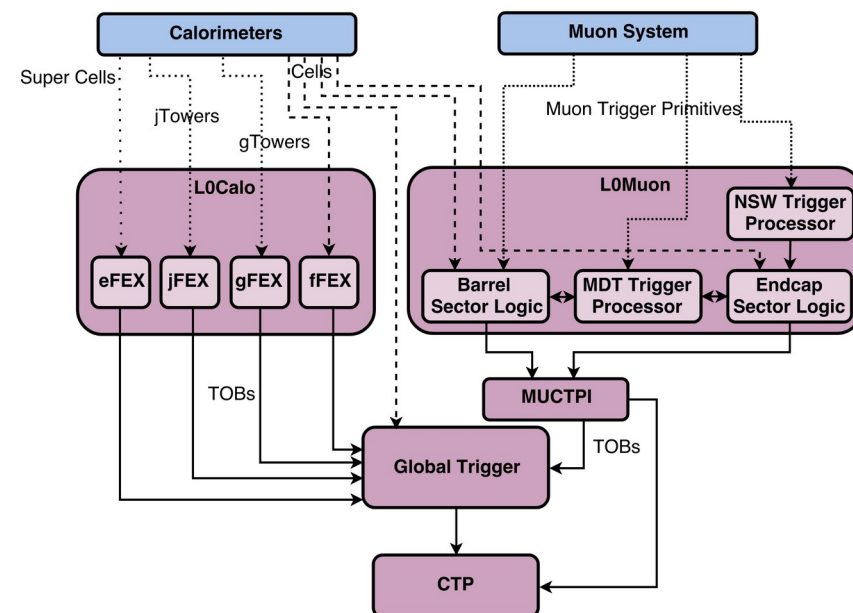
- decouple real-time domain from software processing
- enable advanced data processing strategies



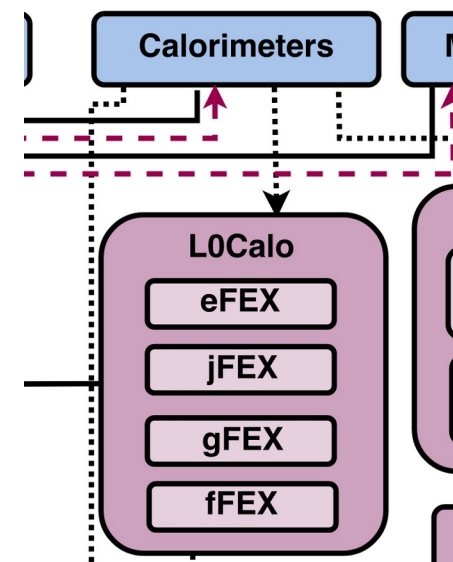
- Evolution path to a two-level hardware trigger included in the design
 - L0 – 4 MHz
 - L1 – 1 MHz
 - Event Filter – 10 kHz
- Possible transition from baseline to evolution driven by physics requirements
 - hadronic trigger rates
 - occupancy of inner layers of ITk
- Avoid the baseline TDAQ implementation restricting the trigger menu at the ultimate HL-LHC operating conditions
- Level-1 Trigger combines L0 objects with track information from a dedicated subsystem to discriminate against pileup in the calorimeter



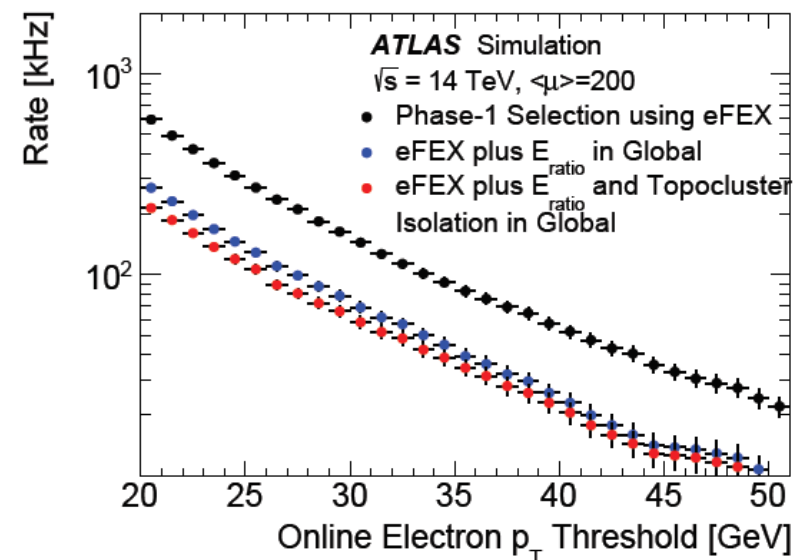
- Operates at 40 MHz applying selection criteria based on
 - calorimeter activity
 - muon detection
 - topological information
- Central Trigger Processor includes
 - interface to the LHC timing
 - prescaling and preventive deadtime functionalities
- Completely new trigger & timing distribution system
 - options based on passive optical splitters and point-to-point links



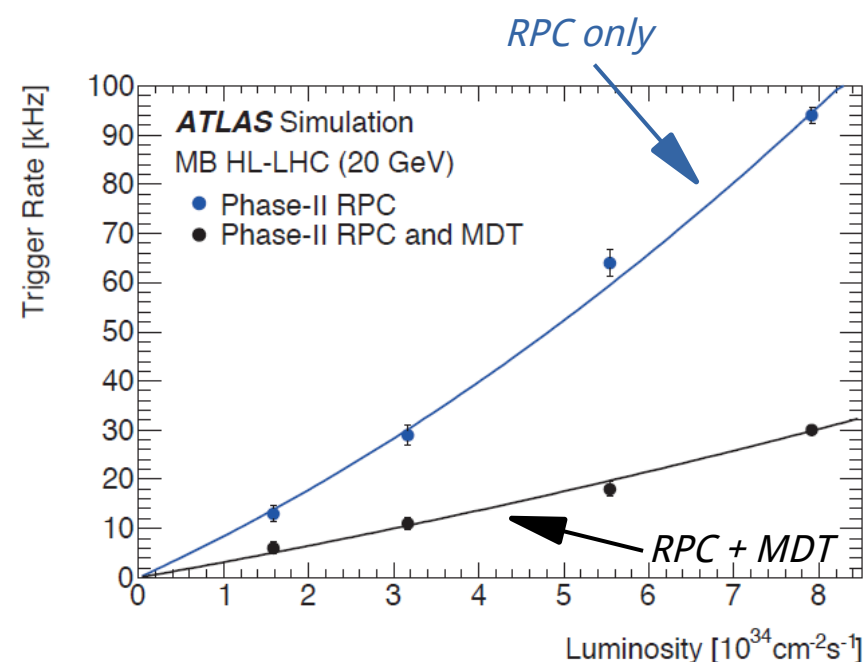
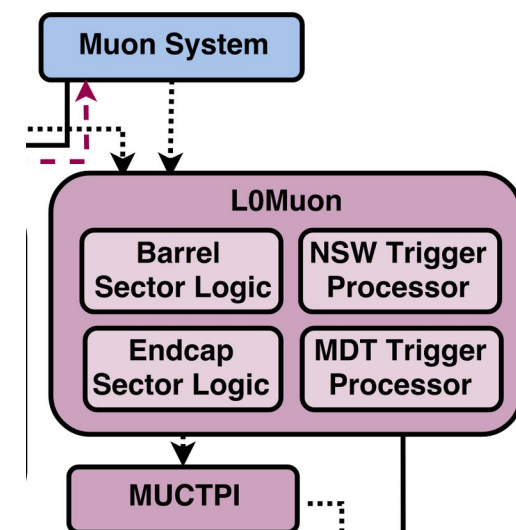
- Largely inherited from the ongoing Phase-I upgrade
- Exploits reduced-granularity data from EM and hadronic calorimeters. Dedicated collections of boards implement:
 - electron and photon identification (eFEX)
 - single jet identification (jFEX)
 - large-R triggers and global quantities (gFEX)
 - forward electromagnetic jets identification (fFEX)



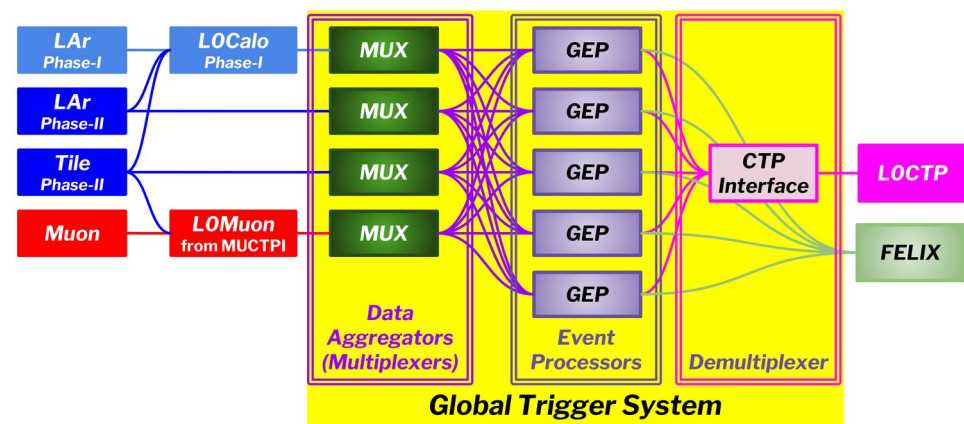
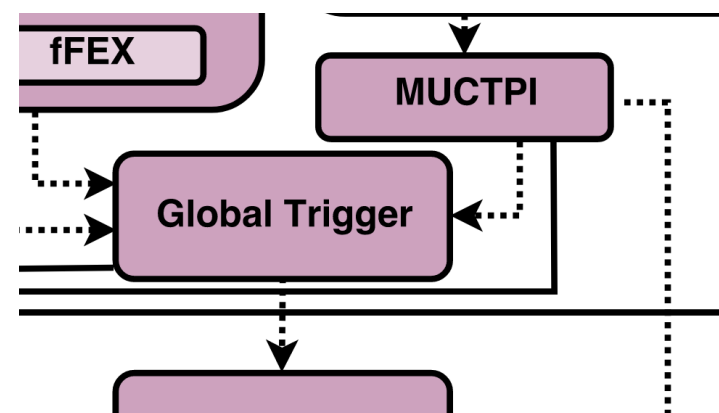
| Subsystem | Trigger Object | Approximate Granularity | Coverage $ \eta $ |
|-----------|---------------------------------------|---------------------------------------|-------------------|
| eFEX | $e/\gamma, \tau$ | Super Cells (10 in 0.1×0.1) | < 2.5 |
| jFEX | $\tau, \text{jet}, E_T^{\text{miss}}$ | 0.1×0.1 | < 2.5 |
| jFEX | $\tau, \text{jet}, E_T^{\text{miss}}$ | 0.2×0.2 | $2.5 - 3.2$ |
| jFEX | $\tau, \text{jet}, E_T^{\text{miss}}$ | 0.4×0.4 | $3.2 - 4.9$ |
| gFEX | Large-R jet, E_T^{miss} | 0.2×0.2 | < 4.9 |
| fFEX | e/γ | Full detector EMEC, HEC, FCal | $2.5 - 4.9$ |
| fFEX | jet | Full detector FCal | $3.2 - 4.9$ |



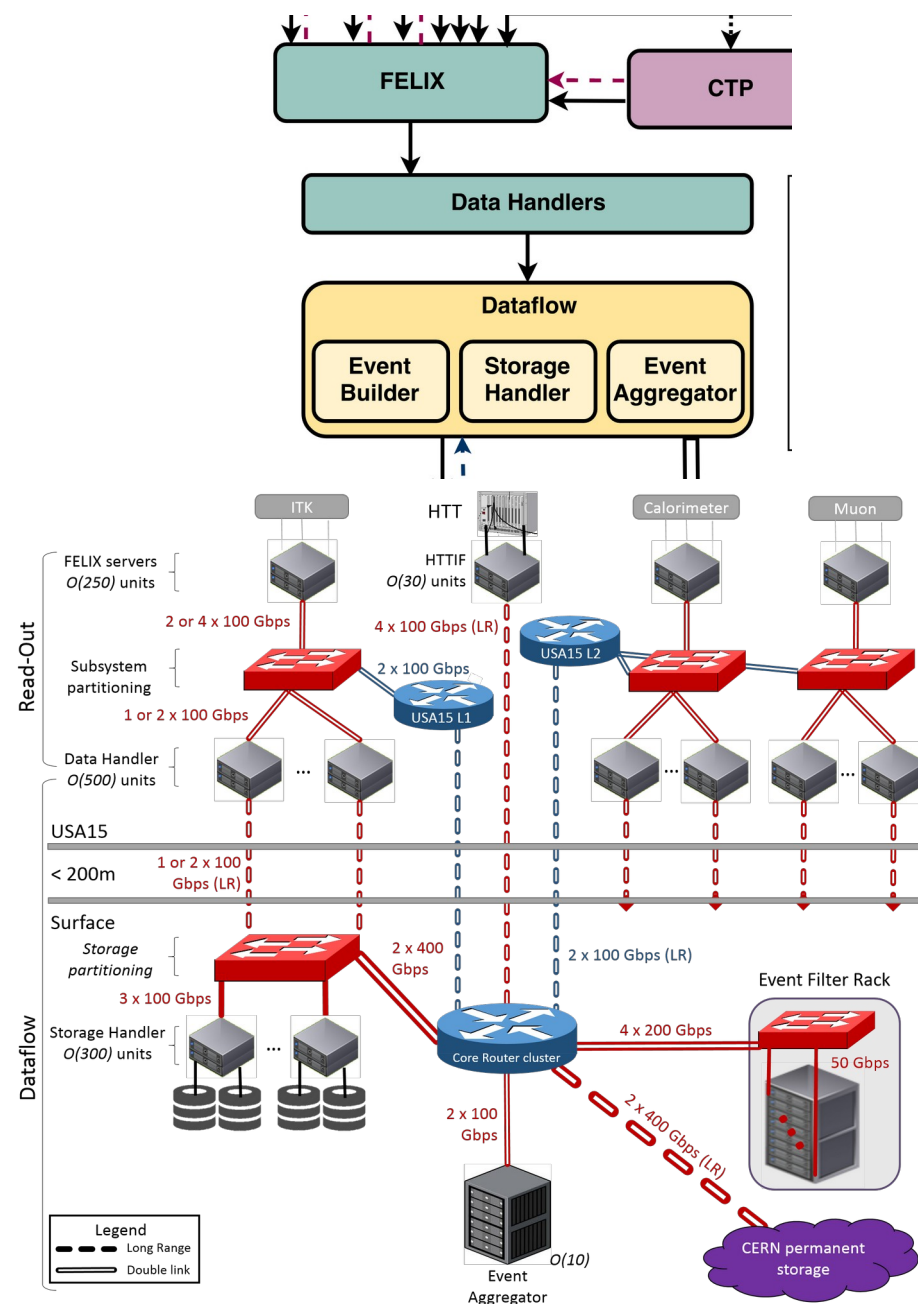
- Muon identification based on muon spectrometer and hadronic calorimeter
 - data processing moved mainly to off-detector electronics
- Major improvements
 - increased acceptance thanks to extended detector coverage (RPC chambers)
 - better momentum resolution by including precision drift chambers (MDT) information
- Selectivity of current Level-1 muon trigger limited by spatial resolution of trigger detectors (RPC, TGC)
 - thanks to MDT \rightarrow p_T resolution close to offline reconstruction
 - significant reduction in trigger rate



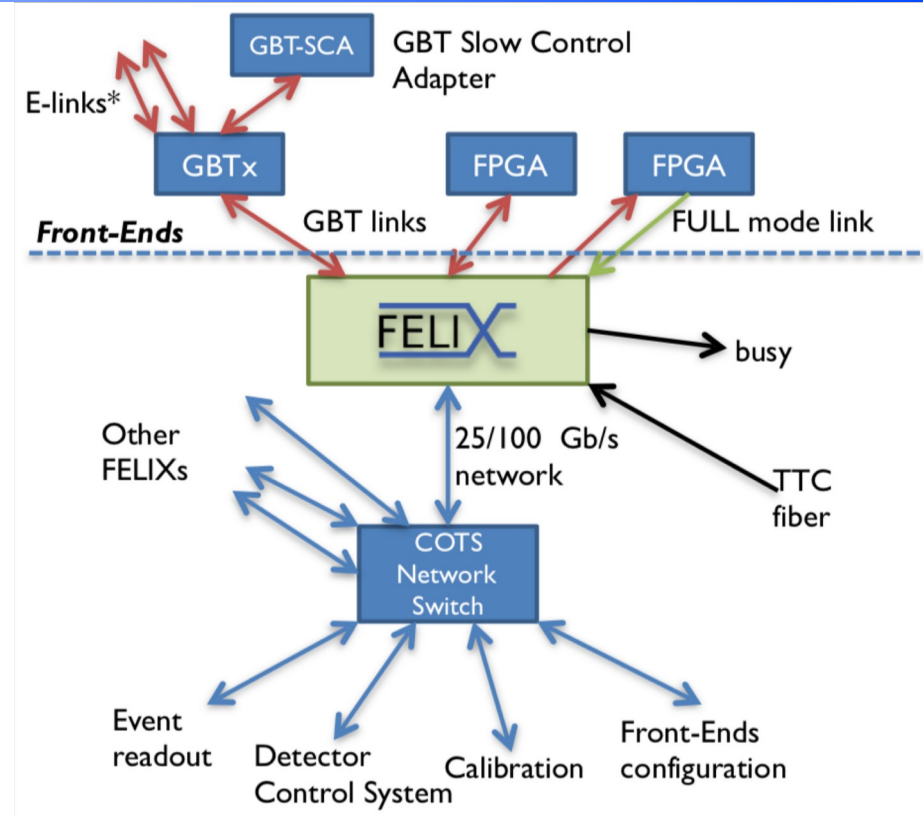
- Complements Level-0 Calo with additional high-granularity energy data and muon information
- Aims to bring Event Filter-like algorithms to the hardware trigger level
 - e.g. topological clusters and “anti- k_T ” algorithm
 - overall event view enables topological selections
- Time-based multiplexing/de-multiplexing design
 - multiple processing boards operating in parallel on different events
 - input and output systems provide data aggregation and serialisation functionalities



- **DAQ infrastructure responsible for**
 - interfacing the detector readout links to a commercial network domain
 - buffering the data and serving them to the Event Filter processors
 - discarding rejected events and formatting selected data for offline transfer
- **Largely implemented with commodity off the shelf hardware**
- **Backbone is a multi-layered sliced network**
 - baseline design based on Ethernet, do not exclude HPC technologies
- **Investigating the use of commodity software**
 - filesystem and cluster management



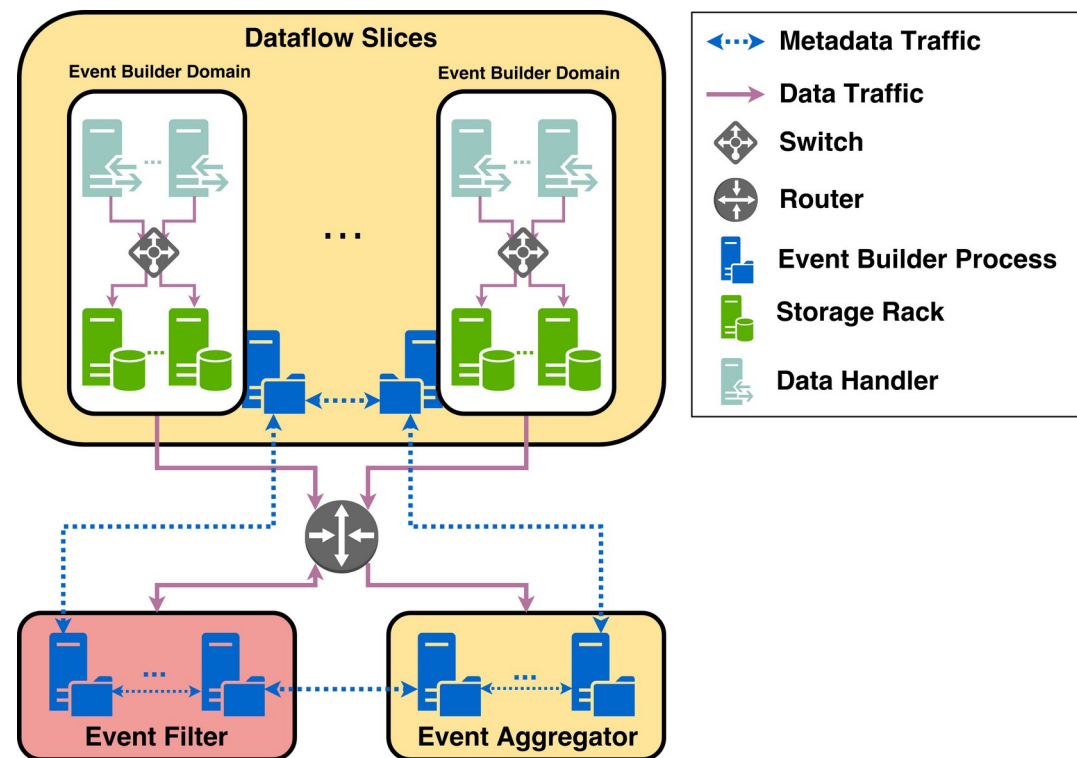
- Detector interfacing relies on a concept being deployed for Run 3
 - extended to the whole ATLAS
- Front-end Link Exchange (FELIX) acts a heterogeneous router
 - translates between network and serial links
 - distributes timing and trigger signals
 - as detector-agnostic as possible
 - *still provision for detector specific firmware*
- Implementation based on commercial servers equipped with custom FPGA-based PCIe interfaces
 - plan for 48 10Gbps links per card
 - ~550 cards serving almost 20000 links
- Detector-specific data processing deferred to dedicated servers
 - “Data Handlers”



Phase-I FELIX Interface Card

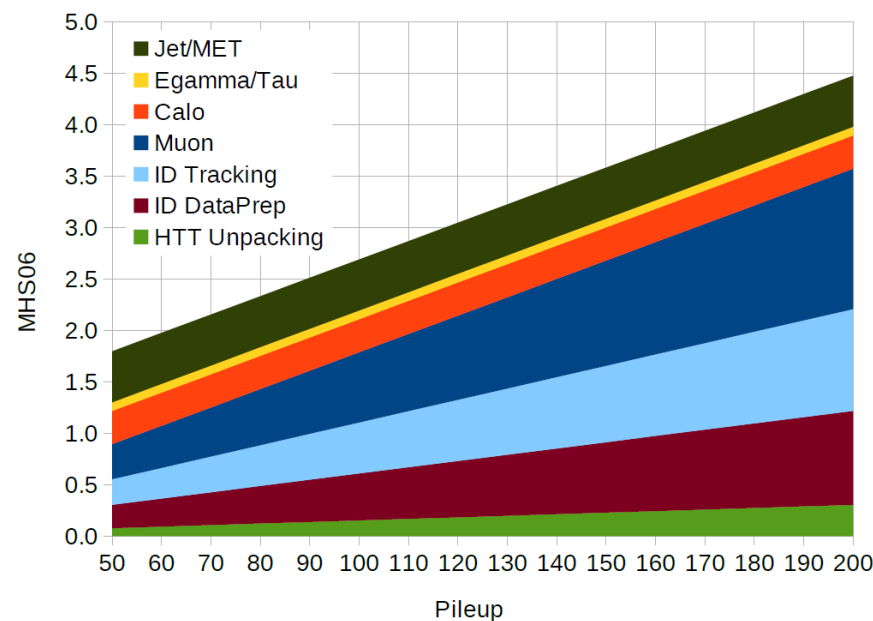
“FELIX: commissioning the new detector interface for the ATLAS trigger and readout system”
N.Ilic, October 3rd

- Extend the DAQ buffering capabilities using a large storage infrastructure
 - decouple real-time domain (Level-0) and software domain (Event Filter)
 - enable delayed processing or fail-over scenarios
- Event building could be either logical or physical
- Event Filter computer farm may be operated similarly to a batch system
 - quasi-real-time data stream required for online physics and detector monitoring

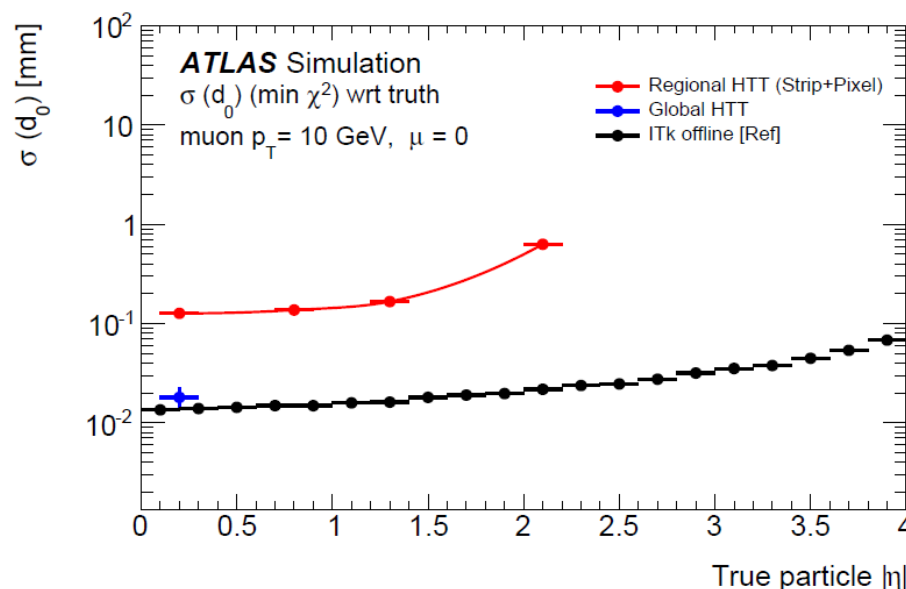
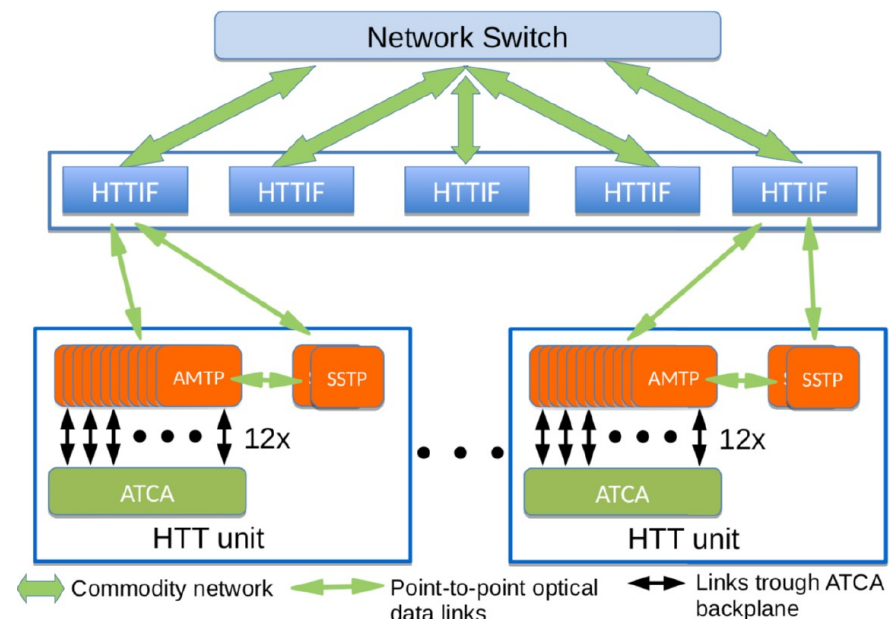


| Component Connection | | Traffic |
|--|--------------------------------------|----------|
| Detector Front-ends to FELIX | | 5.2 TB/s |
| FELIX to Data Handlers | | 5.2 TB/s |
| Data Handlers to Event Builder/Storage Handler | | 5.2TB/s |
| Storage Handler to Event Filter | | 2.6 TB/s |
| Event Filter to HTTIF | Event Filter to rHTT | 175 GB/s |
| | Event Filter to gHTT | 560 GB/s |
| Event Filter to Event Aggregator and Permanent Storage | | 60 GB/s |

- Similar to Run 3 → large computer farm
 - aided by a dedicated tracking system
 - performs the last level of selection from 1 MHz to 10 kHz
- In high pileup environment tracking is key to recover algorithms performance and maintain low thresholds
 - separation of electrons and background jets
 - calculation of global event quantities like $E_{T,miss}$
 - jet energy resolution
- Baseline implementation is based on CPUs
 - assume 3000 dual-socket servers will suffice on the time-scale of Phase-II
 - in parallel investigations of accelerators (GPGPU & FPGA) and associated dedicated algorithms



- Based on current ITk tracking software → 10 times larger computer farm would be required
 - ongoing software optimisations potential to significantly reduce this estimate
- HTT (Hardware Track Trigger) massively parallel performing tracking via Associative Memories (AM ASICs)
 - driven by the Event Filter requests
 - the low latency feature enable a transition into a Level-1 tracking system in the evolved scenario
- Two tracking capabilities
 - rHTT: regional tracking with 8 ITk layers and $p_T > 2$ GeV → support rate reduction to 400 kHz
 - gHTT: global tracking with full ITk data and $p_T > 1$ GeV → support rate reduction to 10 kHz
- In parallel to HTT development, alternative tracking strategies being assessed
 - using commodity hardware platform: software on CPU, accelerators (GPU, FPGA)



Phase-II ATLAS TDAQ Upgrade documented in the Technical Design Report

Major re-implementation of the Trigger & Data Acquisition System

- apply lessons and experience from Run 1/2/3
- take advantage of the technology evolution
- coping with the HL-LHC conditions requires a major scale-up
- specific solutions to specific challenges
 - Global Trigger
 - Hardware Track Trigger
 - Evolution mechanism



Bonus