NEC'2019

Design of the front-end electronics based on multichannel IDEAS ASICs for Silicon and GEM detectors

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JINR VBLHEP

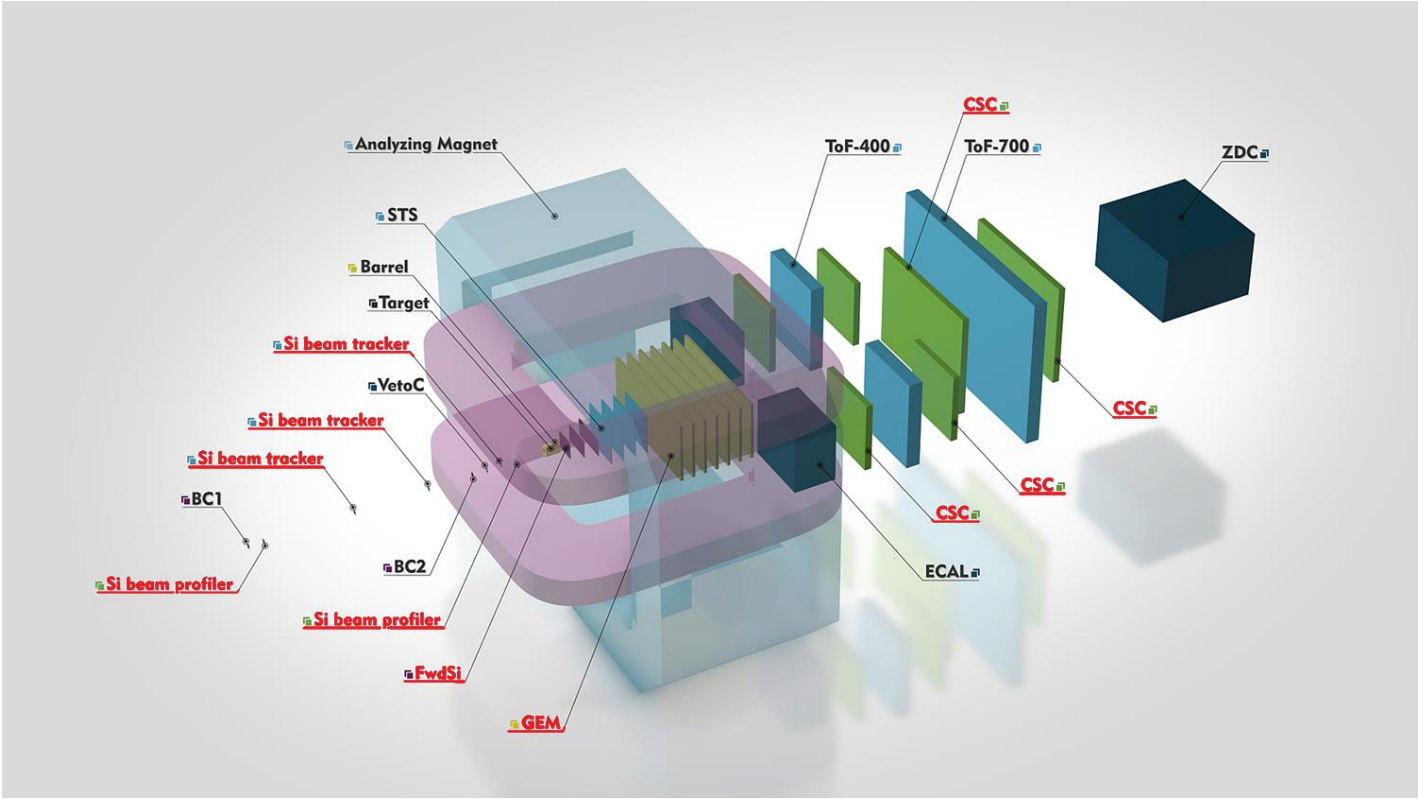
Using of IDEAS ASICs for BM@N facility

Current FEE BM@N configuration (March 2018) is based on ASICs provided by commercially company (IDEAS) for next detectors:

- Forward Silicon Detector;
- GEMs (Gas Electron Multiplier);
- CSC (Cathode Strip Chamber).

According to upgrade plans for BM@N FEE for new detectors also will be based on the IDEAS ASICs:

- Si beam tracker;
- Si beam profilometer;
- Forward Silicon Tracking Detectors.



[http://bmn.jinr.ru/about/]

Number of Forward Silicon Tracking Detector channels for BM@N experiment

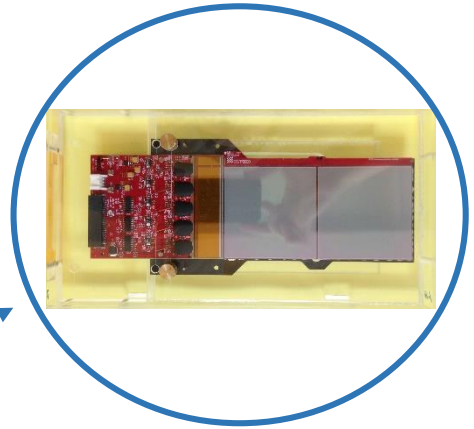
Forward Silicon Tracking Detectors

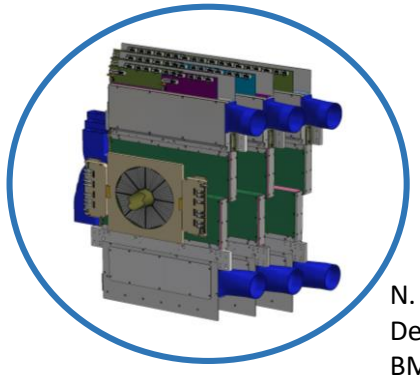
- 3 coordinate planes

Total detector modules: 42.
The total number of measuring channels: 53760.

Three coordinate planes

- 10 detector modules;
- 14 detector modules;
- 18 detector modules.





N. Zamyatin
Detector council
BM&N meeting,
09.04.19

Detector module

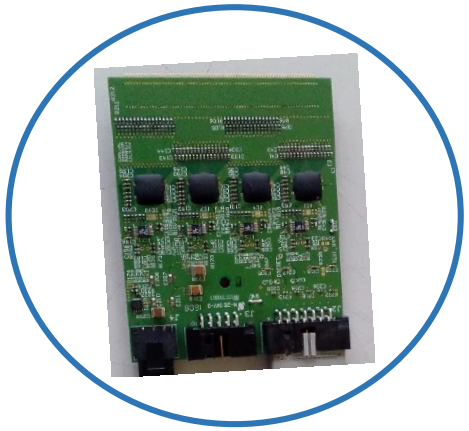
- 1280 channels:
  - Double-sided Silicon Strip Detectors;
  - 10 VATAGP7.1 IDEAS ASICs;
  - 128 ch/chip.

Number of GEM Tracking System channels for BM@N experiment

GEM Tracking System

- 7 GEM planes

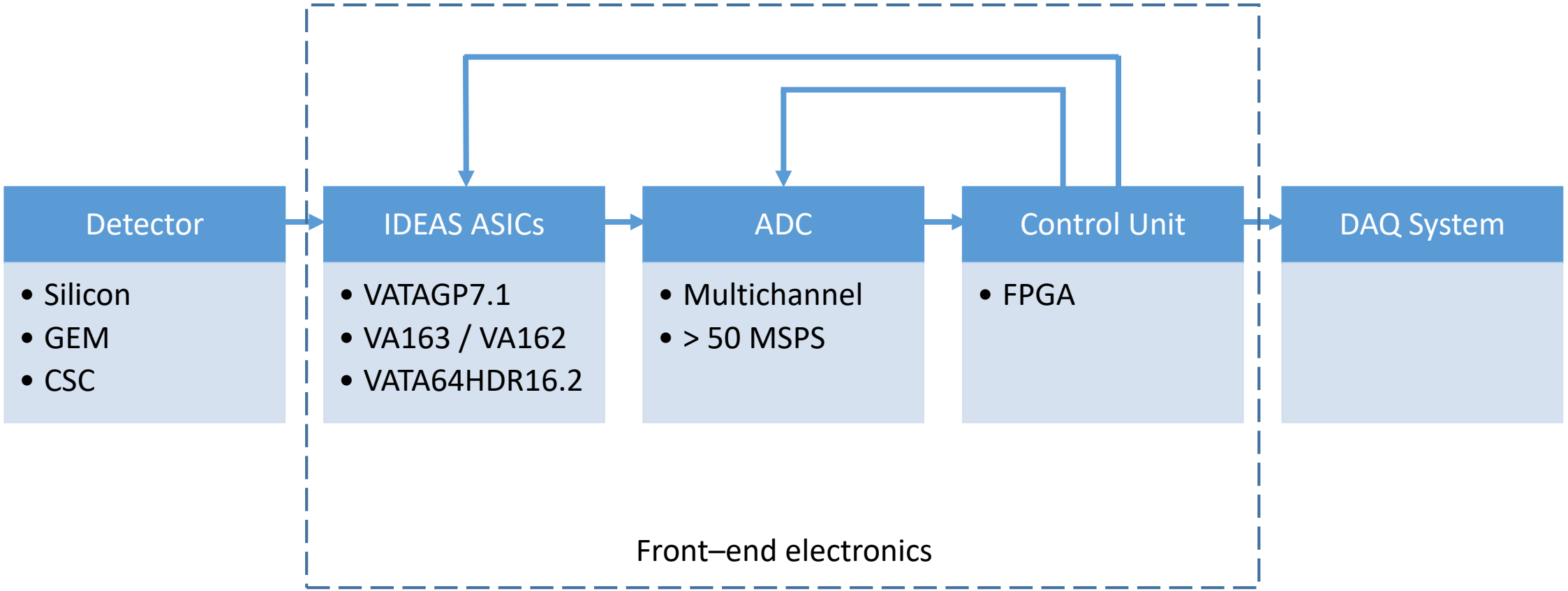
The total number of measuring channels: 89600.



GEM plane

- 6400 channels:
  - 50 FEE boards;
  - 4 VA163 IDEAS ASICs;
  - 32 ch/chip.

Front-end electronics block diagram

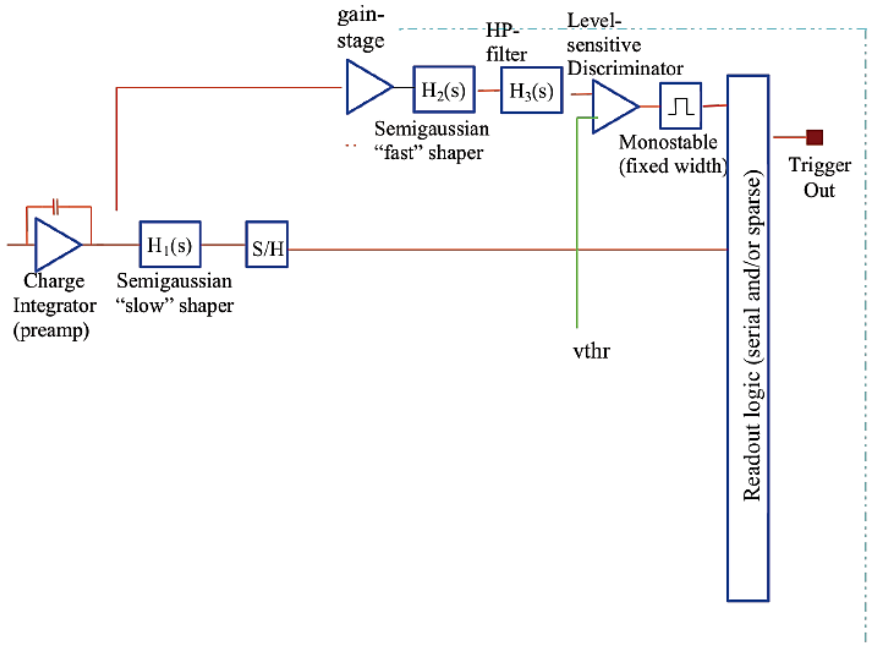


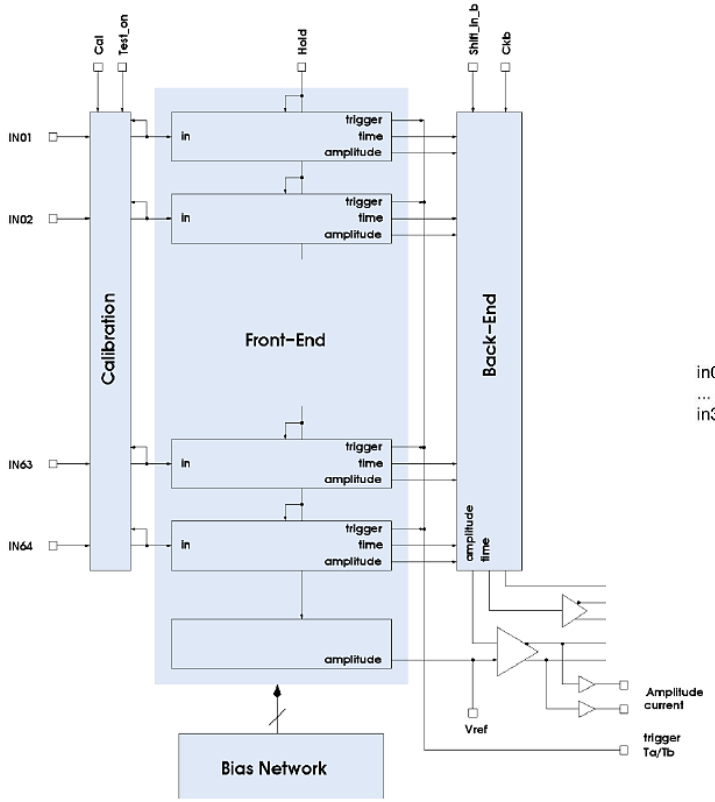
IDEAS ASIC's features

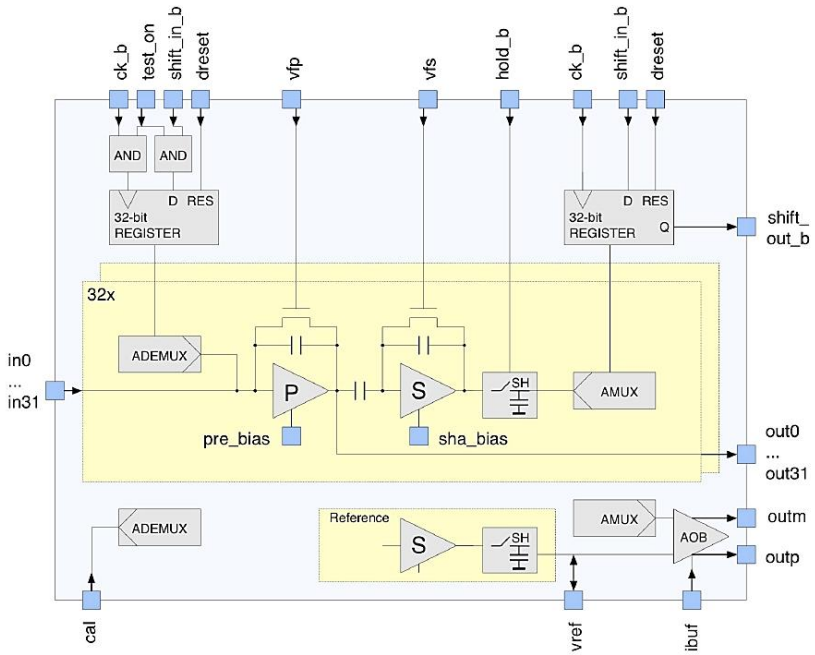
	VATAGP7.1	VATA64HDR16.2	VA32HDR11	VA163	VA162
Number of channels	128	64	32	32	32
Input charges	-30fC ÷ +30fC	-20pC ÷ +55pC	-35pC ÷ +25pC	-750fC ÷ +750fC	-1.5pC ÷ +1.5pC
Shaping time	500ns	50/100/150/300ns	0.9µs	500ns	2 ÷ 2.5µs
Noise	70e^- ENC + 12e^-/pF	1fC	13000e^- ENC	1797e^- ENC at 120pF load	2000e^- ENC at 50pF load
Gain	20µA/fC	2-gain settings	36 µA/pC	0.88µA/fC	0.5µA/fC
1 analogue multiplexed output	✓	✓	✓	✓	✓
Time-to-amplitude converter		✓			
Self-trigger	on-chip		with IDEAS TA32cg2		
Application	are used for Forward Silicon Detector	will be used for Si beam tracker	will be used for Si beam profilometer	are used for GEMs, CSC	were used for GEMs, CSC

IDEAS ASIC’s functional description

VATAGP7.1	VATA64HDR16.2	VA162





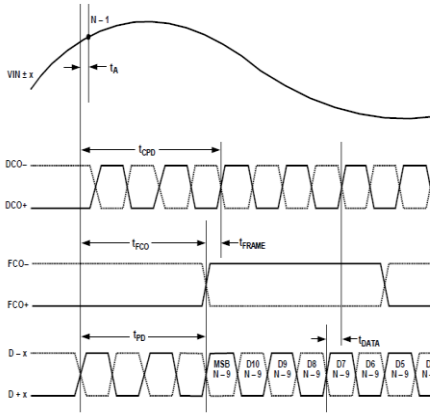


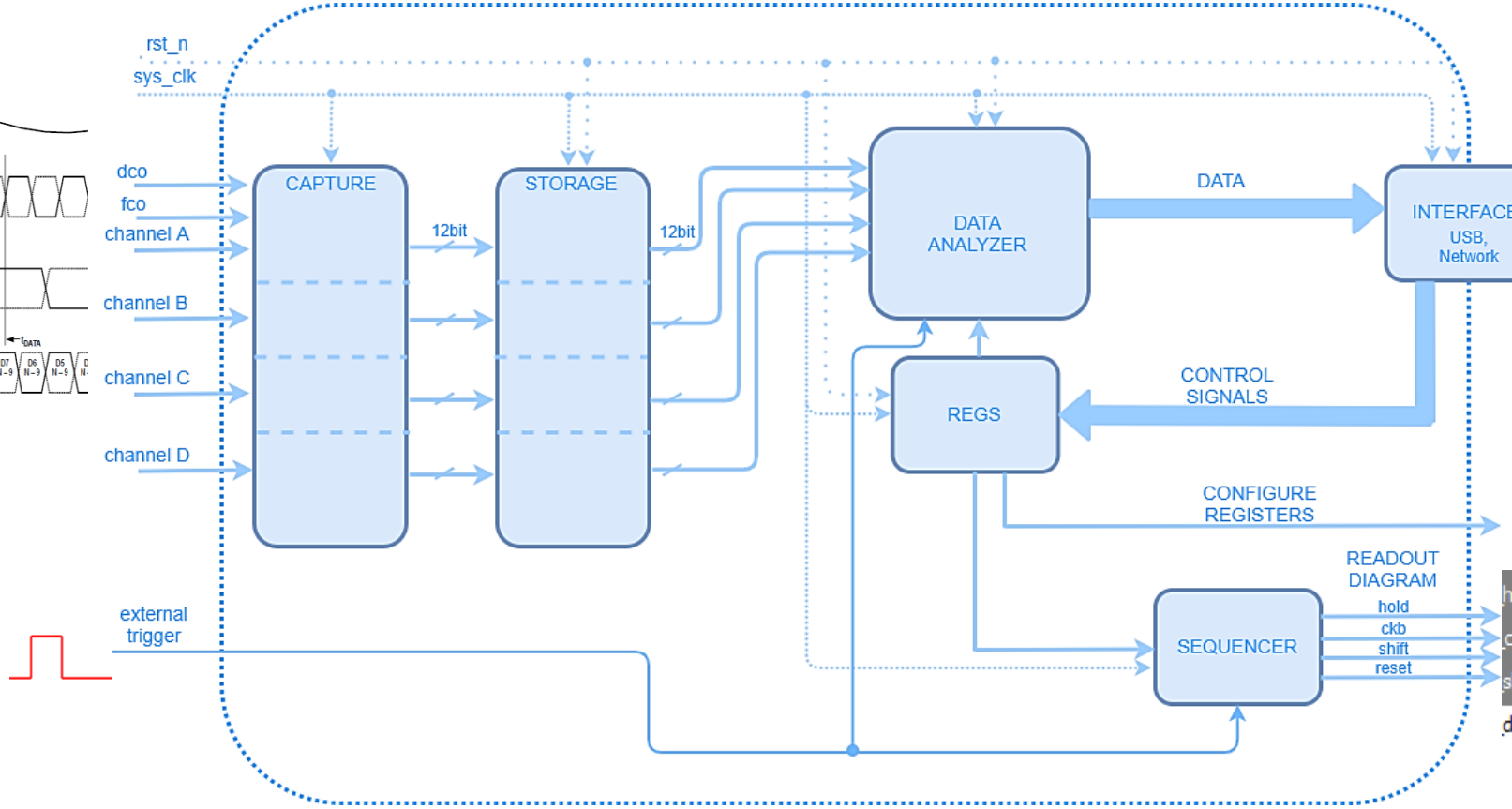
[VATAGP7.1
IDEAS DATASHEET:
128 Channel Silicon Detector Readout with Trigger]

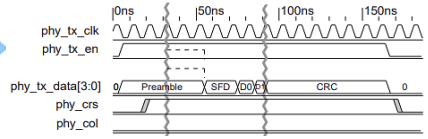
[VATA64HDR16.2 IDEAS DATASHEET]

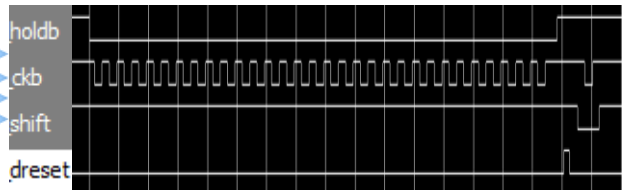
[VA162 IDEAS DATASHEET:
32 CSAs with Pre-amplifier Outputs,
Sample-and--Hold and Multiplexer Output]

FPGA Design

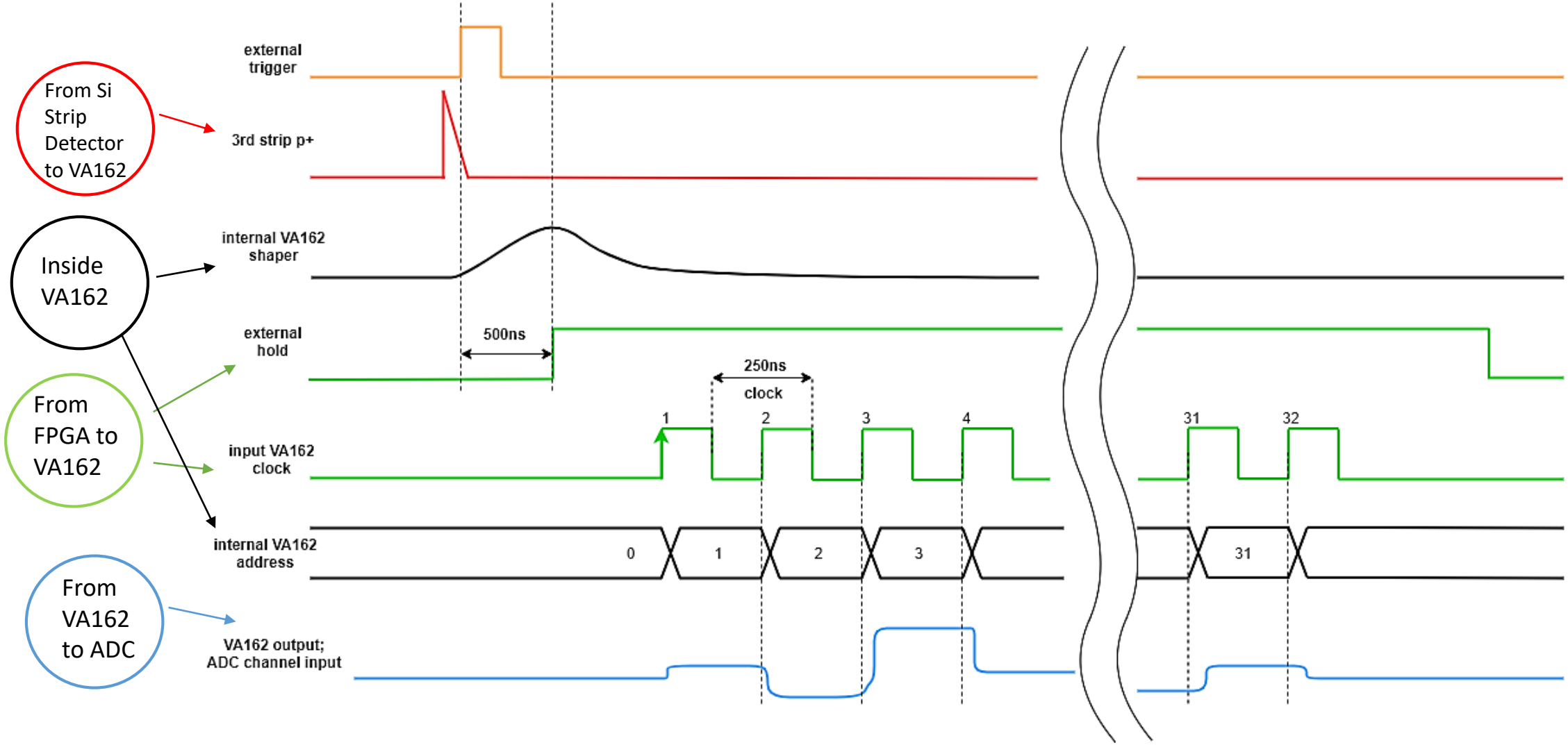

DCO-
DCO+
FCO-
FCO+
D-x
D+x


rst_n
sys_clk
dco
fco
channel A
channel B
channel C
channel D
CAPTURE
12bit
STORAGE
12bit
DATA ANALYZER
DATA
INTERFACE: USB, Network
REGS
CONTROL SIGNALS
CONFIGURE REGISTERS
READOUT DIAGRAM
hold
ckb
shift
reset
SEQUENCER
external trigger

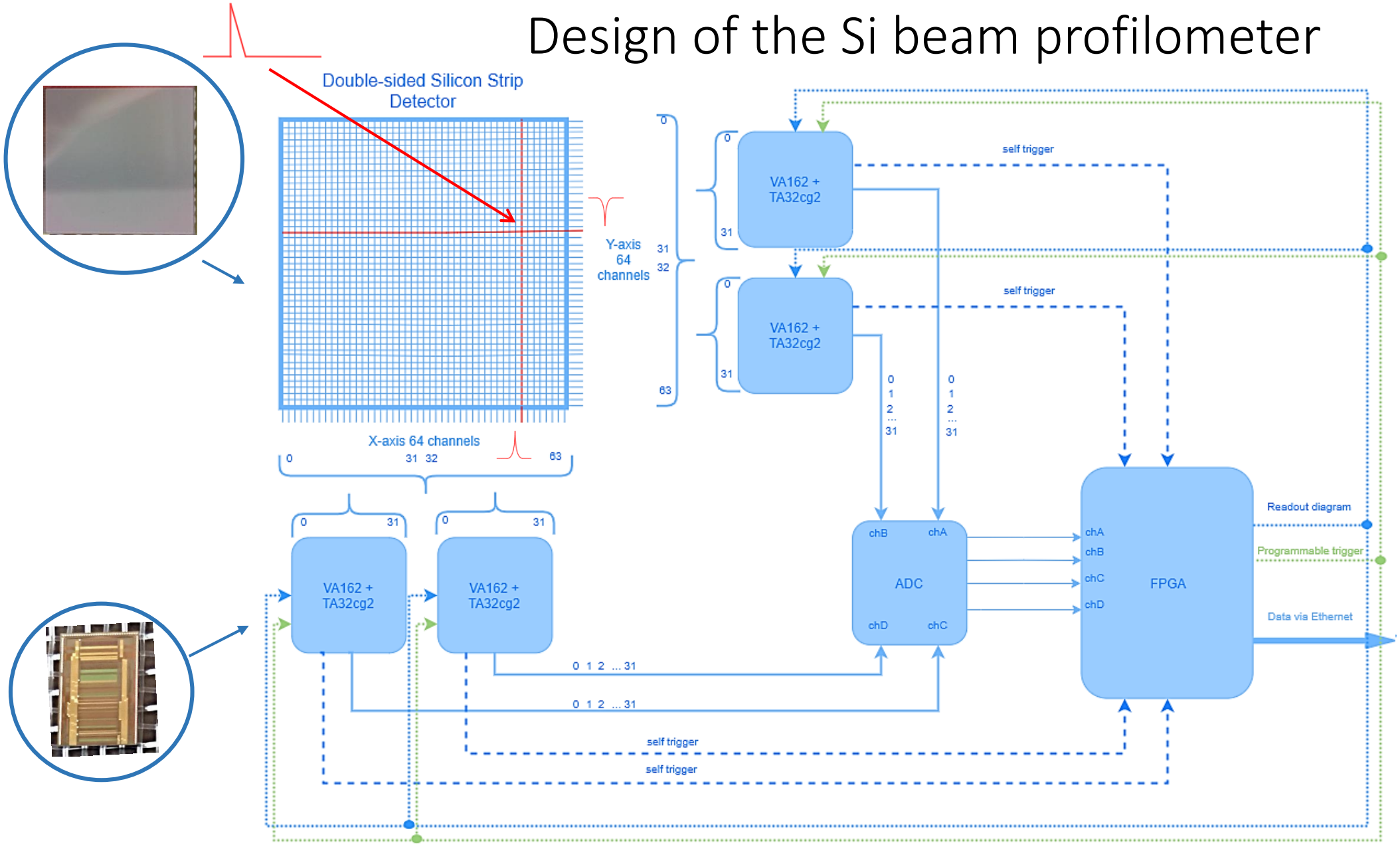

0ns
50ns
100ns
150ns
phy_tx_clk
phy_tx_en
phy_tx_data[3:0]
phy_crs
phy_col
Preamble
SFD
CRC


holdb
ckb
shift
dreset

Event readout



Design of the Si beam profilometer



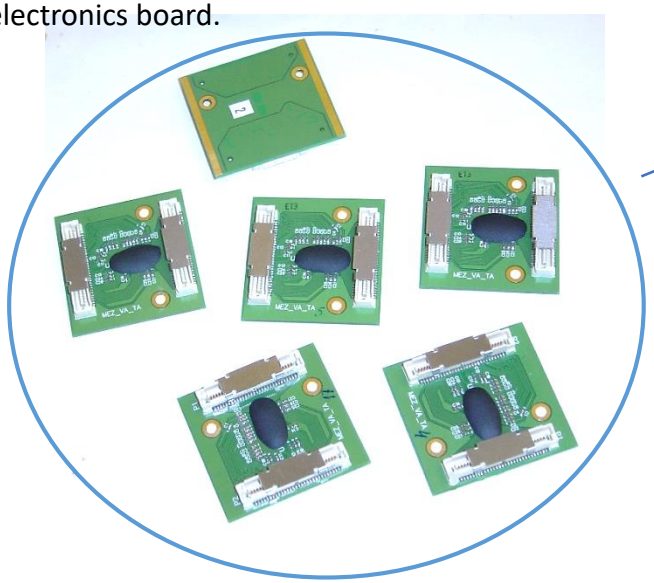
Configuration TA32cg2 registers:

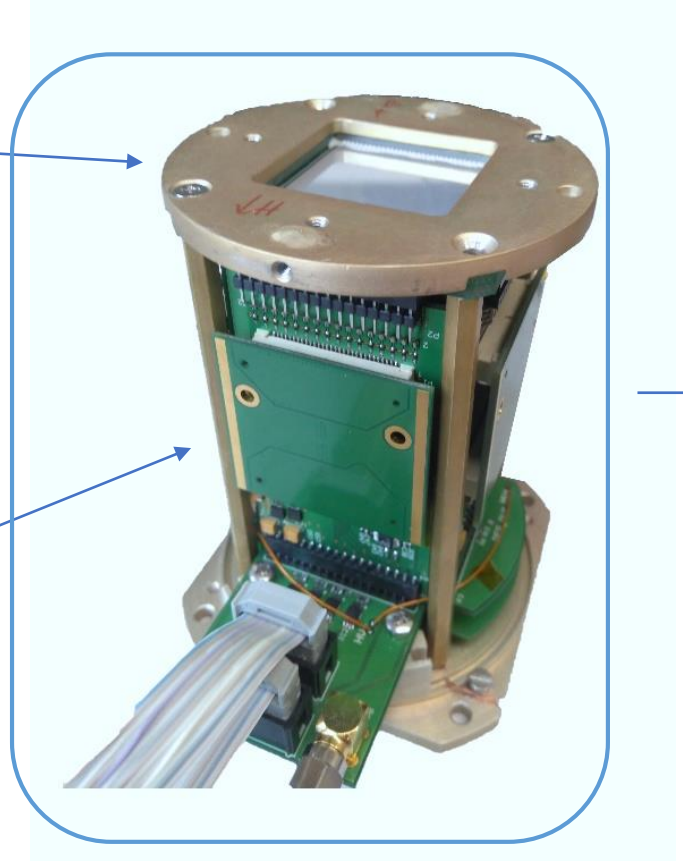
- pre-amplifier gain;
- pre-amplifier input potential;
- trigger disable for each 64 channels;
- trigger threshold;
- test channel.

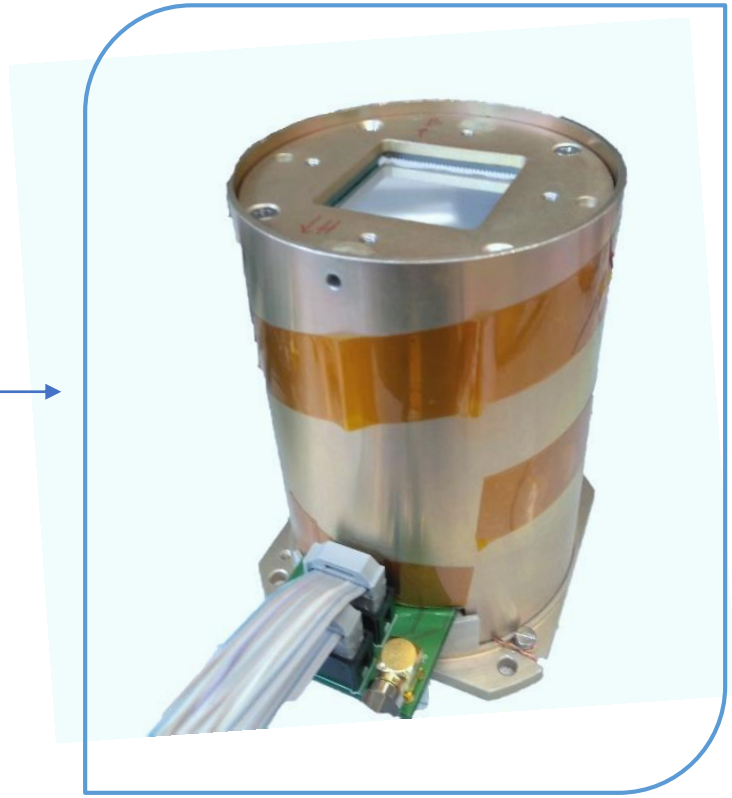
Si beam profilometer prototype

Double-sided Silicon Strip Detector

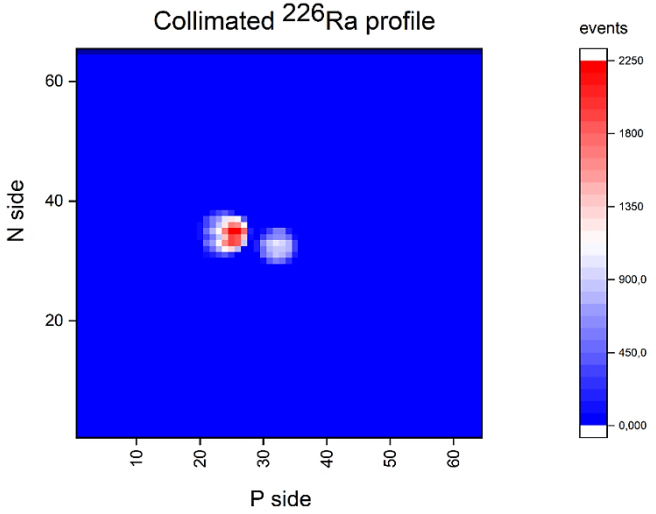
A mezzanine card with one or two (VA+TA) of the IDEAS ASICs might be plugged into another front-end electronics board.

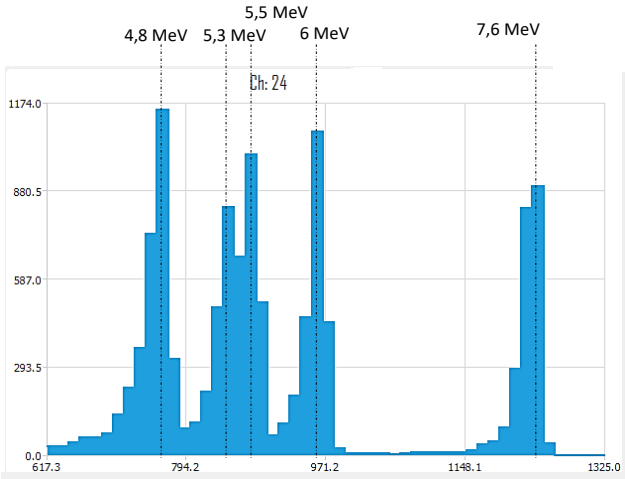


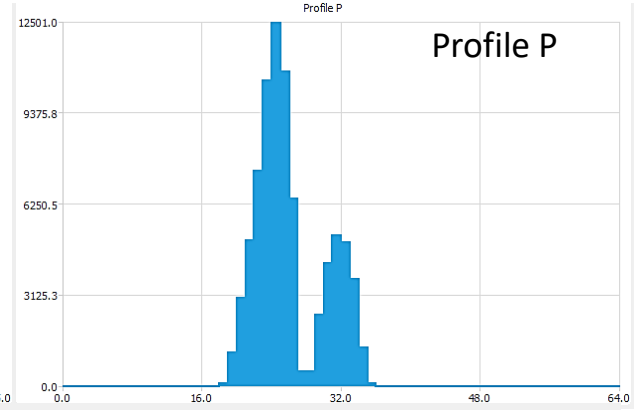


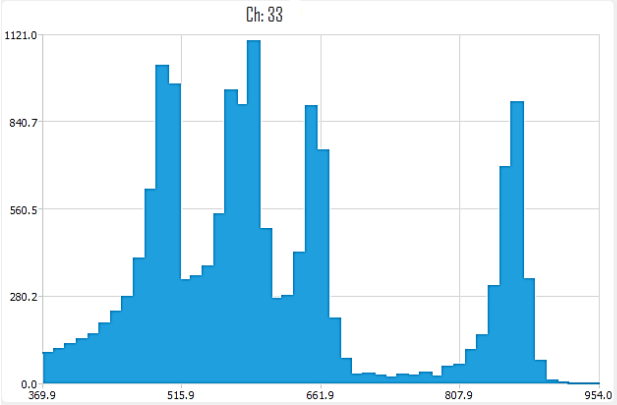


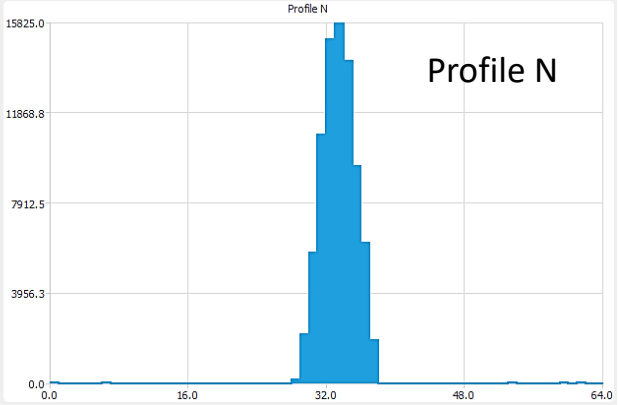
Test with collimated ^{226}Ra (VA162)



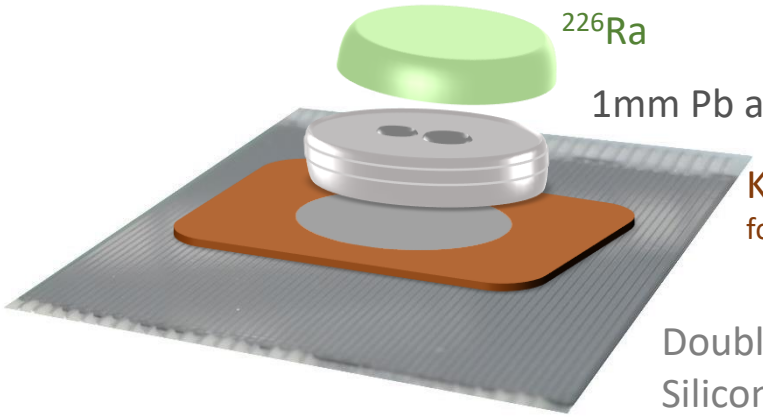








Experimental setup (no vacuum)

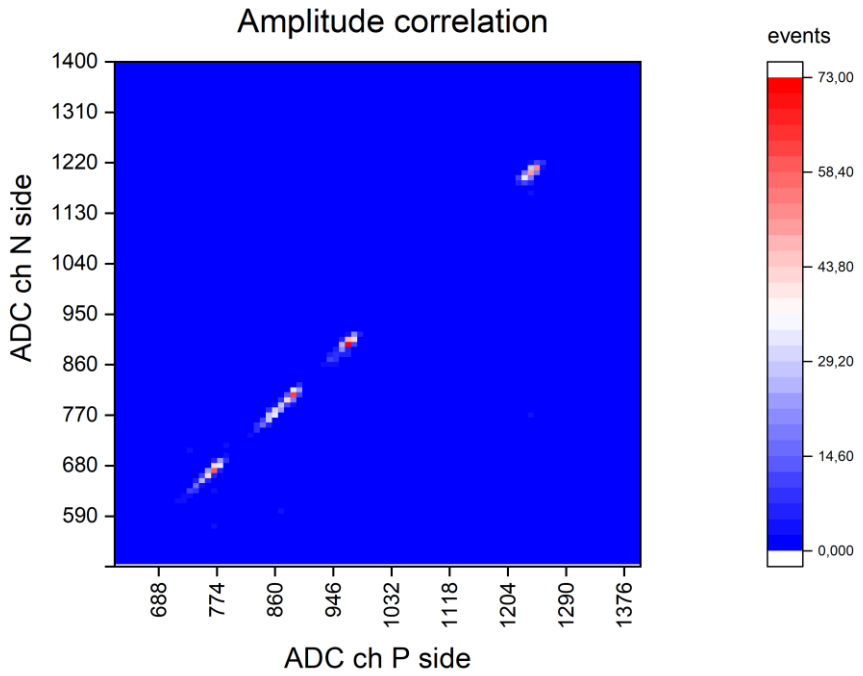


^{226}Ra

1mm Pb as a collimator

Kapton layer
for electrical insulation strips

Double-sided
Silicon Strip Detector
(64x64 strips; size 35x35mm)



Conclusions

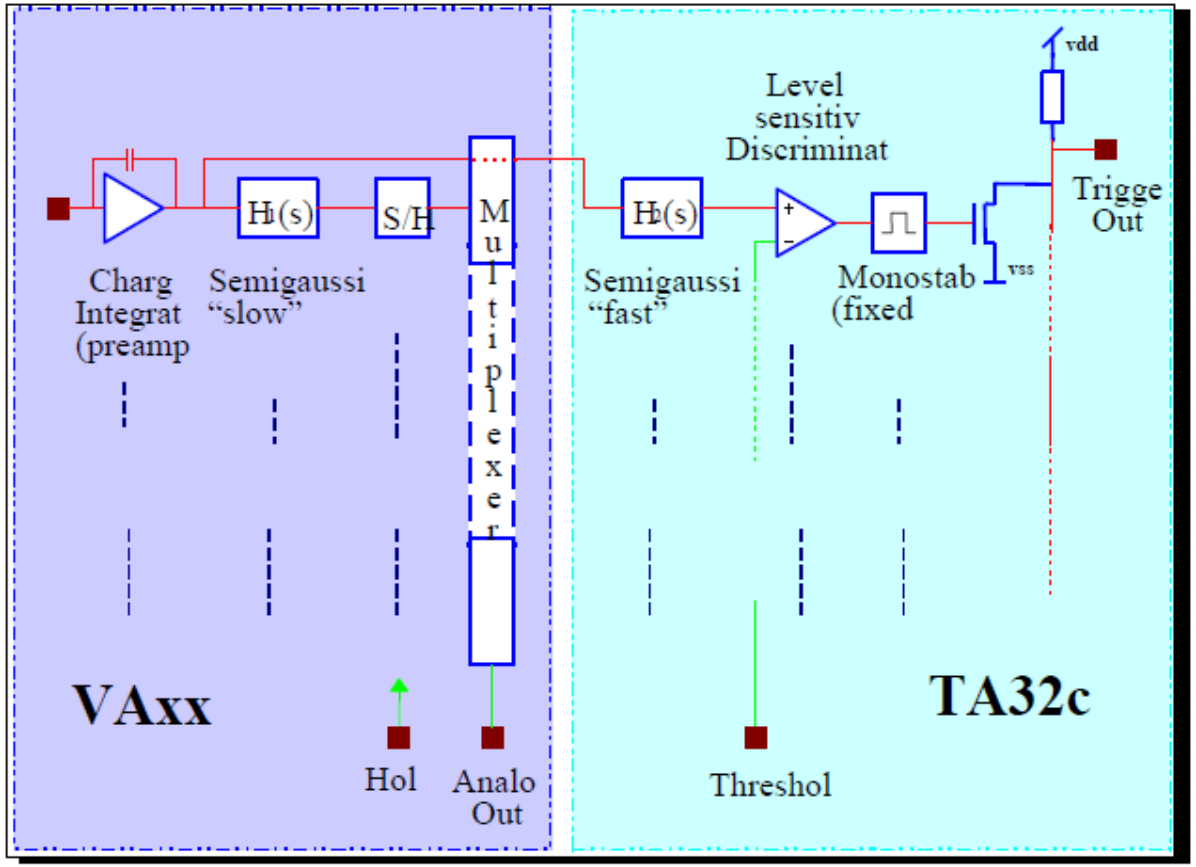
- IDEAS (Norway) produces multichannel (32, 64, 128), commercially available ICs with wide input charge range for front-end readout of ionizing radiation detectors;
- FEE based on IDEAS ASICs for Silicon Detector, GEMs, CSC were successfully run for BM@N experiment in March 2018;
- The Si beam profilometer prototype (FEE based on IDEAS VA162 and FPGA readout) has been designed and tested with ^{226}Ra.

Plans

- Front-end readout electronics are being designed for upgraded BM@N experiment for:
  - Forward Silicon Tracking Detector (3 coordinate planes);
  - 3 Silicon beam trackers;
  - 2 Silicon beam profilometers;
  - GEMs.

Acknowledgments

I would like to show gratitude to Nikolay Zamyatin for result discussions and tests, and to Evgeniy Zubarev for design and manufacture of structures.

TA32cg2 & TA32cg3

	TA32cg2	TA32cg3
Number of channels	32	
Peaking time	75-150 ns	75-100 ns
Threshold DACs	3 x 32bit DAC-mask	
Gain	Programmable	
Polarity	Negative or positive