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Design of the front-end electronics based on multichannel IDEAS ASICs for silicon and GEM detectors

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IDEAS ASICs are designed for the front-end readout of ionizing radiation detectors and produced by commercial fabless IC supplier –Integrated Detector Electronics AS (Norway). IDEAS ASIC is a multichannel (32/ 64/ 128) chips. Each chip channel has pre-amplifiers, shaper and multiplexed analogue readout. It's necessary to configure internal chip registers, control analogue readout and transmit data from each measuring channel to DAQ System. These are basic functions of Control Unit based on FPGA. Design of the front-end electronics for silicon and GEM detectors consists of IDEAS IC, ADC and Control Unit.

Current FEE BM@N configuration (March 2018) is based on IDEAS ASICs for Forward Silicon Detector, GEM detectors and CSC. According to upgrade plans for BM@N FEE for Si beam tracker, Si beam profiler, Forward Silicon Tracking Detectors also will be based on the same ASICs. This paper presents the design of the front-end electronics of the BM@N Si beam profiler:

- Double-Sided Silicon Detectors –a coordinate plane with 2x128 measuring channels;
- IDEAS ASICs –the front-end readout of DSSD;
- Analog Devices ADC;
- FPGA Xilinx –Control Unit.

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