Multi-channel pulse counter based on the Altera FPGA

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JUNO experiment: Physics and layout

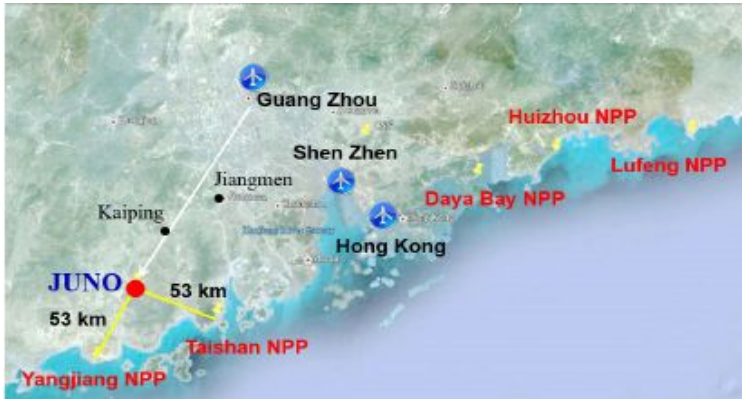
Main goals:

- Neutrino mass hierarchy
- Precision of neutrino oscillation parameters $\Delta m^2_{21}, \Delta m^2_{32}, \sin^2\theta_{12}$ below 1%

Other:

- Astroparticle physics
- SN bursts, diffuse SN neutrinos
- Solar neutrinos
- Atmospheric neutrinos
- Geoneutrino (U+Th neutrino flux)
- Indirect DM search

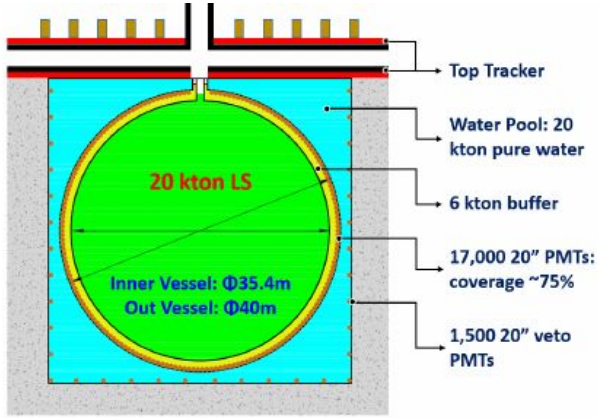
Kaiping, Jiangmen, Guangdong

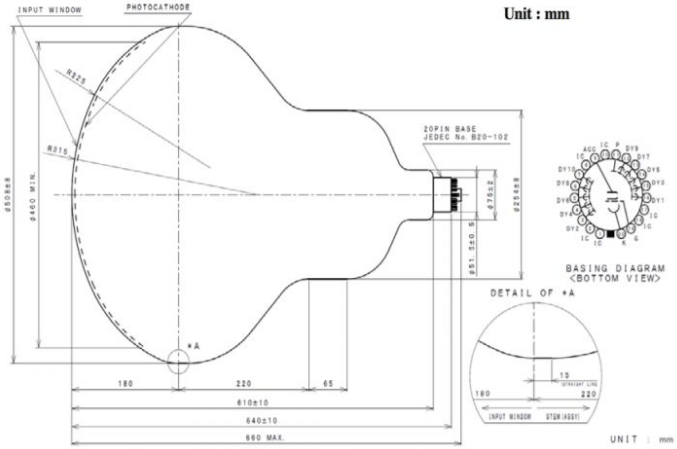


JUNO experiment: Detector

PMTs requirements:

- High and uniform quantum efficiency
- Good SPE detector capability
- Large dynamic range
- Low noise rate
- High reliability
- Long lifetime



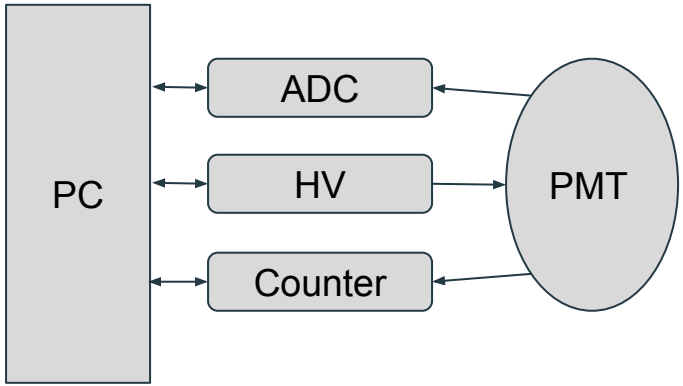


PMT testing: Ongoing status

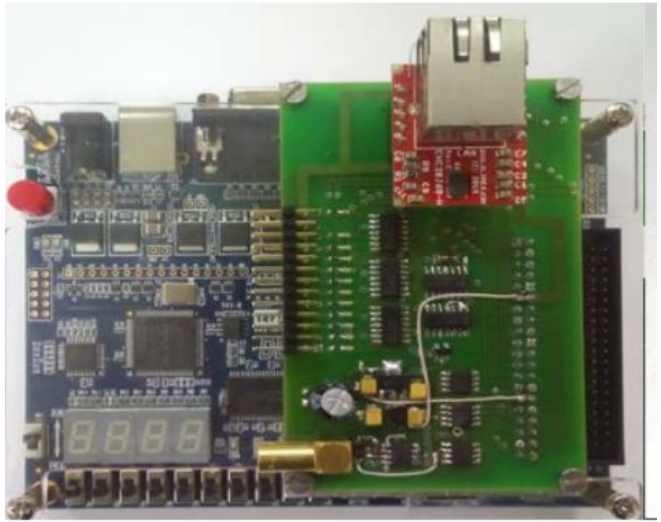
~20 000 LPMTs are being tested:

- **PMT scanning station: precise measurements**
- **Container system:**

Long-term stability tests are to be carried out

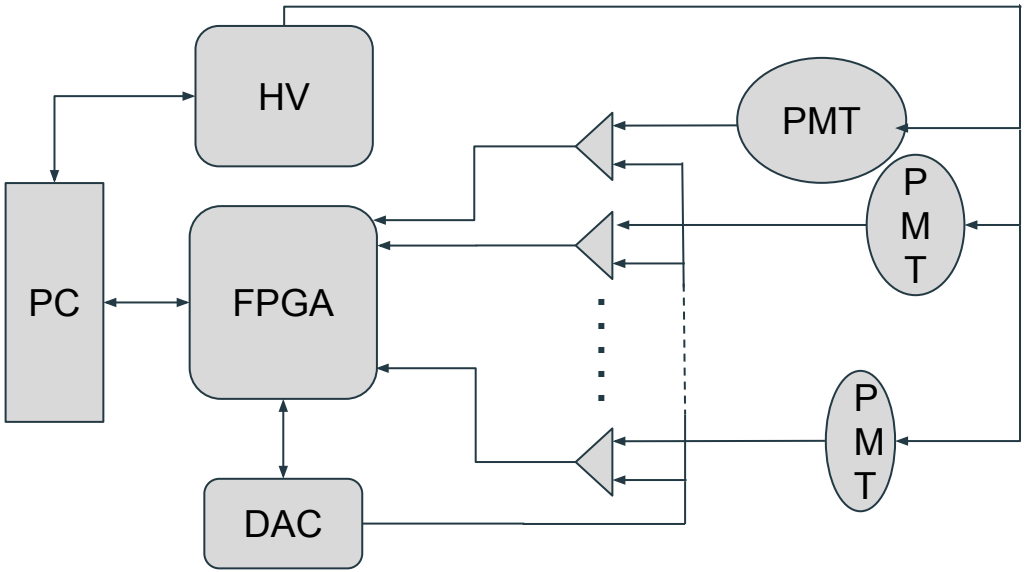


Control block for PMT scanning station

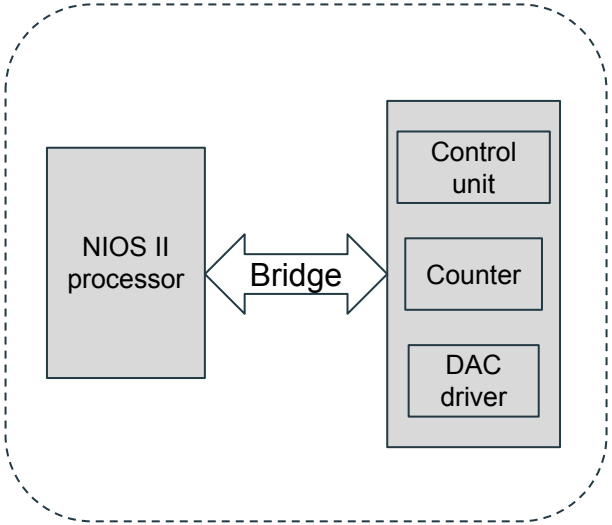


Multi-channel counter

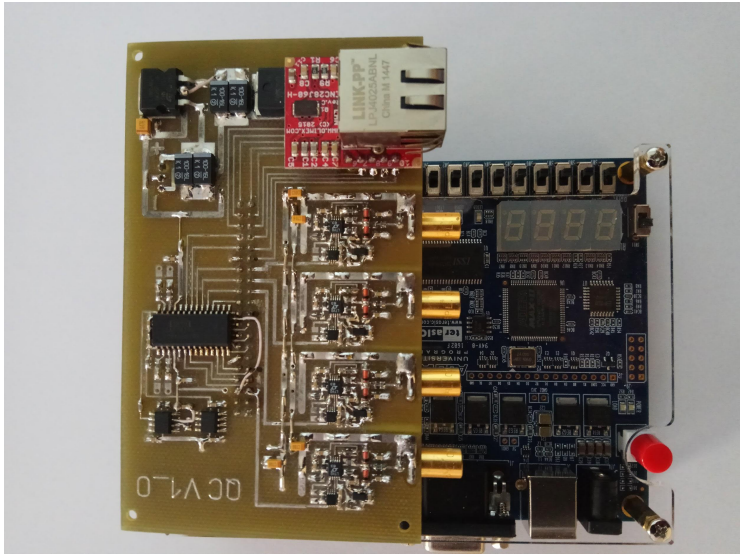
Conceptual design



FPGA layout



Multi-channel counter: first prototype



Quad-channel pulse counter

- Altera DE0 Development and Education Board
- Texas Instruments 12-Bit Quad Voltage Output DAC7624
- Linear Technology 4ns, 150MHz Dual Comparator
- Olimex ENC28J60-H Development Board

Inner blocks
Control unit, counter, DAC driver
Mealy machine
Verilog/System Verilog HDL

NIOS II CPU
Altera IP Core

Software core
UDP listener over Ethernet
Infinite cycle C

Multi-channel counter: ongoing status

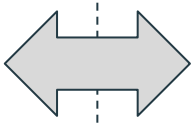
KEYSIGHT 33600A Series Waveform Generator tests:

Rectangular pulses ⟶ Missing events

100kHz ⟶ 999995 counts

1MHz ⟶ 999956 counts

10MHz ⟶ 99999547 counts



On-board MEC oscillator:

Frequency stability from manufacturer

±25ppm - ±100ppm

Aging factor

±3ppm/year (25°C)

Multi-channel counter: status & future prospects

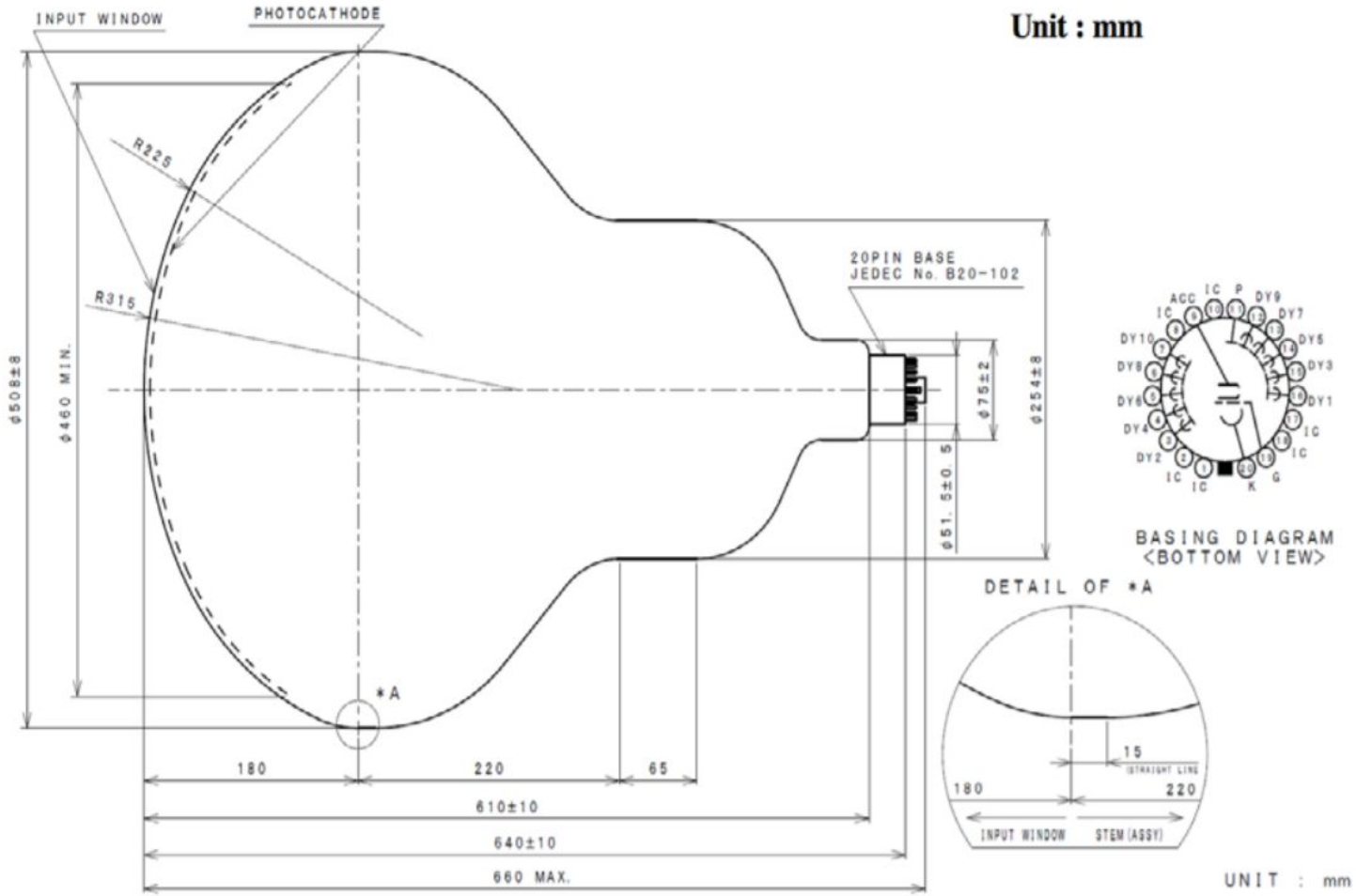
What has been done:

- DAC driver and quad-channel pulse counter (Verilog HDL)
- UDP server (C)
- Library for encoding/decoding of input and output FPGA data (C)
- Command-line user interface (C, Python)
- Scale the project for more channels (logic part of the firmware)
- Graphical user interface (Python, Tkinter) - has not been finished yet

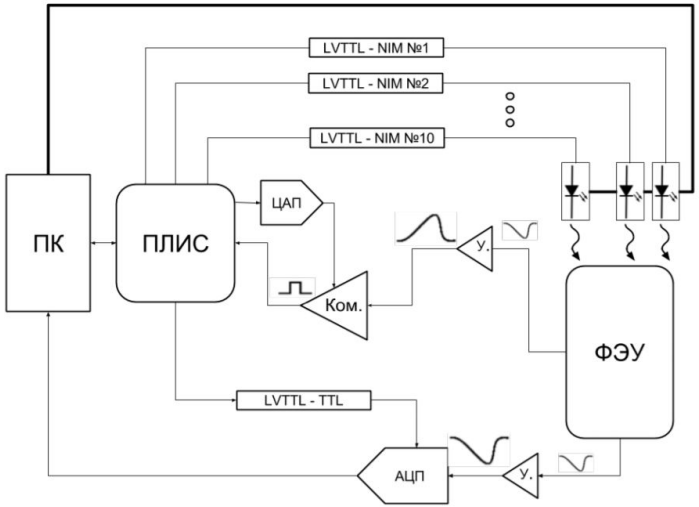
To be done:

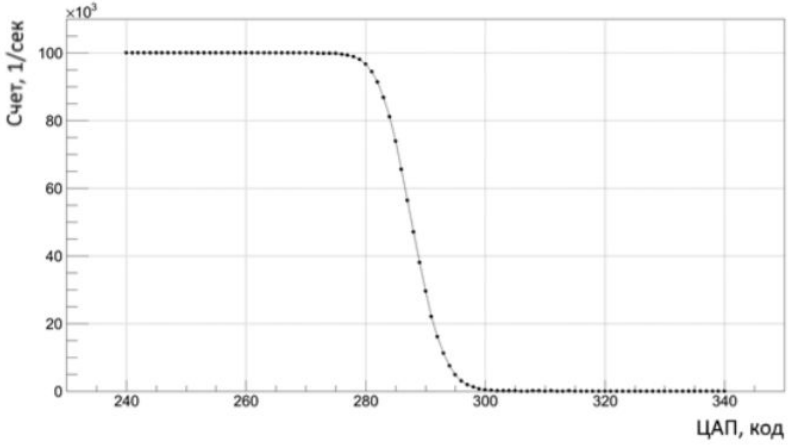
- Perform channels voltage calibration
- Perform tests with true noise signals (PMT, SiPM)
- Move to another FPGA board

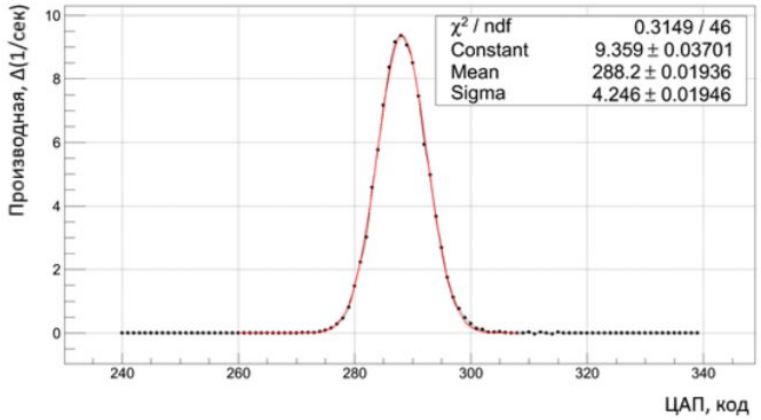
Thank you for your attention!

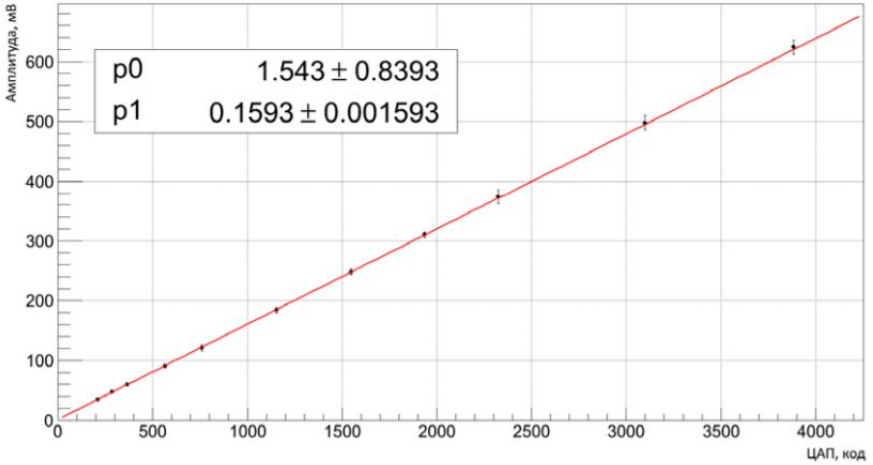

Unit : mm
INPUT WINDOW
PHOTOCATHODE
R225
R315
φ508±8
φ460 MIN.
20PIN BASE
JEDEC No. B20-102
φ75±2
φ254±8
φ51.5±0.5
*A
180
220
65
610±10
640±10
660 MAX.
BASING DIAGRAM
<BOTTOM VIEW>
DETAIL OF *A
15
STRAIGHT LINE
180
220
INPUT WINDOW
STEM (ASSY)
UNIT : mm

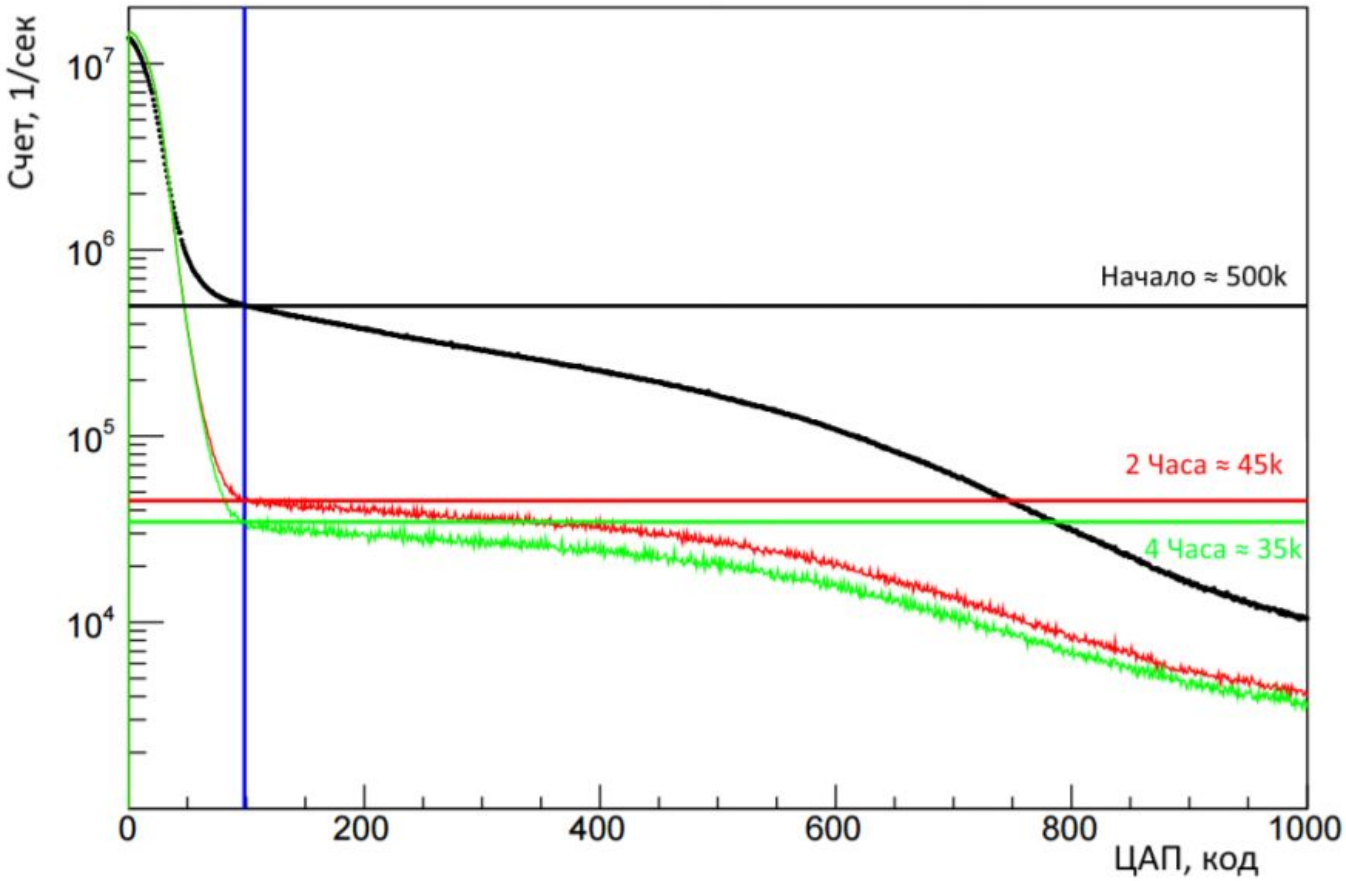

импульсные источники света
Вращающаяся дуга


LVTTL - NIM №1
LVTTL - NIM №2
LVTTL - NIM №10
ПК
ПЛИС
ЦАП
Ком.
У.
ФЭУ
LVTTL - TTL
АЦП
У.


Счет, 1/сек
×10³
100
80
60
40
20
0
240
260
280
300
320
340
ЦАП, код


Производная, Δ(1/сек)
10
8
6
4
2
0
240
260
280
300
320
340
ЦАП, код
χ² / ndf 0.3149 / 46
Constant 9.359 ± 0.03701
Mean 288.2 ± 0.01936
Sigma 4.246 ± 0.01946


Амплитуда, мВ
600
500
400
300
200
100
0
0
500
1000
1500
2000
2500
3000
3500
4000
ЦАП, код
p0 1.543 ± 0.8393
p1 0.1593 ± 0.001593


Счет, 1/сек
10^7
10^6
10^5
10^4
Начало ≈ 500k
2 Часа ≈ 45k
4 Часа ≈ 35k
0
200
400
600
800
1000
ЦАП, код