1	Name	CrateSerial	Slot	BoardSerial
2				
3	TDC72VHL	0x076D3892	18	0x076D180A
4	TDC72VHL	0x076D3892	20	0x06E9DA9E
5	TQDC16VS	0x076D3892	13	0x046F0C75
6				

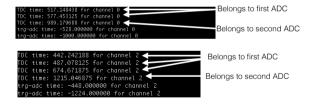
1					
2	Det	Mod	Serial	Slot	Channel
3					
4	TQDC_BC1	2	0x076D3892	13	0
5	TQDC_BC2	2	0x076D3892	13	9
6	TQDC_VC	2	0x076D3892	13	12
7	BC1	1	0x076D3892	18	14
8	BC2	0	0x076D3892	18	9
9	BC2	1	0x076D3892	18	18
10	BC3	0	0x076D3892	18	4
11	BC3	1	0x076D3892	18	6
12	VC	0	0x076D3892	18	0
13	VC	1	0x076D3892	18	10
14	BD	0	0x076D3892	18	12
15	BD	1	0x076D3892	18	42
16	BD	2	0x076D3892	18	46
17	BD	3	0x076D3892	18	39
18	BD	4	0x076D3892	18	38
19	BD	5	0x076D3892	18	16
20	BD	6	0x076D3892	18	47
21	BD	7	0x076D3892	18	36
22	BD	8	0x076D3892	18	40
23	BD	9	0x076D3892	18	43
24	BD	10	0x076D3892	18	20
25	BD	11	0x076D3892	18	37
26	BD	12	0x076D3892	18	41

# TQDC Module Complications



#### Recall data structure:

- ADC Window = 296ns (so TDC value differences < 296 means they</li> come from same ADC)
- TDC time ~ (ADC Trigger Time) clocks aren't exactly sync'd & different resolution



Segarra I 12/10/2018



### TQDC Module Data Structure



- · FIXED: reading correct raw data structure
  - There were issues reading timestamp, and skipping over entries due to increasing indexing inappropriately

