MPD Data Acquisition System Status

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Joint Institute for Nuclear Research

The third Collaboration meeting of the MPD and
BM@N experiments at the NICA Facility

Outline

- DAQ Architecture
- TOF, FFD electronics
- ECAL, FHCAL electronics and cooling
- Common readout unit
- DAQ Control Software
- DAQ IT Infrastructure

For more details please proceed to >>> MPD DAQ TDR

MPD Data Acquisition System

Properties

Reliable data transfer. Pipeline operation with synch and async stages.
Extensive diagnostics in hardware and software. Monitoring, logging.
Data integrity check on all levels. CRC, sequence numbers, FEC.
Fault tolerant, Highly available. Fast self recovery after SEU events.
Distributed, scalable, extendable. Based on open and industry standards.
Flexible architecture. Partitioning for independent subsystem operation.

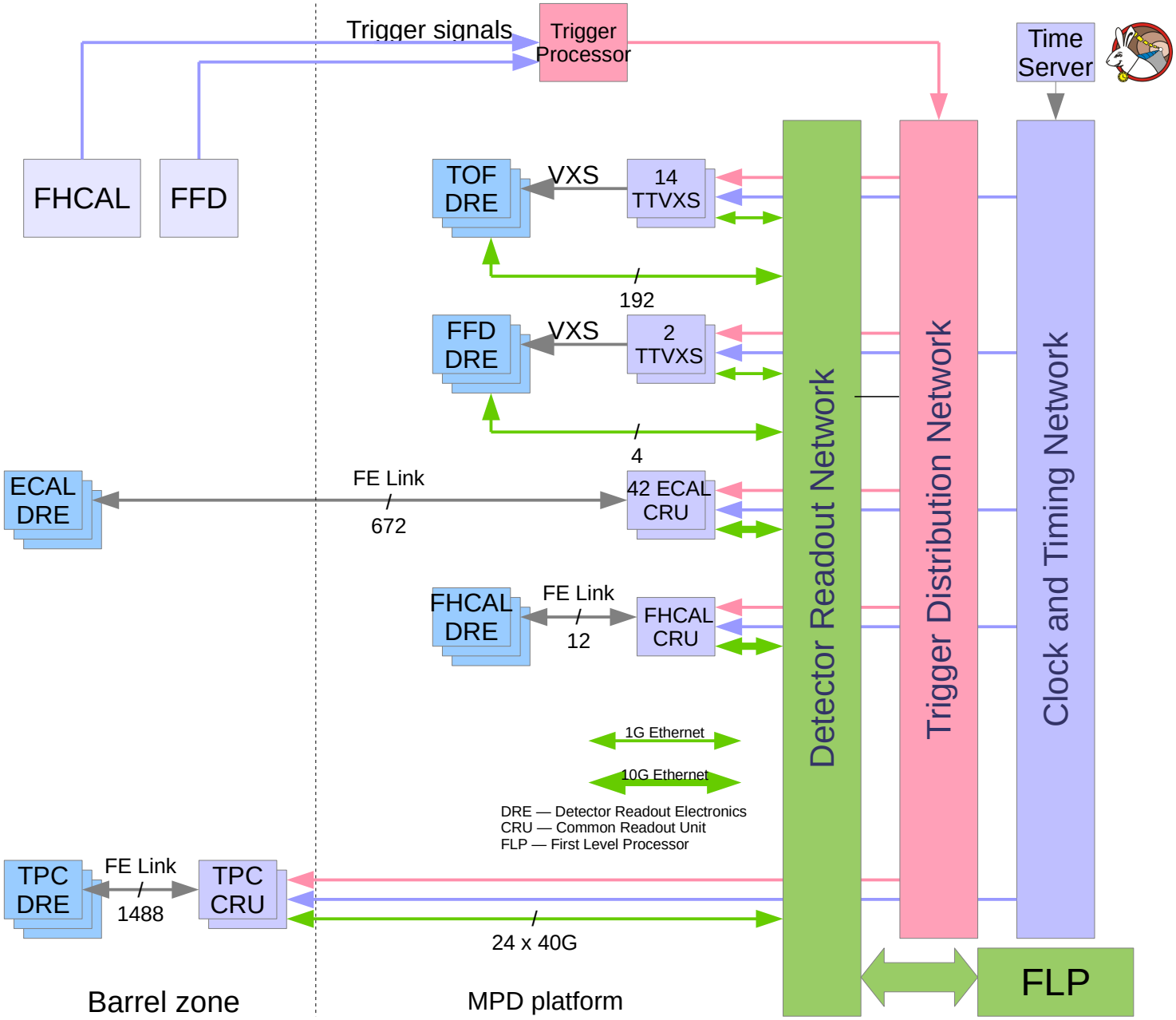
Operation Modes

Multiple hardware trigger classes
Uncompressed, full raw data during MPD commissioning
Large calibration data events at low trigger rate
High multiplicity events from central collisions at planned trigger rate

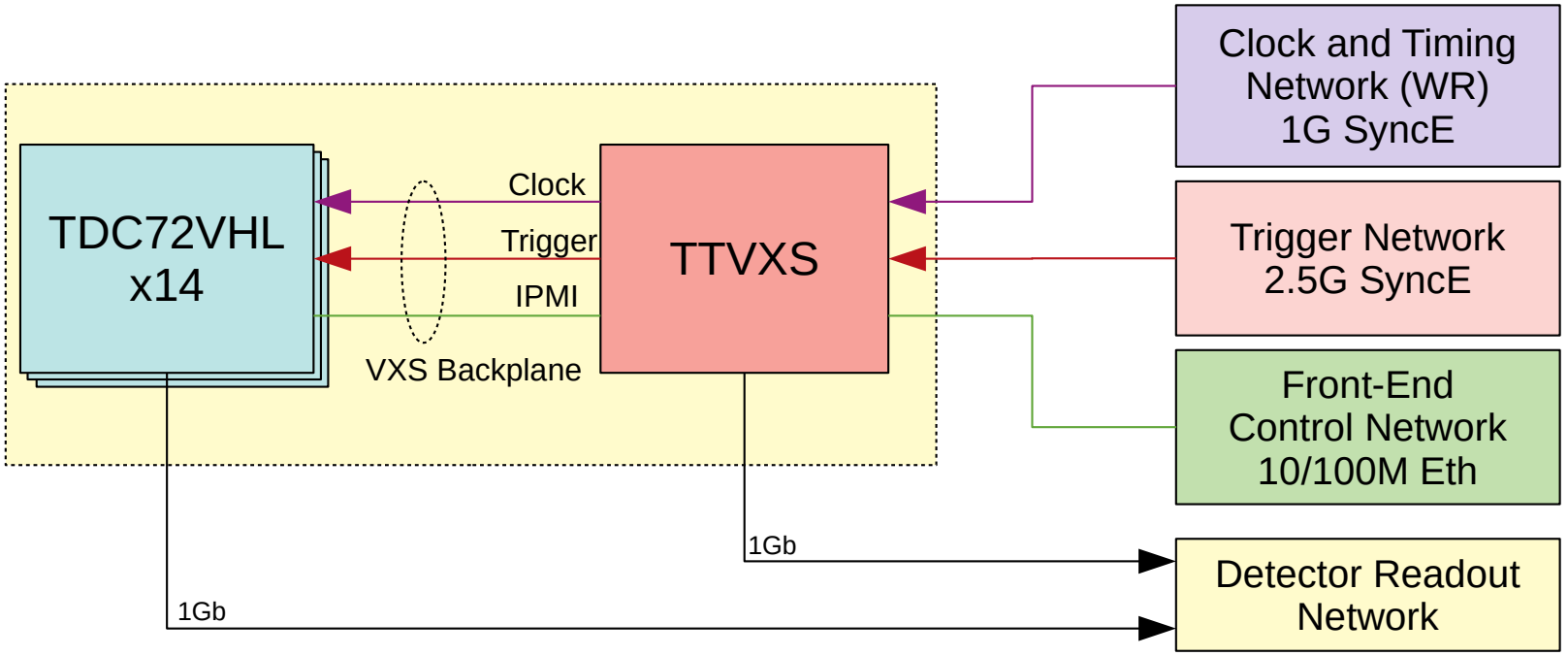
DAQ in numbers

Up to 7 kHz trigger rate, over 1 MB compressed event size to storage device
From 5 to 30 GB/s uncompressed raw data rate from readout cards to FLP
Approx. 200 TB in 2020 to 20 PB in 2023 annual stored data size

MPD DAQ Architecture

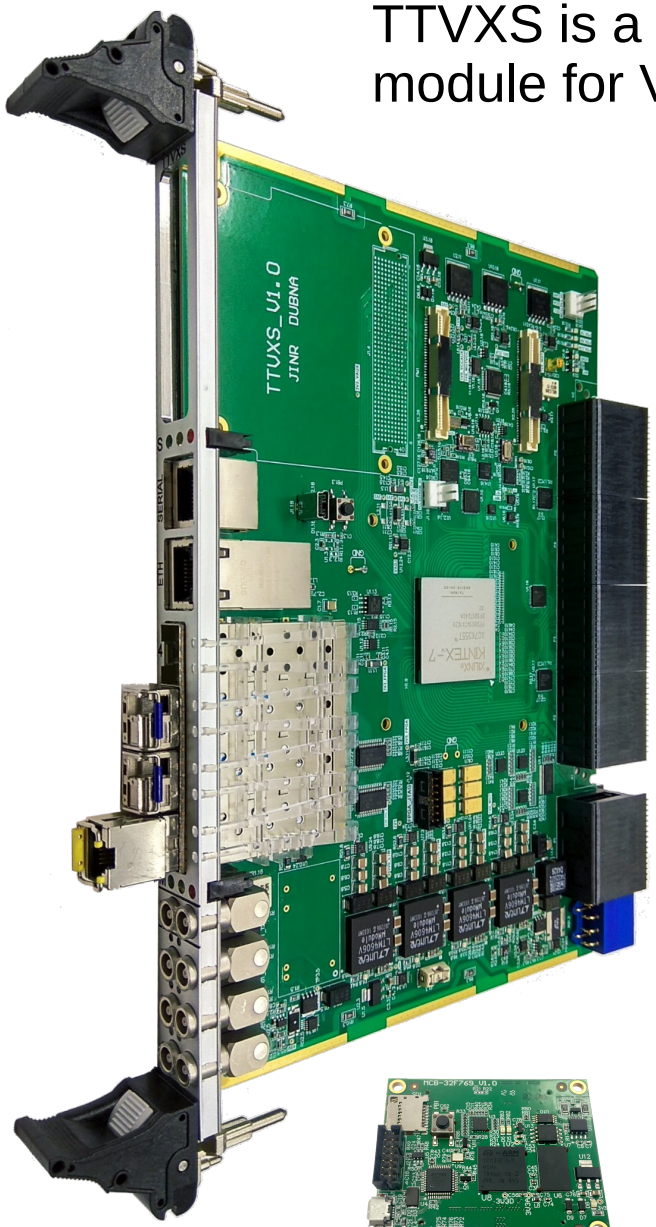


TOF - VXS Readout System



TOF DAQ is comprised of 14 VXS (VMEBus Switched Serial, ANSI/VITA-41) crates each equipped with one TTVXS and 14 TDC72VHL modules. TTVXS receives trigger information from Local Trigger Unit. Reference frequency and timestamp is provided by *Clock and Timing Network.* Module is controlled via *Front-End Control Network*. TTVXS distributes trigger and synchronous clock to TDC72VHL boards by VXS backplane. TTVXS monitors status of boards (voltages, temperature and etc).

TTVXS — VXS Switch Board



TTVXS is a Time, Trigger and Management module for VXS crate

- Clock, timestamp and trigger distribution to VXS payload boards over VXS serial backplane
- 4 SFP+ sockets for Detector Readout, Trigger Distribution and Clock & Timing connections
- Reference frequency and timestamp provided by White Rabbit Network or FE-Link (with CRU-16)
- Additional clock and trigger interface by FMC (VITA-57) card slot – integration with other systems

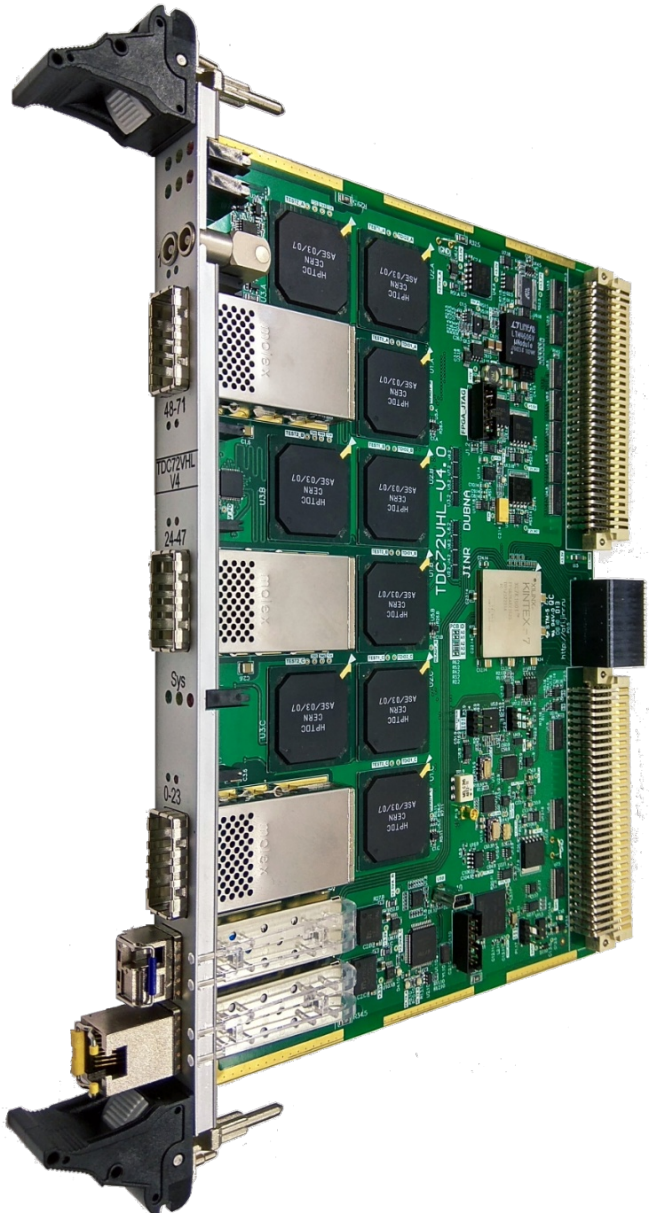
Status: 2 boards ready. Basic functions implemented. Testing.

IPMI mezzanine board

- IPMI (Intelligent Platform Management) function for automatic topology discovery, module status monitoring and control, firmware update

Status: basic functions implemented, improvements ongoing

TDC72VHL — Multihit 25 ps Timestamping TDC



TDC72VHL board performs time-stamping of discrete signals (hits). It is based on HPTDC chip. Hit timestamps are kept for 104 us in ring type memory.

Number of Channels	72
Input Signal	LVDS
Input Impedance	100 Ohm
Input Differential Voltage	25 mV min
Input Connector	CXP Interconnect System
Time Resolution with INL	~25 ps
Data Transfer Interface	SFP, 1000Base-X
Synchronization Interface	TTC over VXS

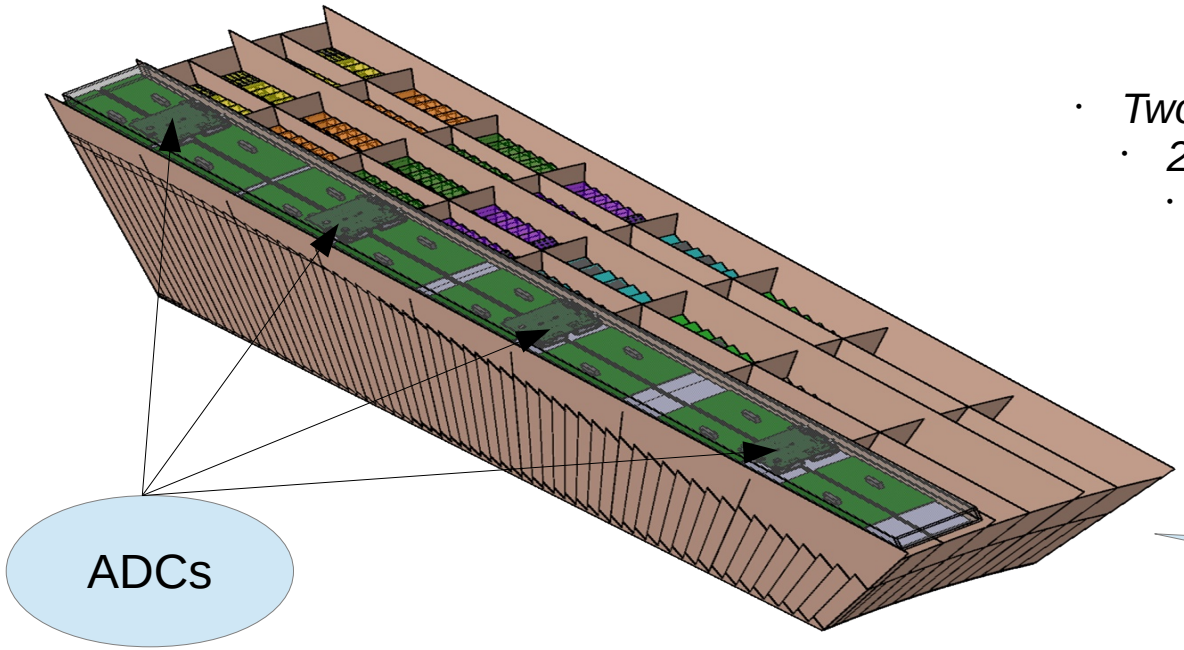
TOF & FFD DAQ Modules Production Status

Module	Produced and Tested	Plan Q4 2019	Plan Q3 2020	Total Qty.
TDC72VHL	72	140	80	220
TTVXS	2	10	7	17
CRU16	-	2	-	2

TDC72VHL:
- Produced ~30%
- In 2019 to produce ~30% more
- In 2020 to produce all remainig, plus spare modules

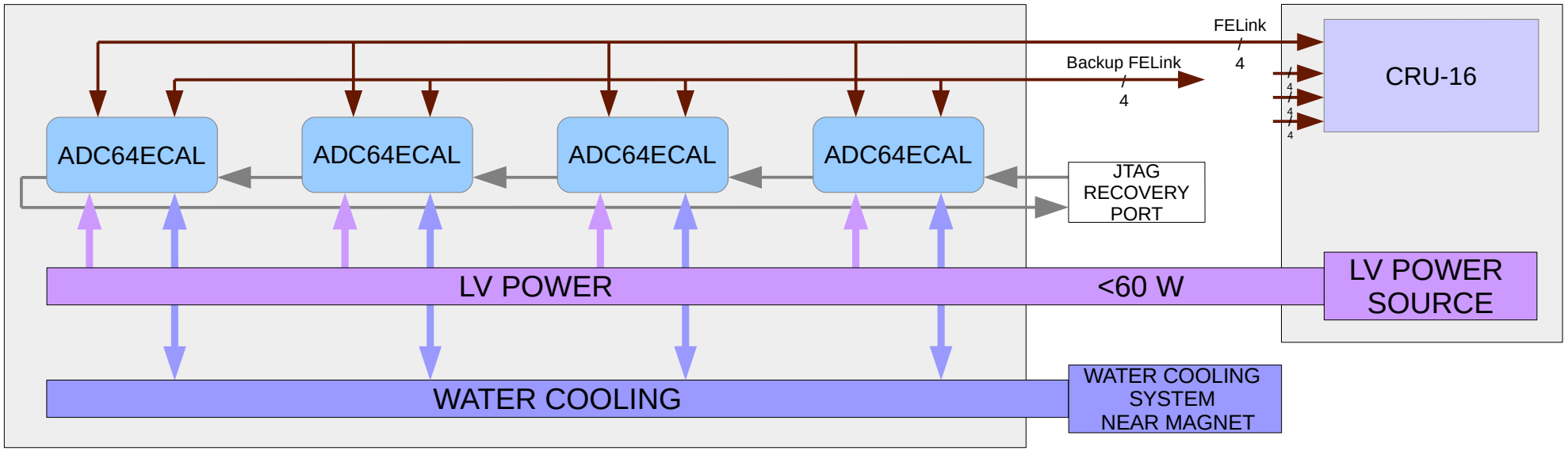
TTVXS:
- Produced ~15%
- In 2019 to produce ~50% more
- In 2020 to produce all remainig, plus spare modules

ECAL Structure

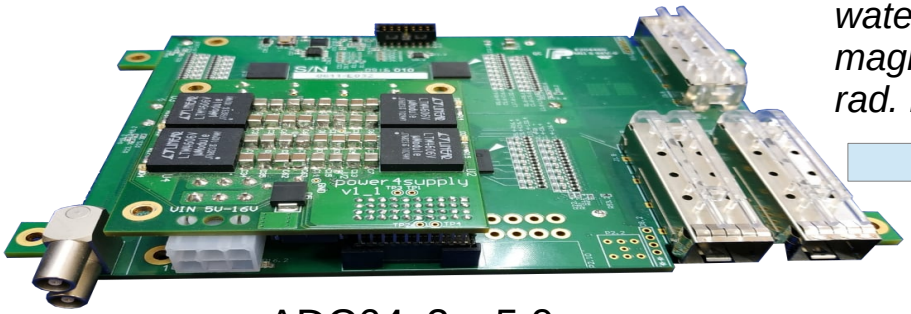


- *Two sides, 14 Sectors each*
  - *2 Half-Sectors in a Sector*
    - *3 Boxes per Half-Sector*
      - *4 ADCs per Box*

ECAL box connections

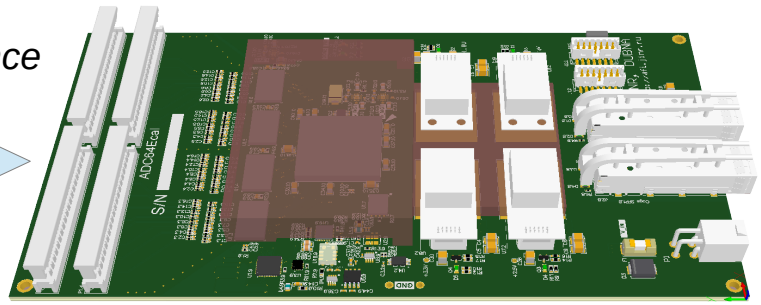


Waveform digitizer for ECAL – ADC64ECAL



ADC64s2_v5.0
2017

mechanics, connectors
water cooling
magn. field tolerance
rad. hard DC/DC



ADC64ECAL
2019

Usage
ECal at BM@N - data taking 2018
FHCal at MPD - ready

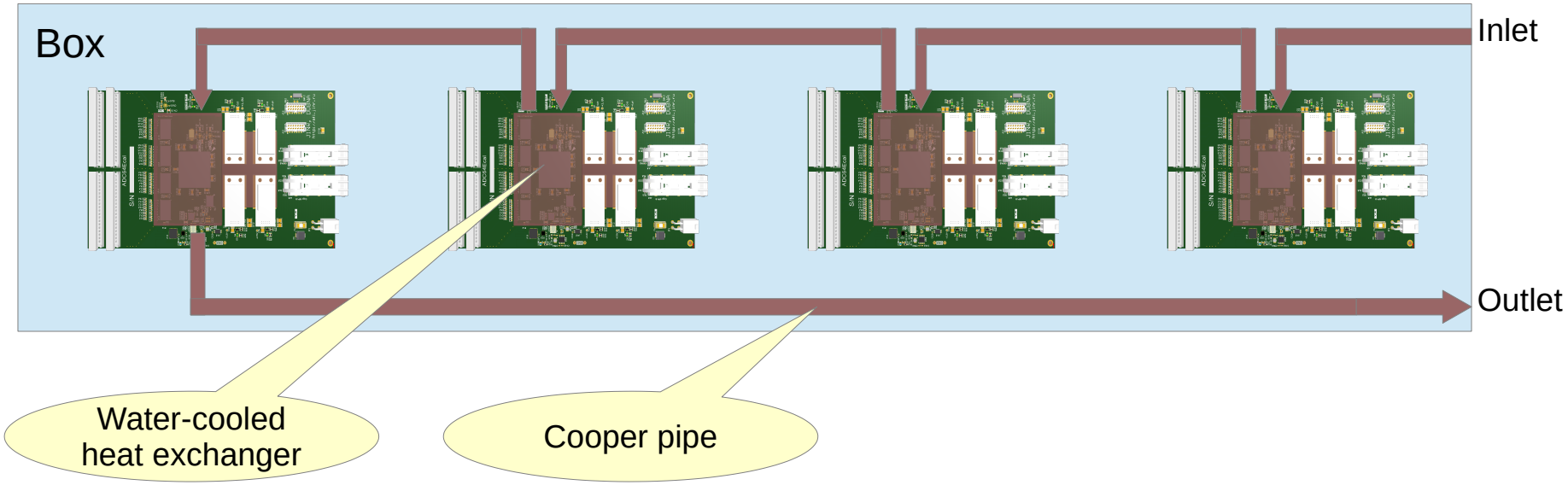
Current status
Firmware is ready
Software is ready
PCB in production

Total quantity for ECal
672 pcs

ADC64ECAL board characteristics

Number of Channels	*64*
Sample rate	*62.5 MS/s*
Resolution	*14 bit*
Power consumption	*< 15 W*
Magnetic field tolerance	*by design*
Radiation hard DC/DC covertors	*yes*

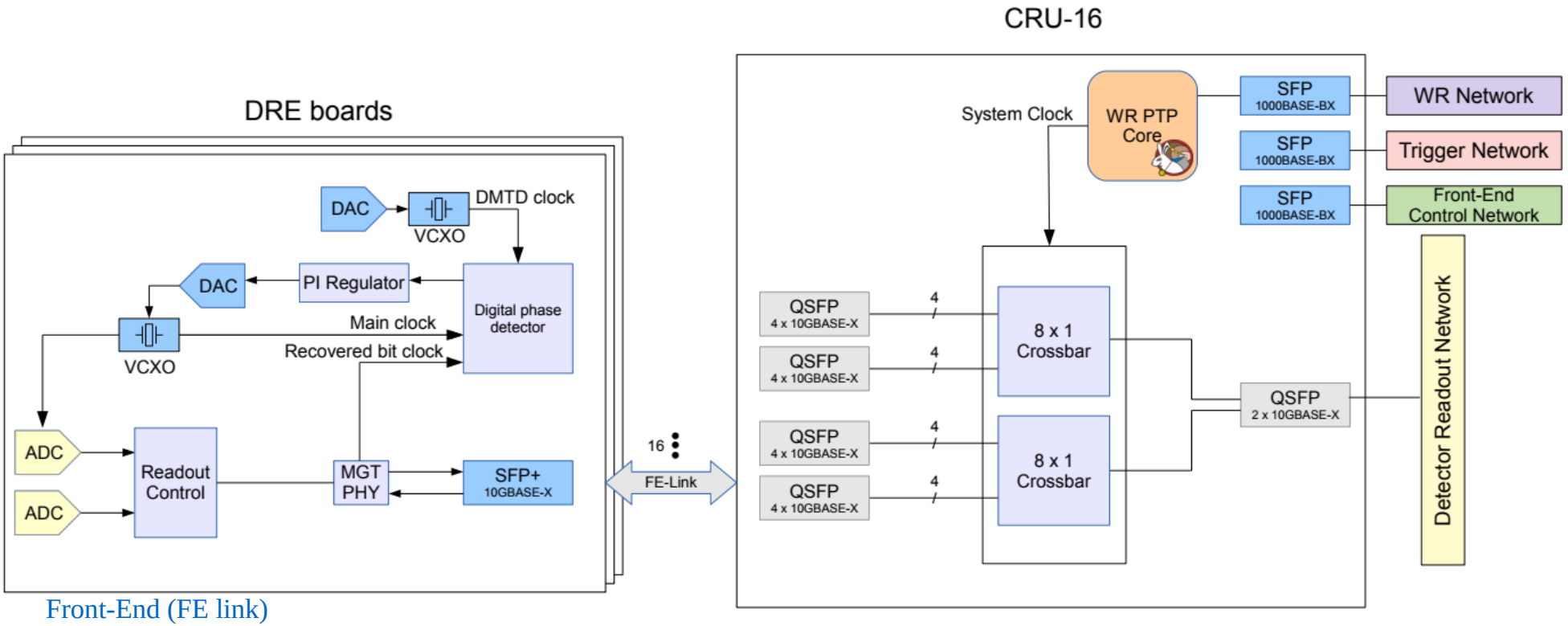
ECAL water cooling system concept



Status: Contract for R&D

- Leakless liquid cooling system (pressure < 0,1 MPa)
- Non magnetic matherials
- 5 years of service-less continuous operation

Common Readout (and everything else) Unit



Front-End (FE link)

"Variable-speed Synchronous Ethernet". Byte-oriented, 8b/10b Ethernet like encoding and framing

Maximum data rate: 2.5 Gb/s VXS backplane (TTVXS), 8 Gb/s (CRU-16) with commercial QSFP fiber-optical transceivers.

DRE clock synchronized to CRU with digital PLL. Short fixed cables – one time delay calibration.

Timestamps, trigger, data readout, control over same link

No TCP-IP stack complexity in DRE. Simple FGPA code with fail-safe FSM and data pipelines to mitigate SEU events.

Aggregation *"switch"* (CRU-16 core)

Not an Ethernet switch. Fixed traffic directions: left-right or right-left only. Connects to DAQ network with 10G Ethernet, UDP-IP.

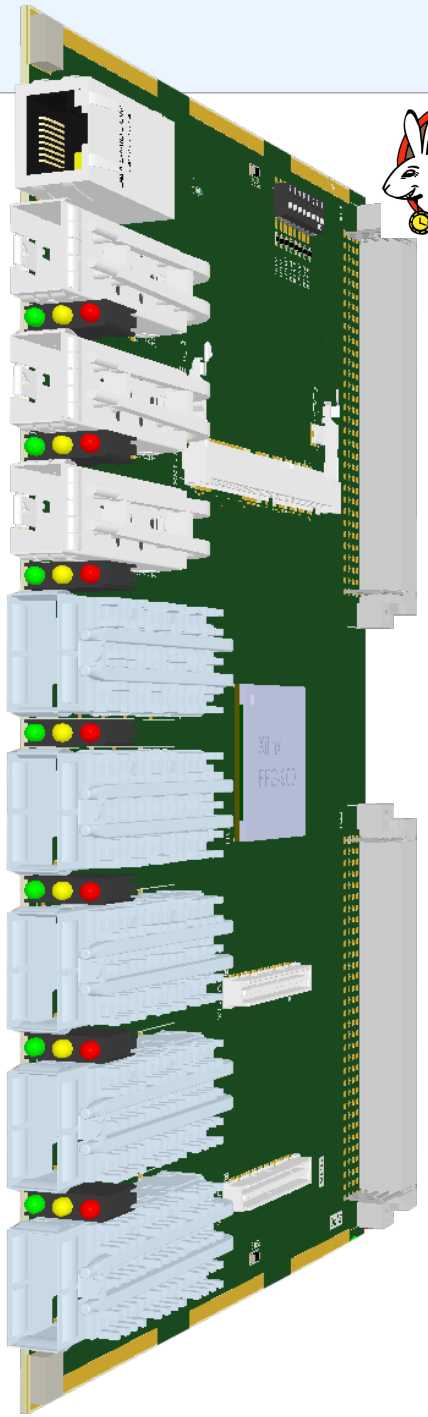
Large FPGA on board running White Rabbit and service CPUs

Extensive diagnostics: hardware histograms, RAM-based multichannel counters

Use speed translation FIFOs. Arbitrated crossbars. Option for large DRAM buffer on board

Future: hardware event merging for connected DRE boards

CRU-16



Common Readout Unit for 16 DRE boards

- FE-Link interface to DRE boards - multi-gigabit duplex serial synchronous interconnect with deterministic latency. Provides clock and trigger information for downstream boards and receives raw data stream
- 4 GB onboard DDR3 memory for data buffering, decouples realtime hardware data flow from software data receivers
- 4 QSFP downlink sockets for 16 Detector Readout boards connections grouped by 4
- 3 SFP sockets for Trigger Distribution, Clock & Timing
- 10/100 Ethernet for Slow Control
- Timing synchronization by White Rabbit Network

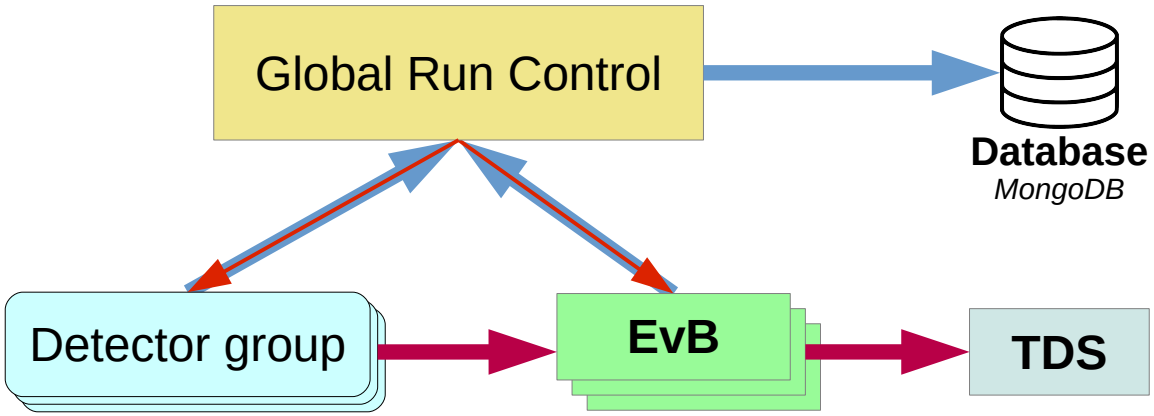
Status

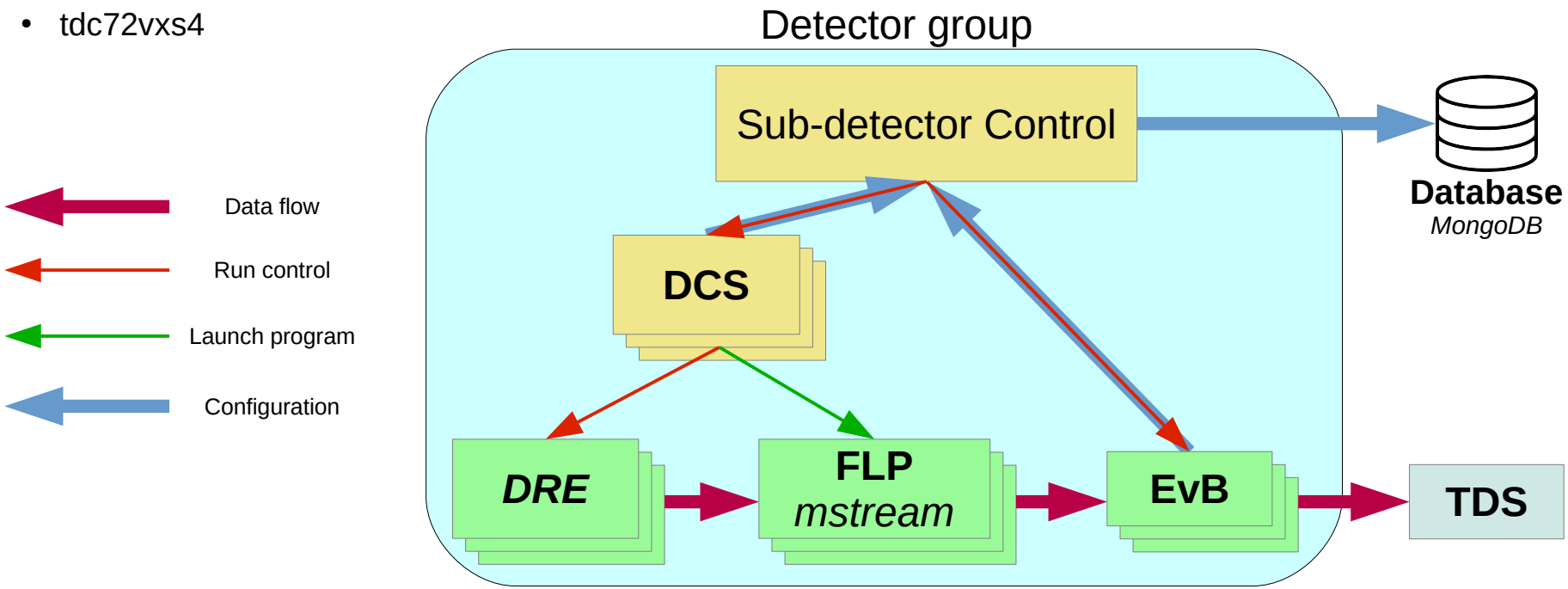
- FE-Link designed and tested on prototype
- PCB to be ready in 2019
- Firmware and software under development

DAQ Control Software overview

Device Control System:
- ADC64-System
- TTVXS run control
- TDC2
- CRU-16 control

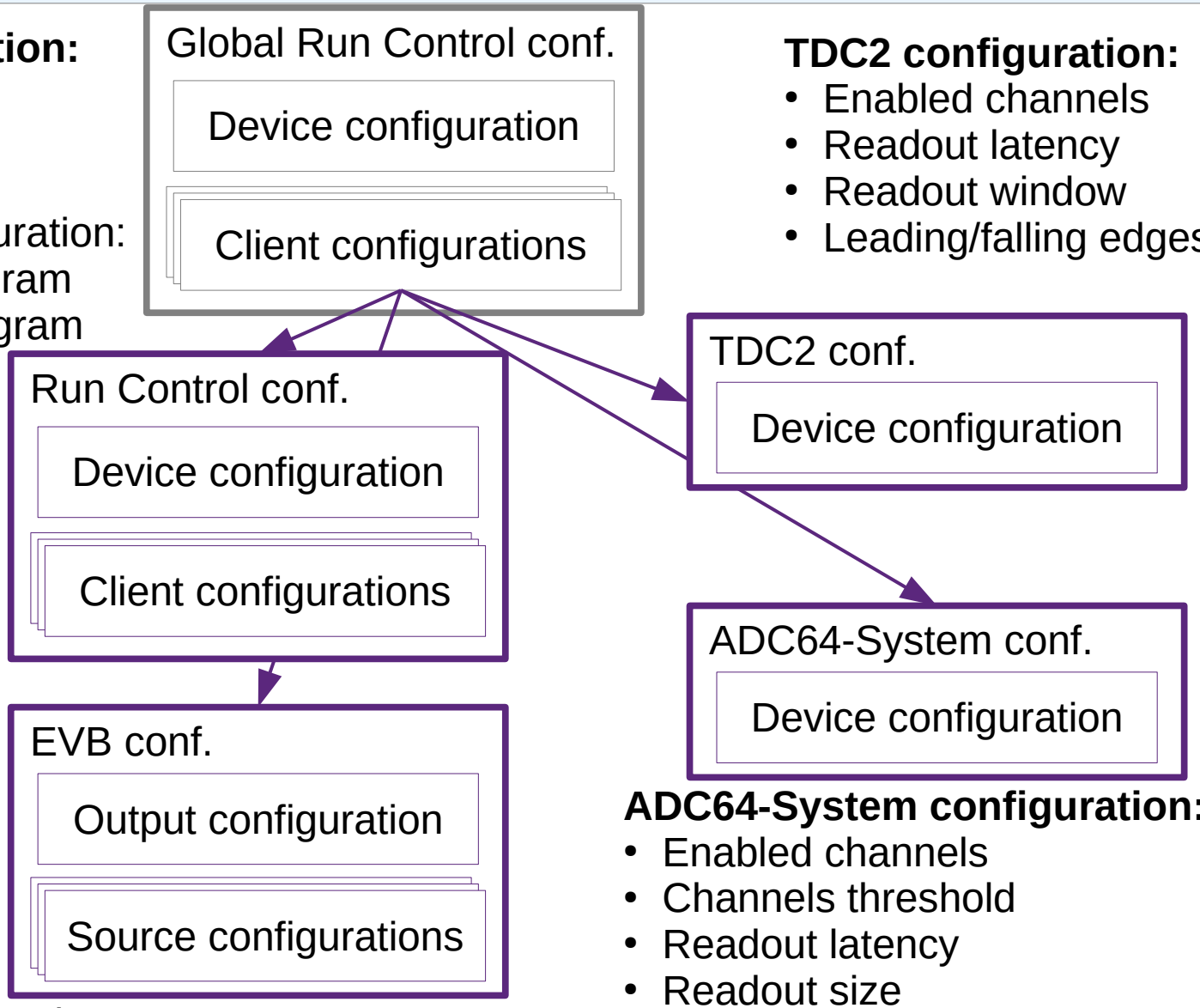
Device Readout Electronics:
- adc64s2 ver.5
- CRU-16 (adc64 for ECal)
- ttvxs
- tdc72vxs4





Run configuration

Run control configuration:
- Trigger source
- Conf. busy inputs from sub-system
- Client program configuration:
  - Type of source program
  - Index of source program

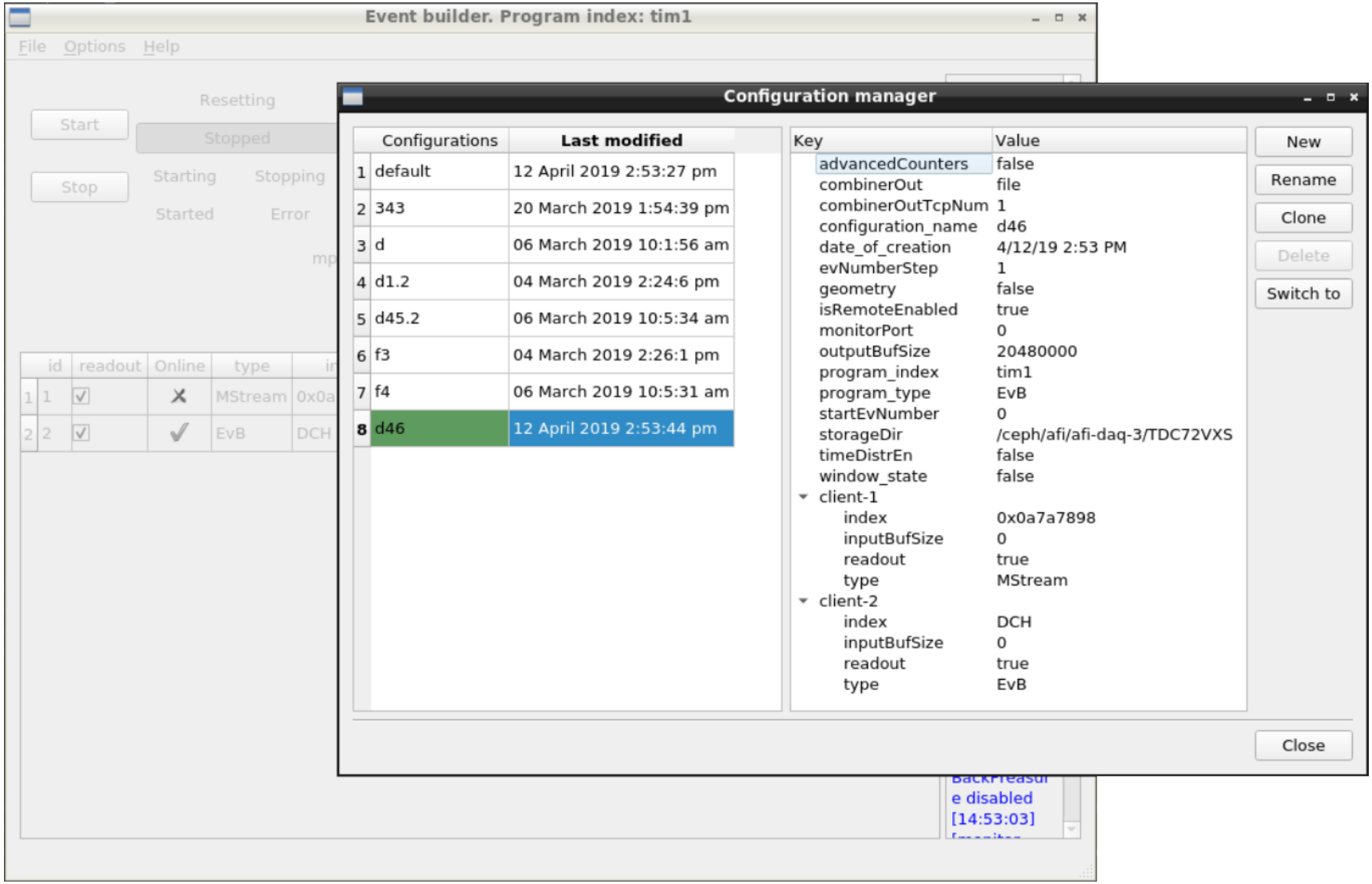


TDC2 configuration:
- Enabled channels
- Readout latency
- Readout window
- Leading/falling edges

ADC64-System configuration:
- Enabled channels
- Channels threshold
- Readout latency
- Readout size
- Digital signal processing conf.
- Zero-suppression conf.

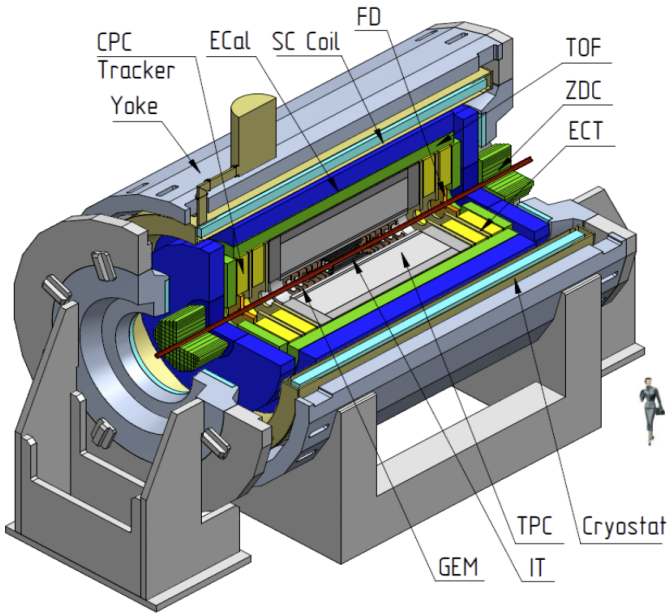
EVB configuration:
- Output destination
- Client program configuration:
  - Type of source program
  - Index of source program

Program configuration



- Stores all parameters which relate only to this program.
- Allow to fast switch from calibration to data taking work.

MPD DAQ Cable Connections (Stage-1)



72 optic fibers (WR, trigger)

TPC

24 ethernet copper cable for SC

2592 optic fibers (data, trigger, synchronization)

Ecal

FHCAL

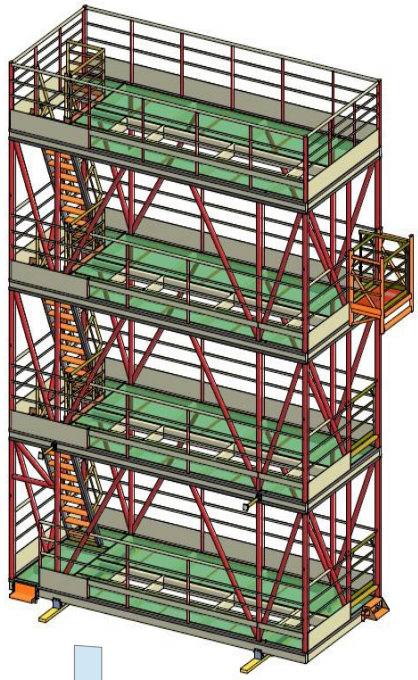
48 optic fibers (data, trigger, synchronization)

14 crates TOF&FFD

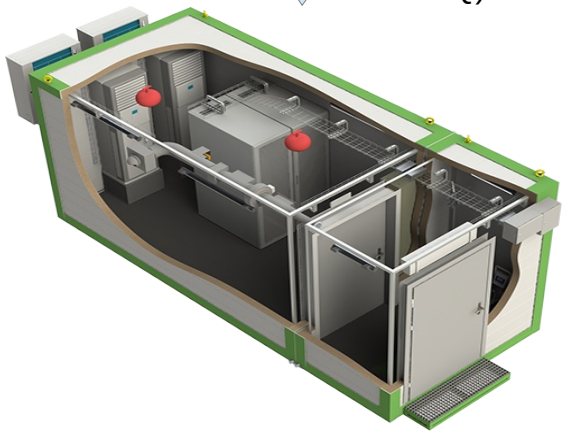
42 signal cables per crate

42 cat5e links (slow control)

98 optic fibers (data, trigger, WR SW intercommunication)



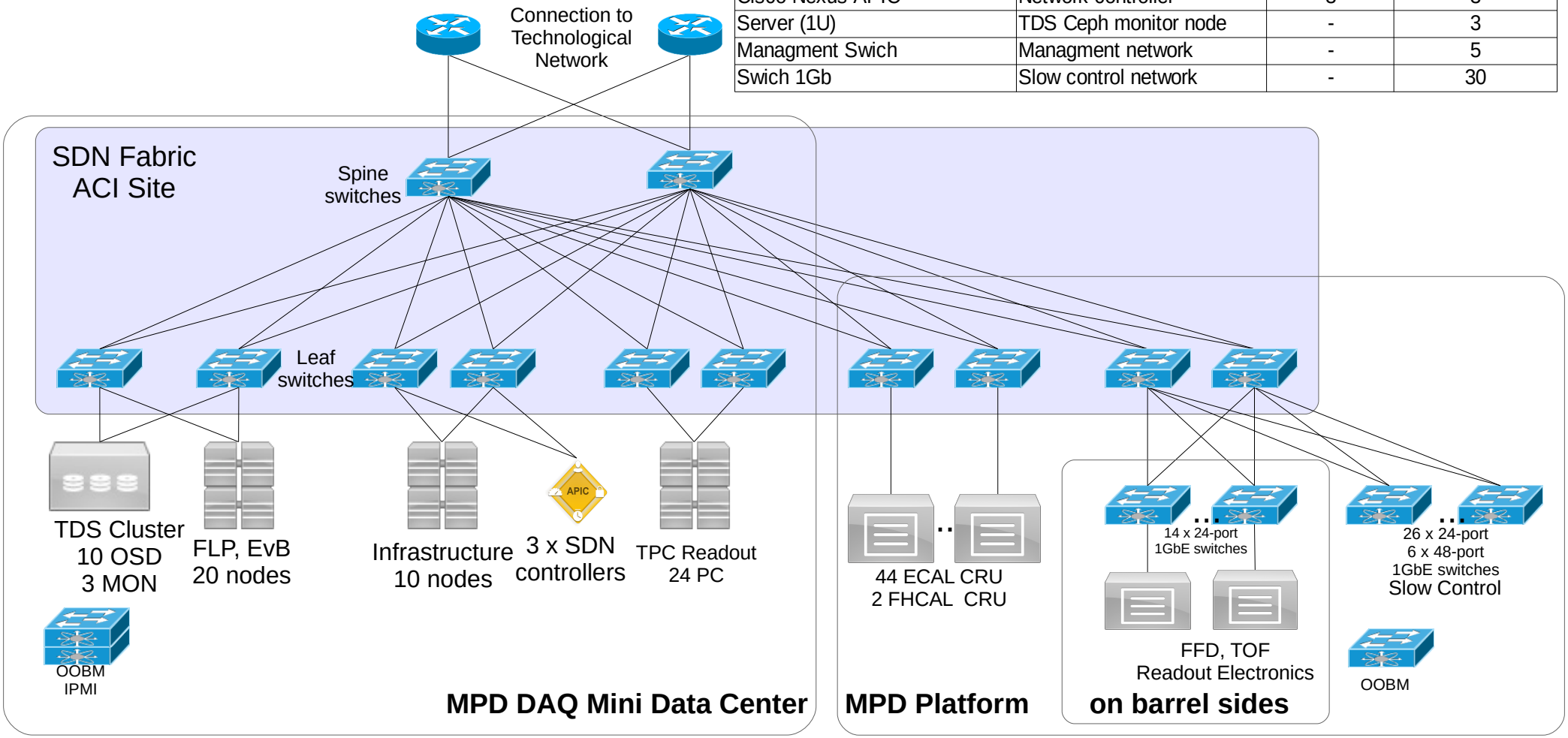
192 optical fibers (all subdetectors to DAQ)



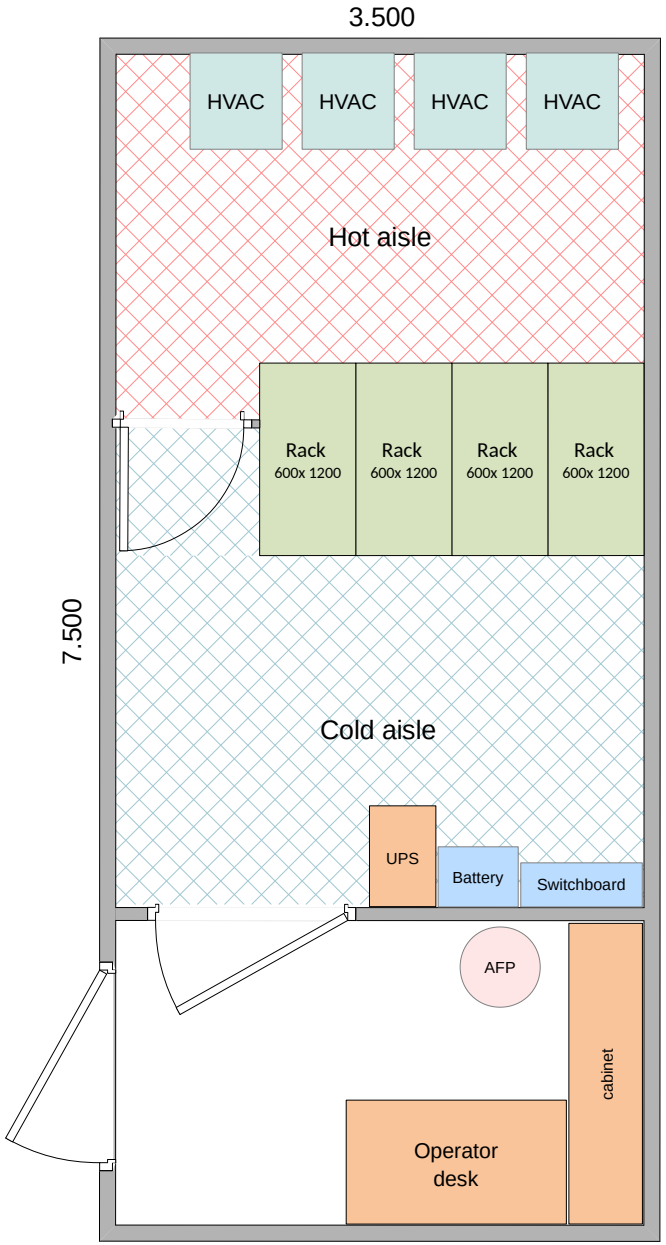
Signal cables	588
Fiberoptical cables	2810
UTP Ethernet cables	66

MPD DAQ Network

Device type	Role	Current status	Planned 3Q 2020
MDC Container	Mini Data Center	-	1
Server (2U) Twin	FLP, EVB, Proxmox	-	10
Server (1U)	TDS Ceph storage node	-	10
Cisco Nexus Leaf 100G	Leaf swich	2	6
Cisco Nexus Leaf 10G	Leaf swich	4	4
Cisco Nexus Spine	Spine switch	2	2
Cisco Nexus APIC	Network controller	3	3
Server (1U)	TDS Ceph monitor node	-	3
Managment Swich	Managment network	-	5
Swich 1Gb	Slow control network	-	30



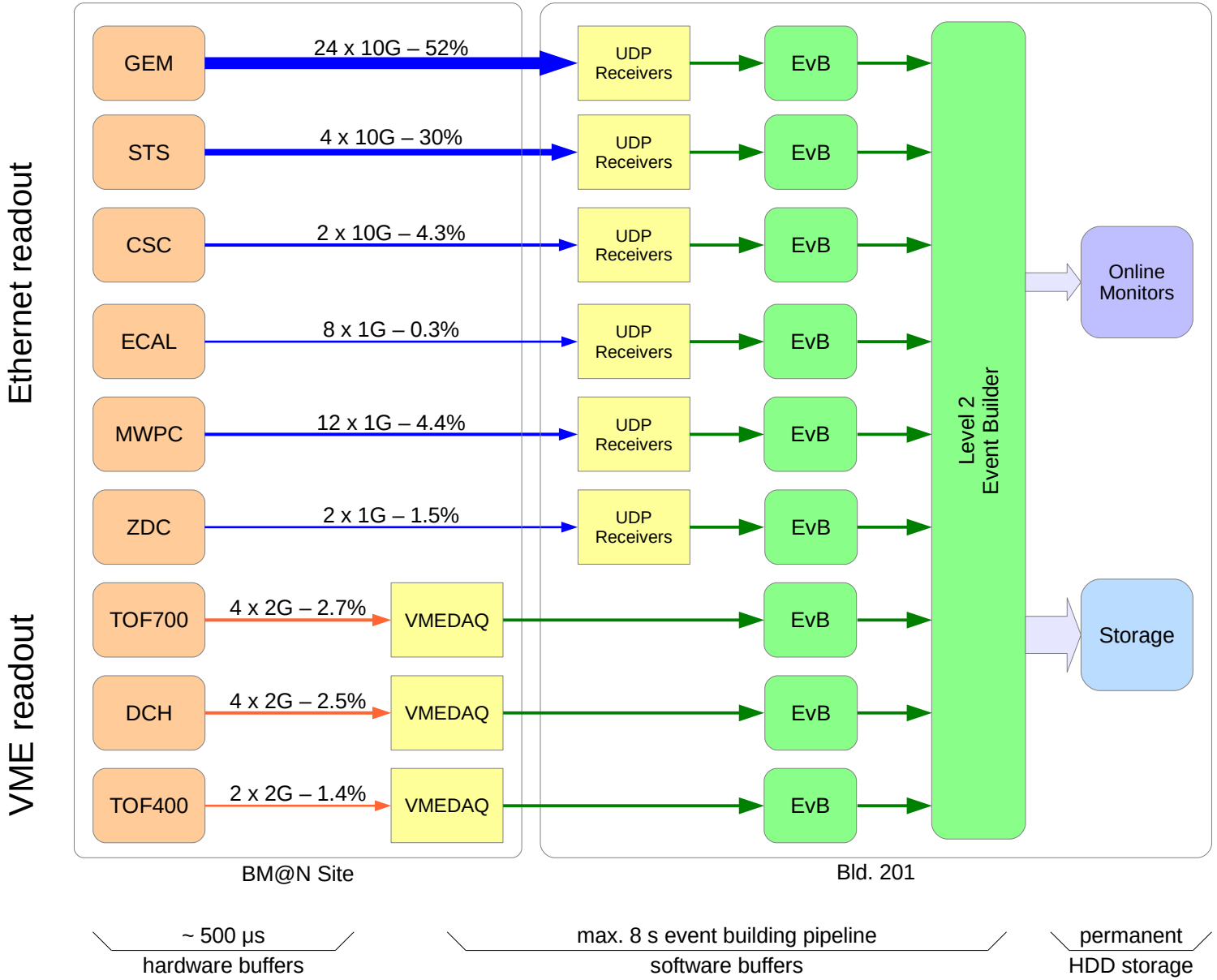
MPD DAQ – Mini Data Center



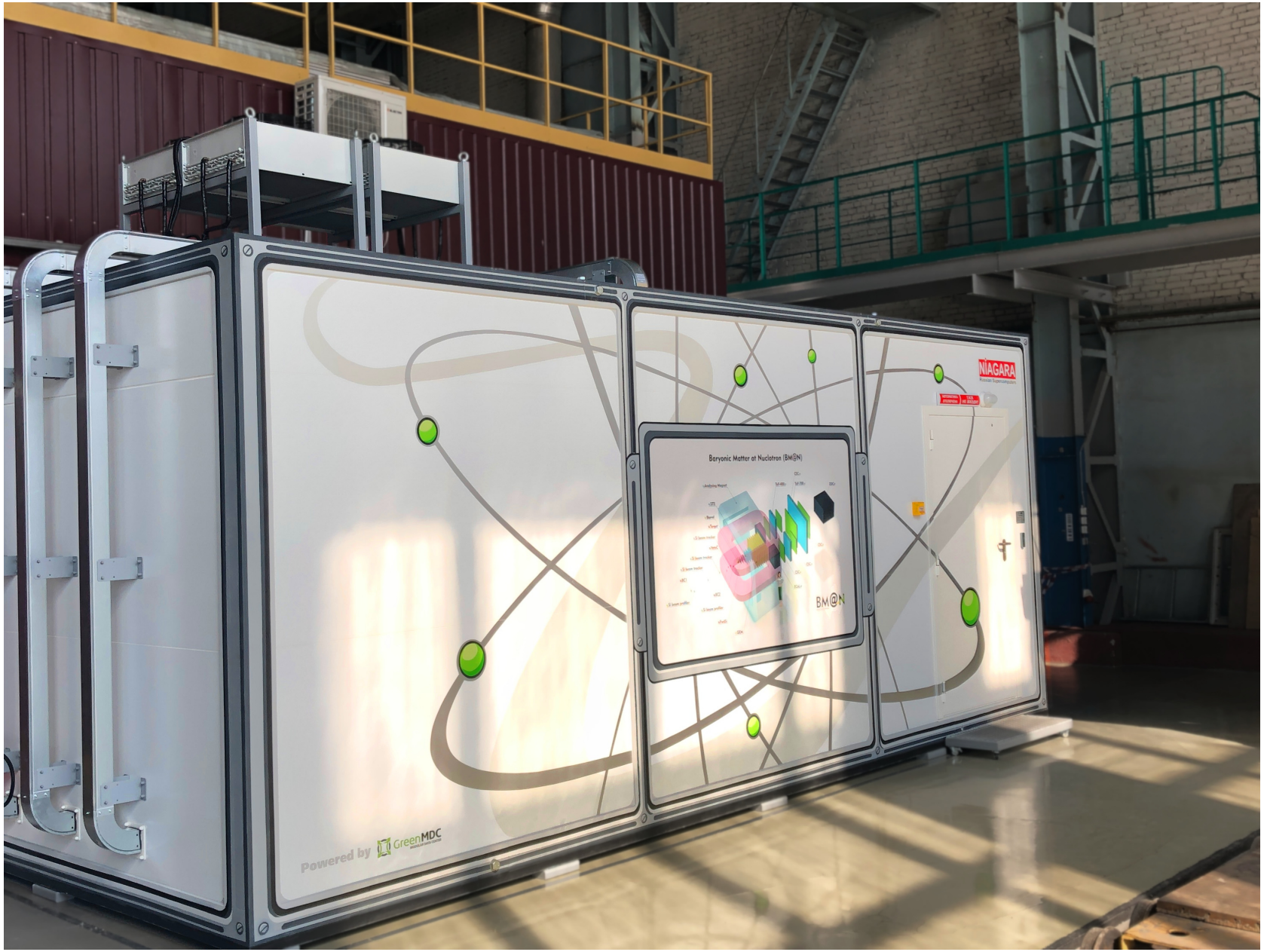
Specifications	
Input power	50 kW
IT power	24 kW (N+1) / 30 kW max
Rack count	4 racks
Redundancy	N+1 (UPS, HVAC)
Battery backup	8 minutes
Rack size	600 x 1200 x 42U

Stage-1 Equipment	Rack Units
Passive network	16
Active network (switches, controllers)	18
Infrastructure nodes	4
FLP, Event Builder nodes	44
Transient Flash Storage	13
Message Logging and Search	5
Reserve (Stage-2)	68

BM@N DAQ setup in March 2018



BM@N Mini Data Center, bld. 205



Thank you!

Extra slides

MPD Data Flow