## Torino group



(present situation)

#### Staff (5 + 1 senior)

Angelo Maggiora (staff senior) Antonio Amoroso (staff) Daniele Panzieri (staff) Flavio Tosello (staff) Michela Chiosso (staff) Oleg Denisov (staff)

### PostDoc (3)

Bakur Parsamyan (postdoc) Maxim Alekseev (postdoc) Jorge Berenguer (postdoc)

### PhD (3 in cotutela)

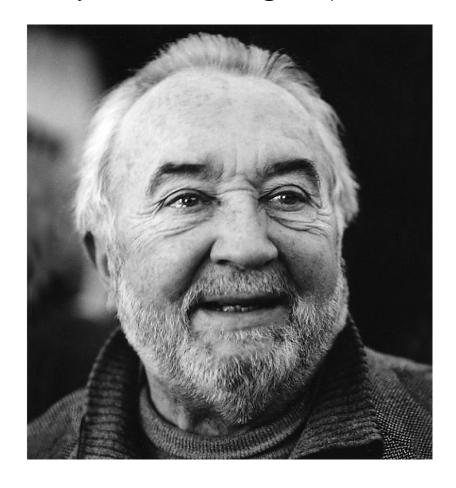
Michael Pesek Ph.D (PhD) Alexander Chumakov (PhD) Bogdan Vasilishin (PhD)

### + Many Master Students

# **COMPASS** Torino group



In memory of **Guido Piragino** (1933 – 2019)



Thanks Maestro

# **COMPASS Torino group**



### A short story

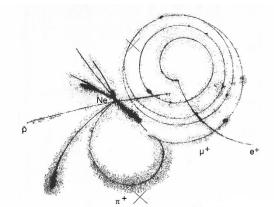
Our Group was involved in many experiments in the years, since 60's, and very often with a *strong collaboration* with JINR, thanks to Guido Piragino:

## Experiments:

- Dub-To (@ JINR)
- ToFras (@ LEALE, Frascati)
- ToFraDupp (@ LEAR, CERN)
- Disto (@ Saturne, Saclay)
- Obelix (@ LEAR, CERN)
- PAINUC (@ JINR)
- COMPASS (@ SPS, CERN)









## **Torino group in COMPASS**





The RichWall (in collaboration with JINR)



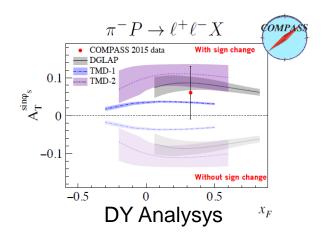
MWPC's (in collaboration with JINR)

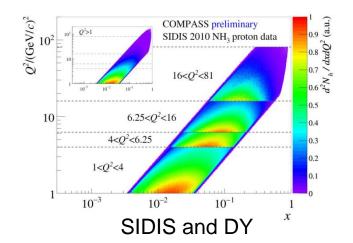


Hadron absorber



Front End Electronics (CMAD)

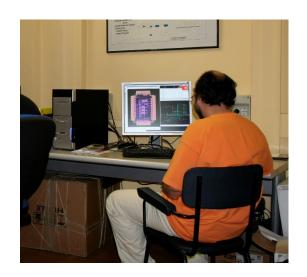




## **INFN Torino**



- Technological Laboratory (mechanics)
- Electronics Laboratory
- Microelectronics Laboratory
- Computer Centre (cloud computing)





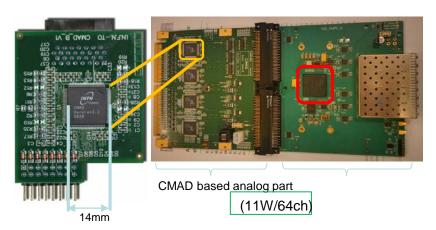


## **Torino group for SPD?**

We can mostly be involved in developments of FEE, where our group and INFN Torino have a good expertises.

Obviously this needs a full approvement (and some funding) from INFN

#### **CMAD**



64ch iFTDC FPGA based digital part

Programmable gain : 0.4 mV/fC - 4.4 mV/fC

8 channels per chip

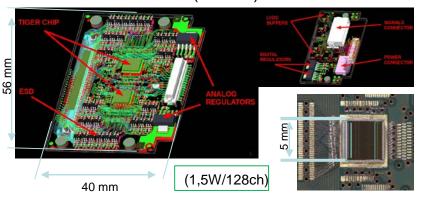
Gain programmable channel by channel

Threshold adjustable channel by channel (On board DACs+Logic)

Hit rate > 5 MHz

Power consumption < 30 mW/channel

Torino Integrated GEM Electronics for Readout (TIGER)



64 channels: VFE, TDC/ADC, local controller SEU protected digital backend On-chip bias and power management On-chip calibration circuitry Fully digital output, LVDS IO 4 TX SDR/DDR links, 8B/10B encoding SPI configuration link Power consumption < 12 mW/channel Nominal 160 MHz system clock Sustained rate per channel: above 100 kHz