COMPASS++/AMBER DAQ

Igor Konorov

Institute for Hadronic Structure and Fundamental Symmetries (E18)

TUM Department of Physics

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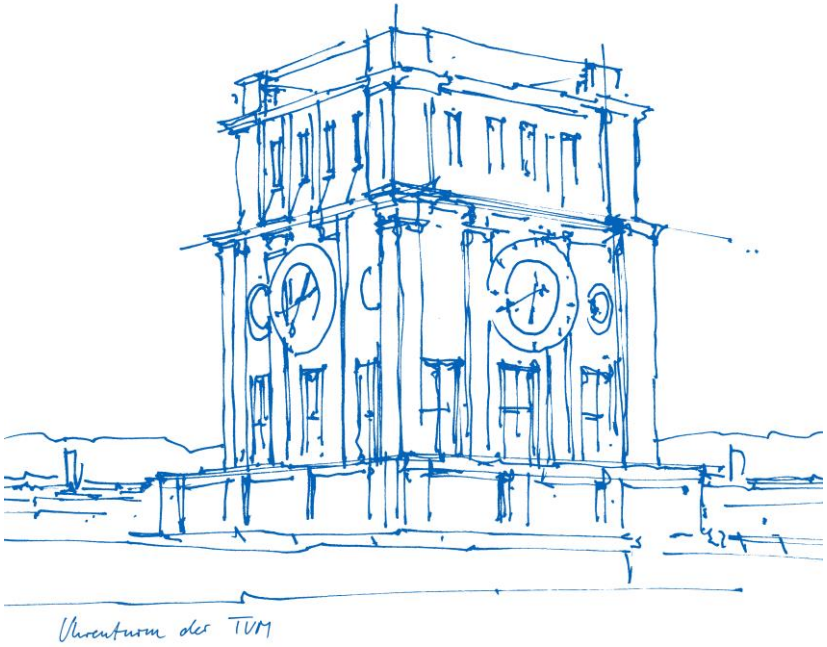
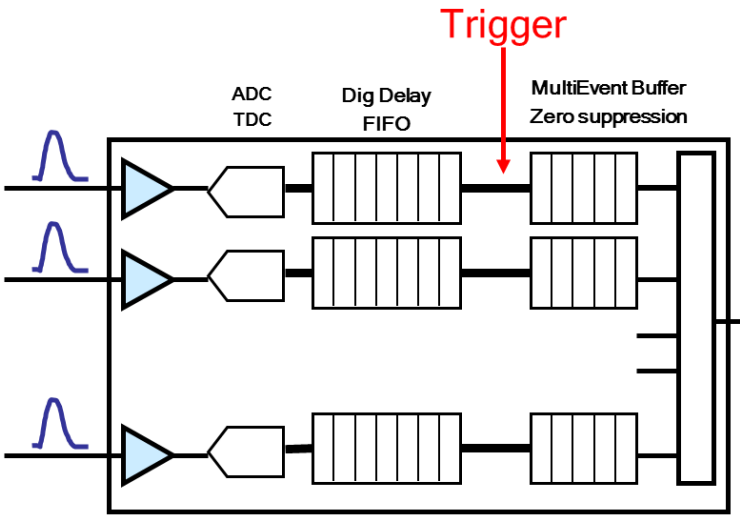
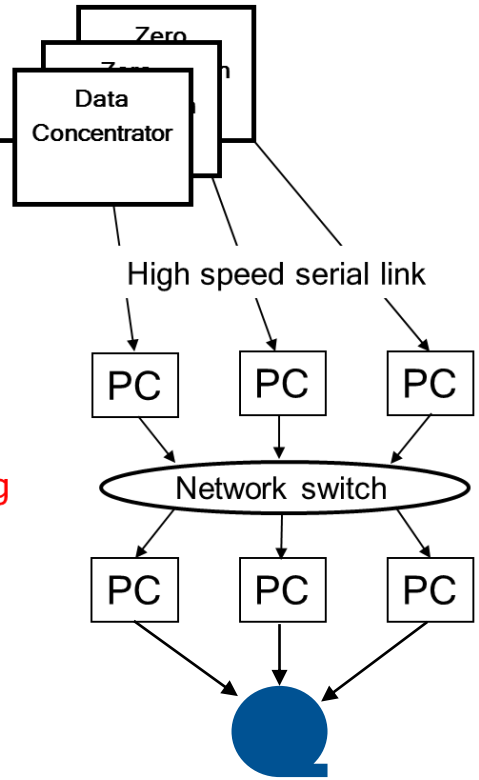
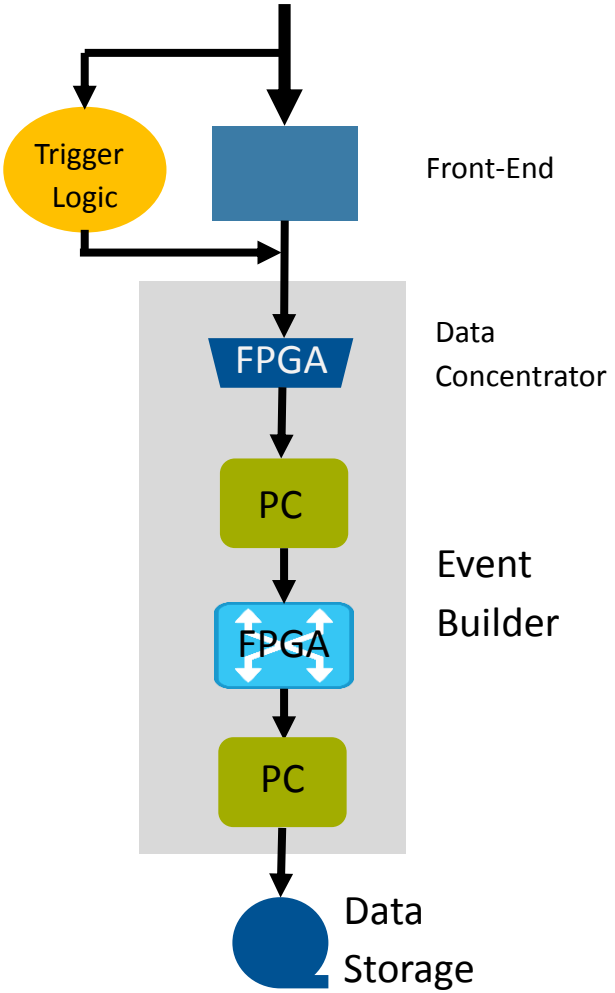


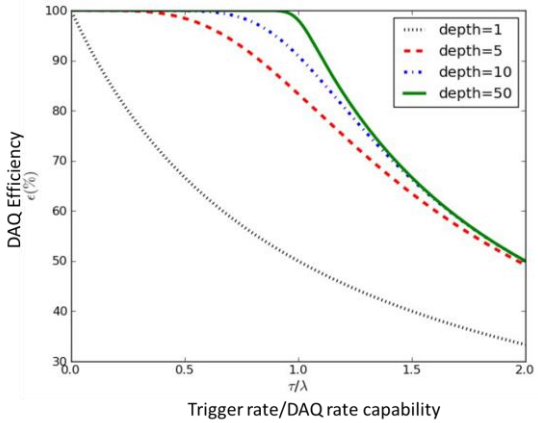
Dead Time less COMPASS DAQ





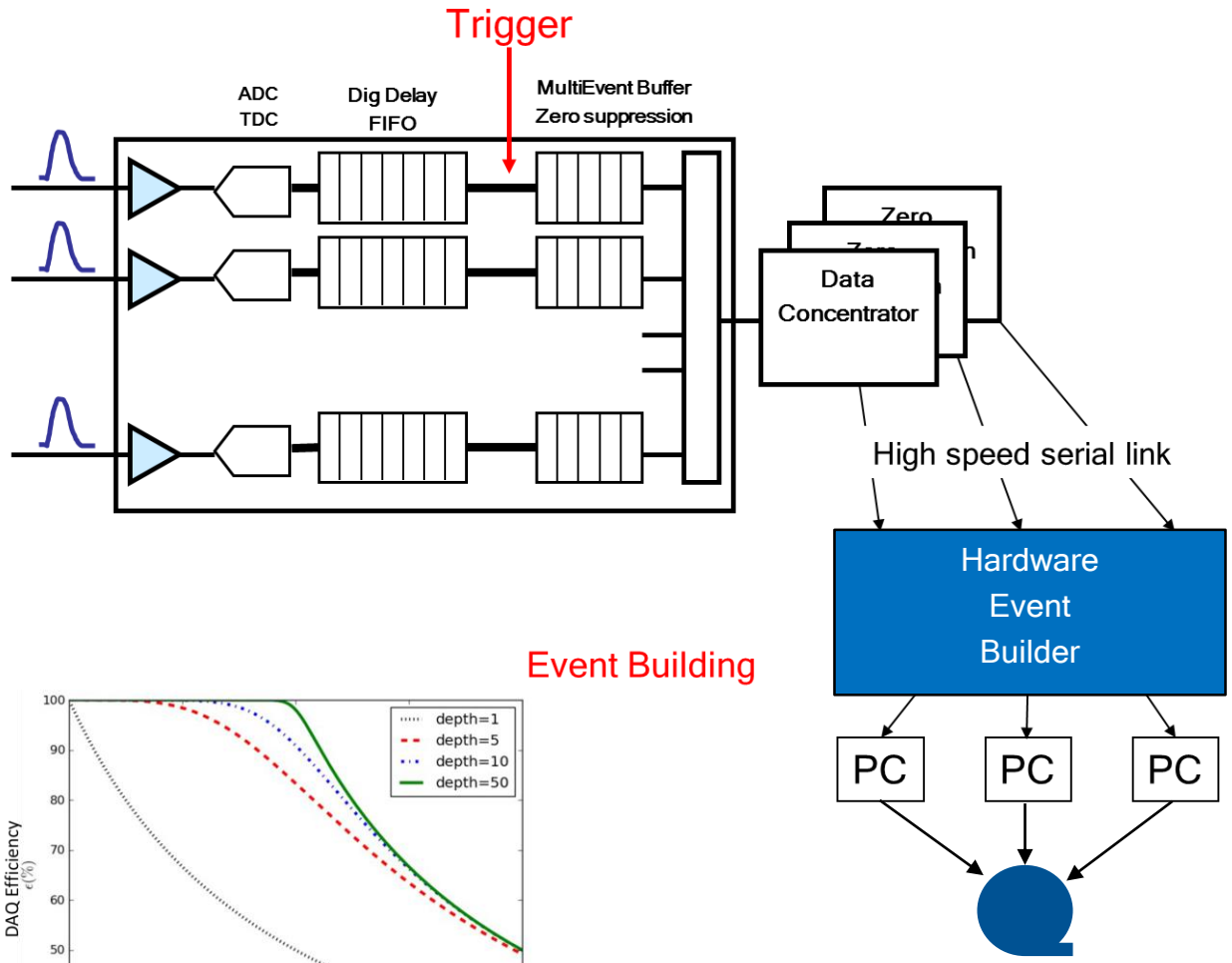


Event Building

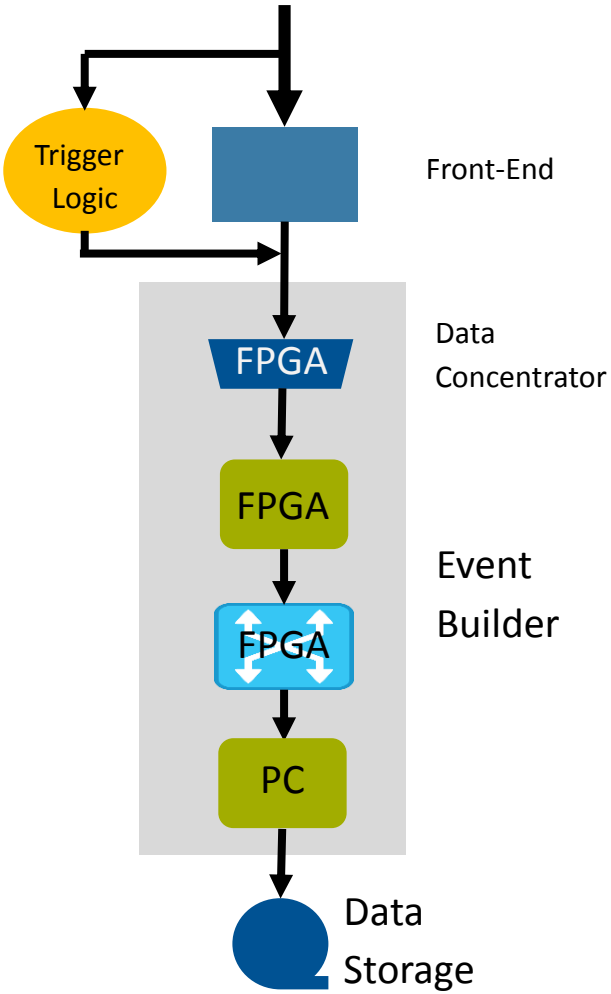


40kHz, 50kB/event

Intelligent FPGA DAQ, after upgrade 2014



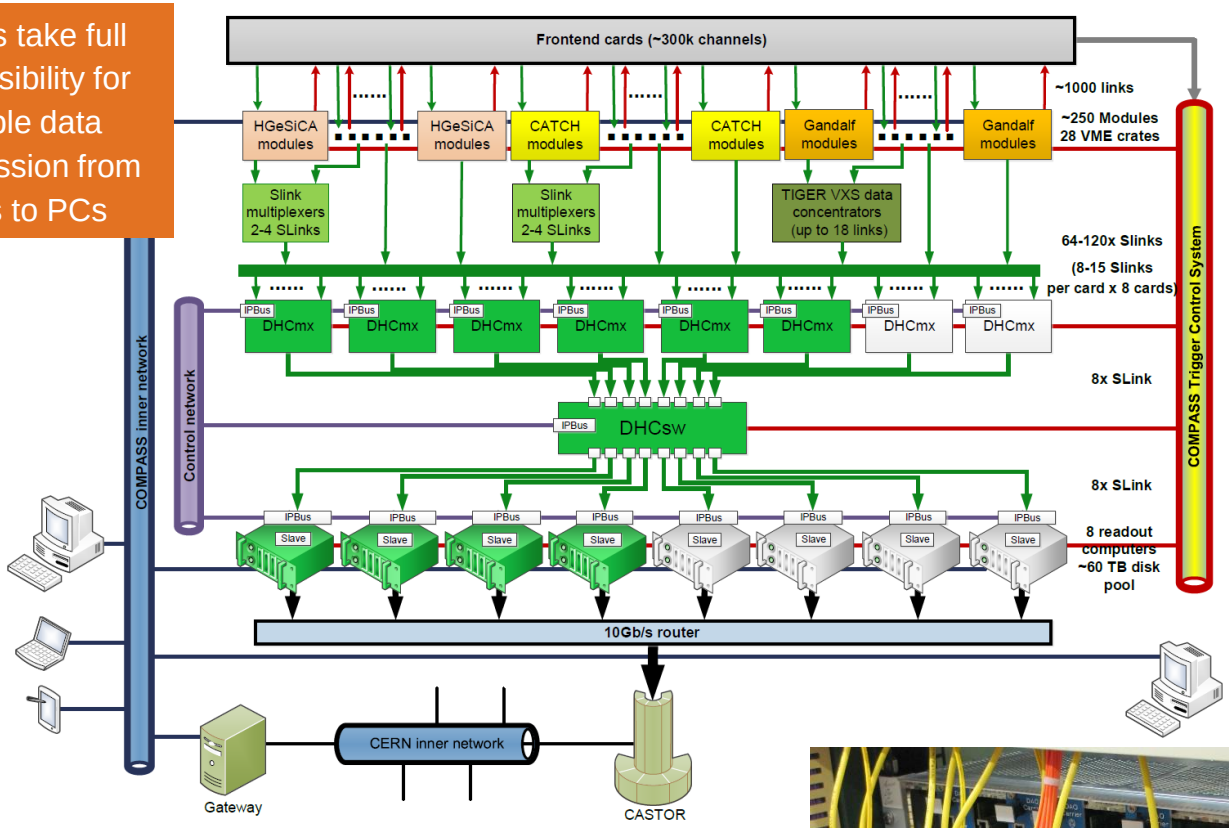
Event Building



40kHz, 50kB/event

iFDAQ Architecture

FPGAs take full responsibility for reliable data transmission from FEEs to PCs



DHmx, DHsw

- Virtex6 XC6V75
- 4GB, DDR3
- 16x6.5 Gb/s links

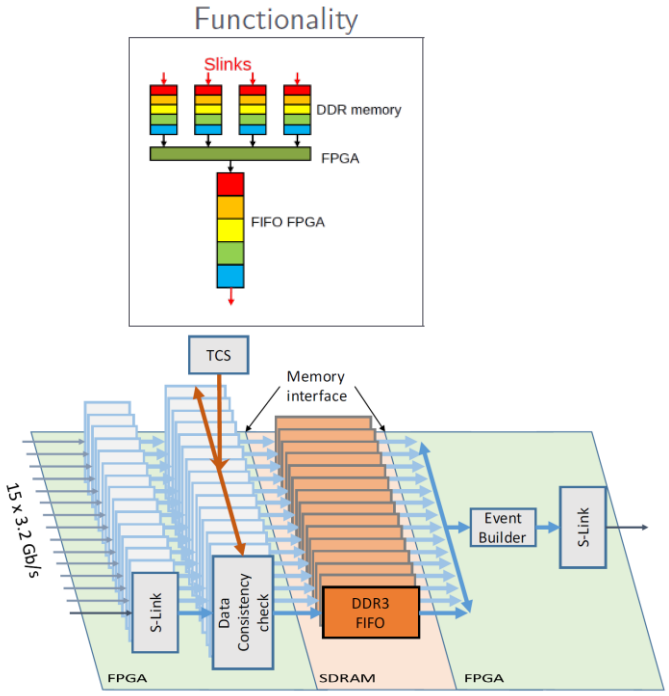
Intelligence elements in hardware:

- Self synchronized data flow (backpressure and throttling)
- FEE Error diagnostics and handling to prevent DAQ crashes
- Automatic resynchronization of FEEs

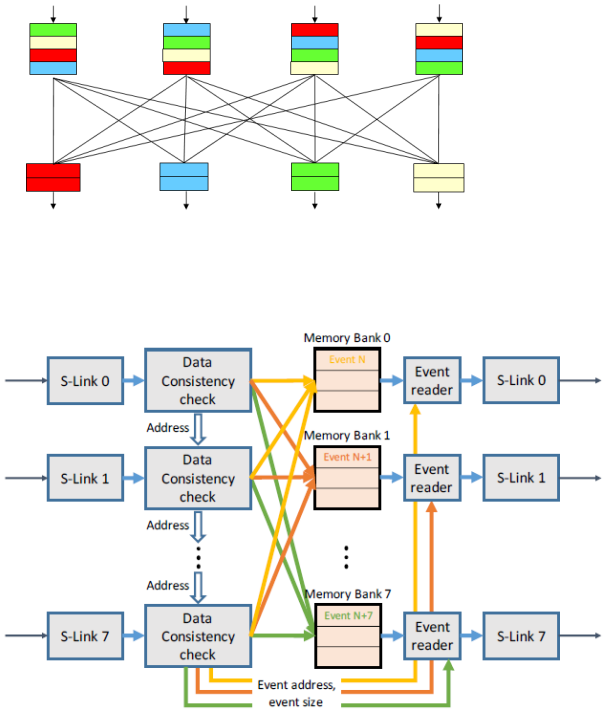
=> FEEs can be attached/detached at any time

iFDAQ Firmware Versions

Data concentrator

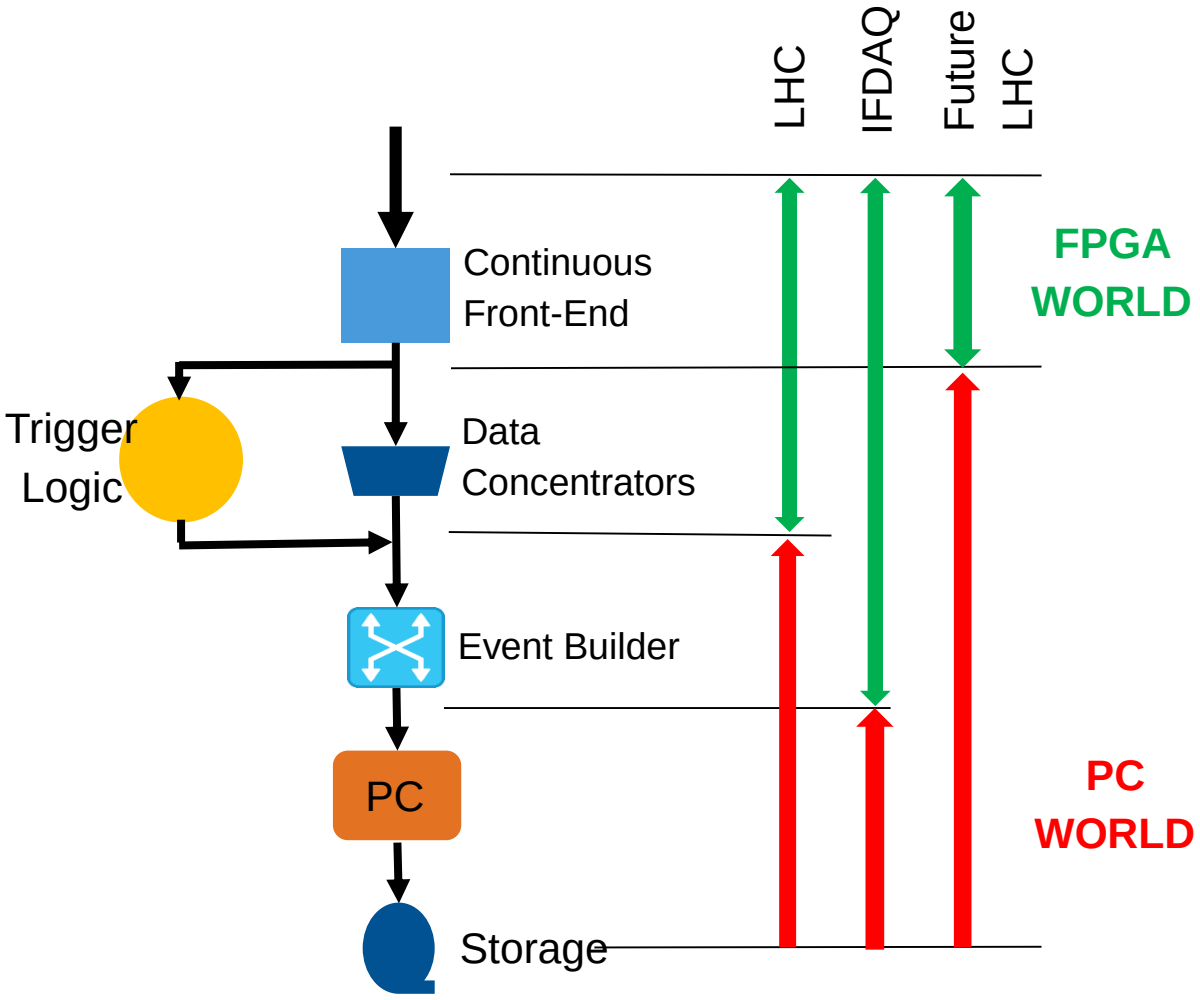


Switch



- Events are processed simultaneously and buffered in DDR, no congestion
- Events distributed between outgoing links in round robin manner
- 2.5 GB/s throughput

DAQ Architectures



Concept of iFDAQ

- **Minimize amount of real-time software processes and implement Event Builder in FPGA**

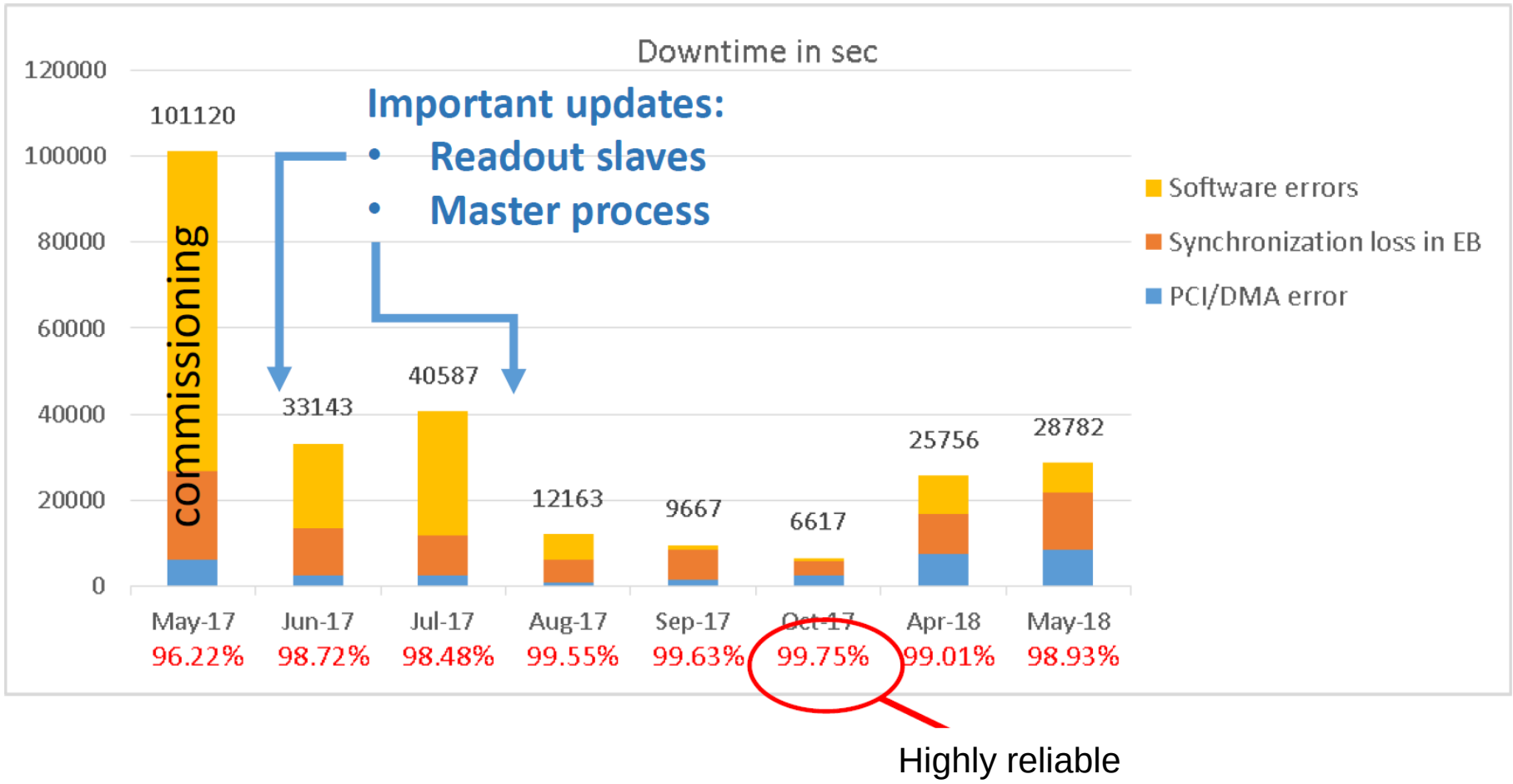
iFDAQ Frame work

- **Implementing congestion free Event Builder in FPGA**
- **Intelligent data handling**
- **Unified Interfaces**
- **Unified IP Cores**
- **Integrated Digital Trigger (to be impl.)**

Advantages

- **Increased compactness**
- **Increased reliability**
- **Reduced cost**

iFDAQ Up Time



COMPASS++/AMBER in 2022-2024

Programme	Physics Goals	Beam Energy [GeV]	Beam Intensity [s^{-1}]	Trigger Rate [kHz]	Beam Type	Target	Hardware additions
muon-proton elastic scattering	Precision proton-radius measurement	100	$4 \cdot 10^6$	100	$\mu^{\pm}$	high-pressure H2	active TPC, SciFi trigger, silicon tracking
Drell-Yan	Pion PDFs	190	$7 \cdot 10^7$	50	$\pi^{\pm}$	C/W	target modification
Input for Dark Matter Search	$\overline{p}$ production cross section	20-280	$5 \cdot 10^5$	25	p	LH2, LHe	liquid helium target, RICH?

Proton Radius Measurement will be first measurement 2022-2023

- Small experimental setup
- Recoil proton (TPC, 60 us drift time) and scattered muon trigger (SciFi, Pixel Silicon)
- Moderate data rate

Motivation and requirements for Trigger less FEEs

Motivation

- Precision measurements => high trigger and data rate
- Complex trigger algorithms
- Flexible DAQ/Trigger architecture

FEEs requirements

- Zero suppression
- Feature extraction

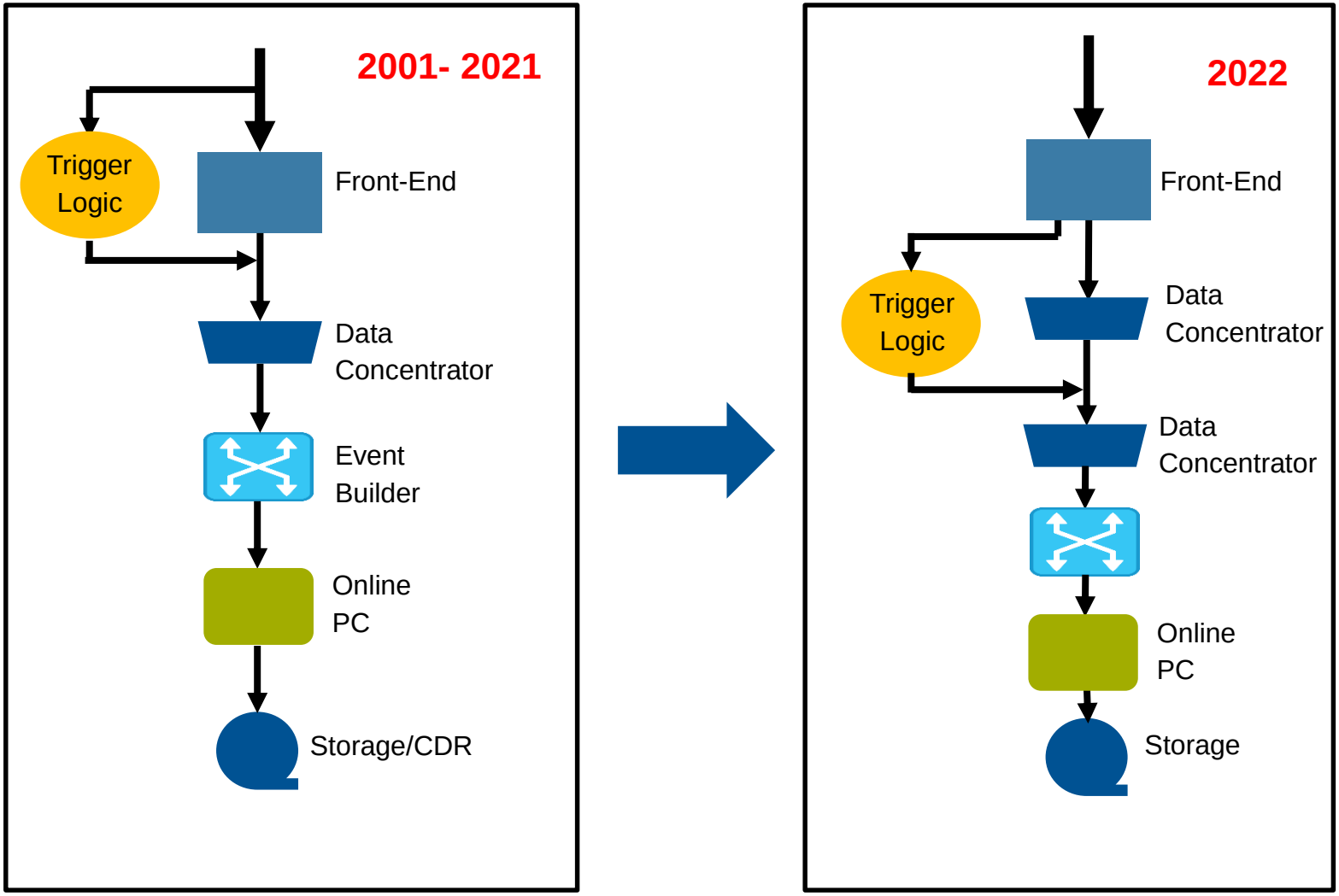
Trigger logic

- Programmable digital logic (FPGA)
- Implementation complex algorithms
- Long latency – up to few seconds

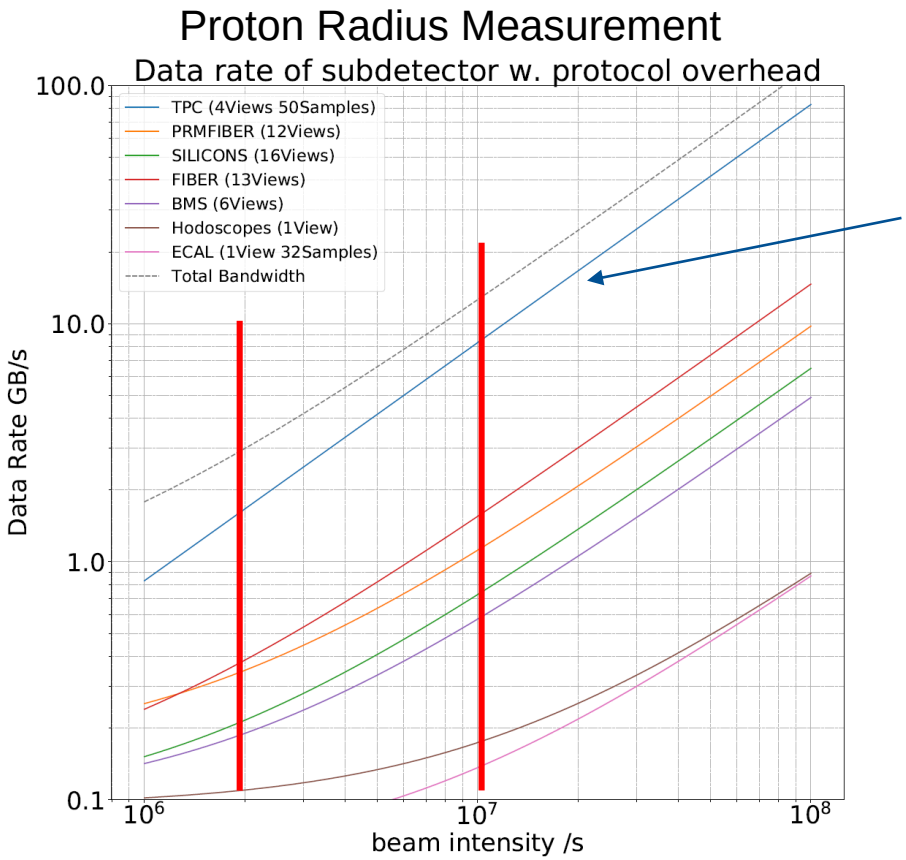
COMPASS++/AMBER TDAQ

- Trigger less front-end electronics
- Programmable Hardware Trigger Processor integrated in DAQ
- iFDAQ upgrade to support both

Evolution of COMPASS DAQ Architecture



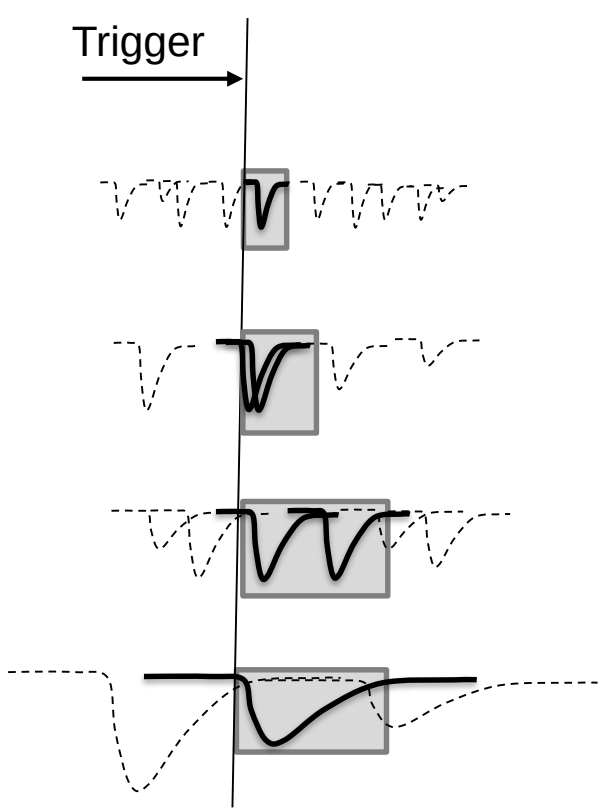
Data Rate



Monolithic silicon pixels
10Mpixels

Programme 2022-2024	Beam Rate	Trigger rate	Non triggered Data Rate	Final Data rate limited by storage
Proton Radius Measurement	$2 \cdot 10^6 - 10^7$	100 kHz	10 GB/s in spill, 3GB/s sustained	< 2 GB/s
Drell-Yan	$7 \cdot 10^7$	50kHz	30 GB/s in spill 10 GB/s sustained	500 MB/s
Input for Dark Matter search	$5 \cdot 10^5$	25 kHz	?	250 MB/s

Data Structure of Standard Triggered DAQ



GATE

SciFi
GATE 20 ns

Si, MM, GEM
GATE 50 ns

Drift Chambers
GATE 400 ns

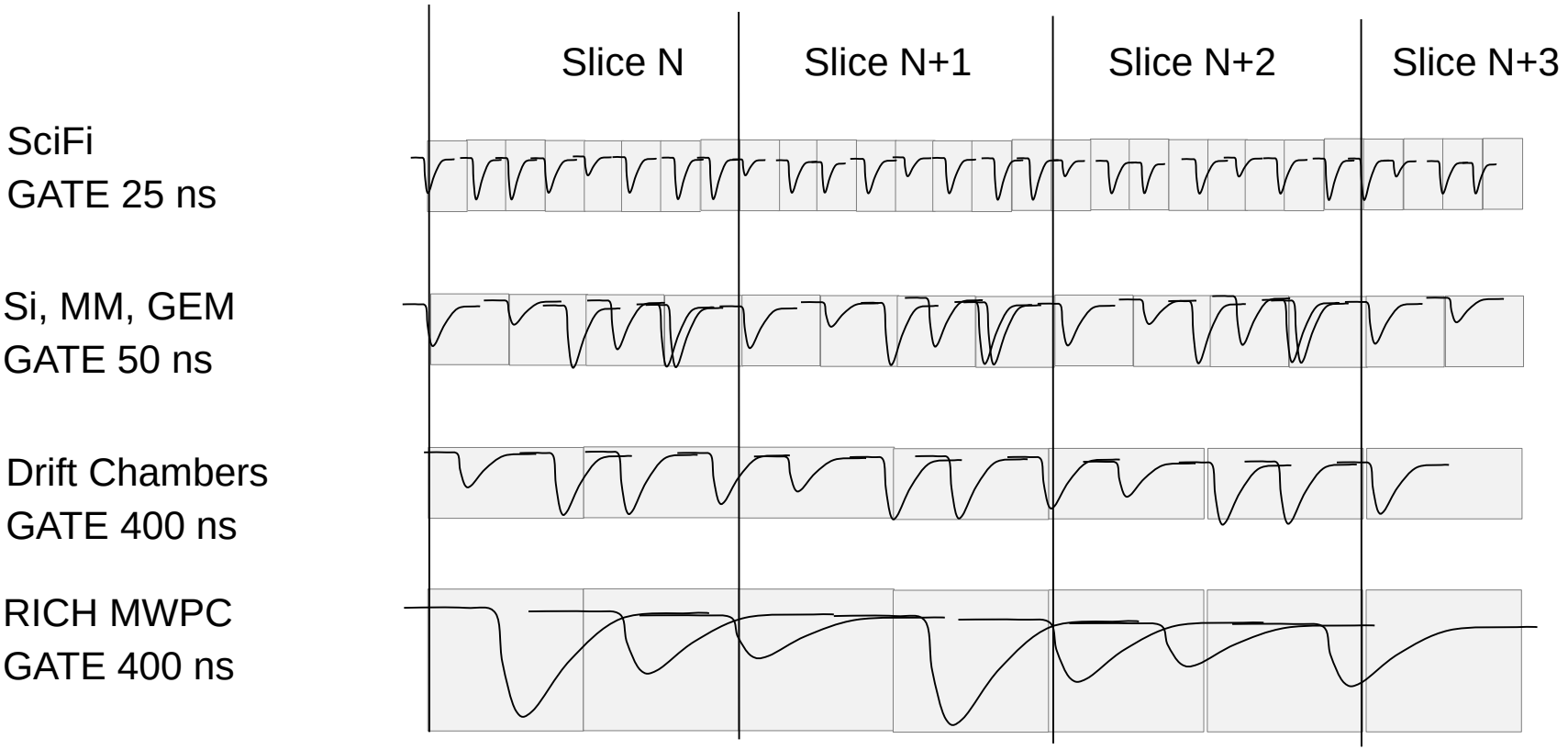
RICH MWPC
GATE 400 ns

Data Structure in Continuous DAQ

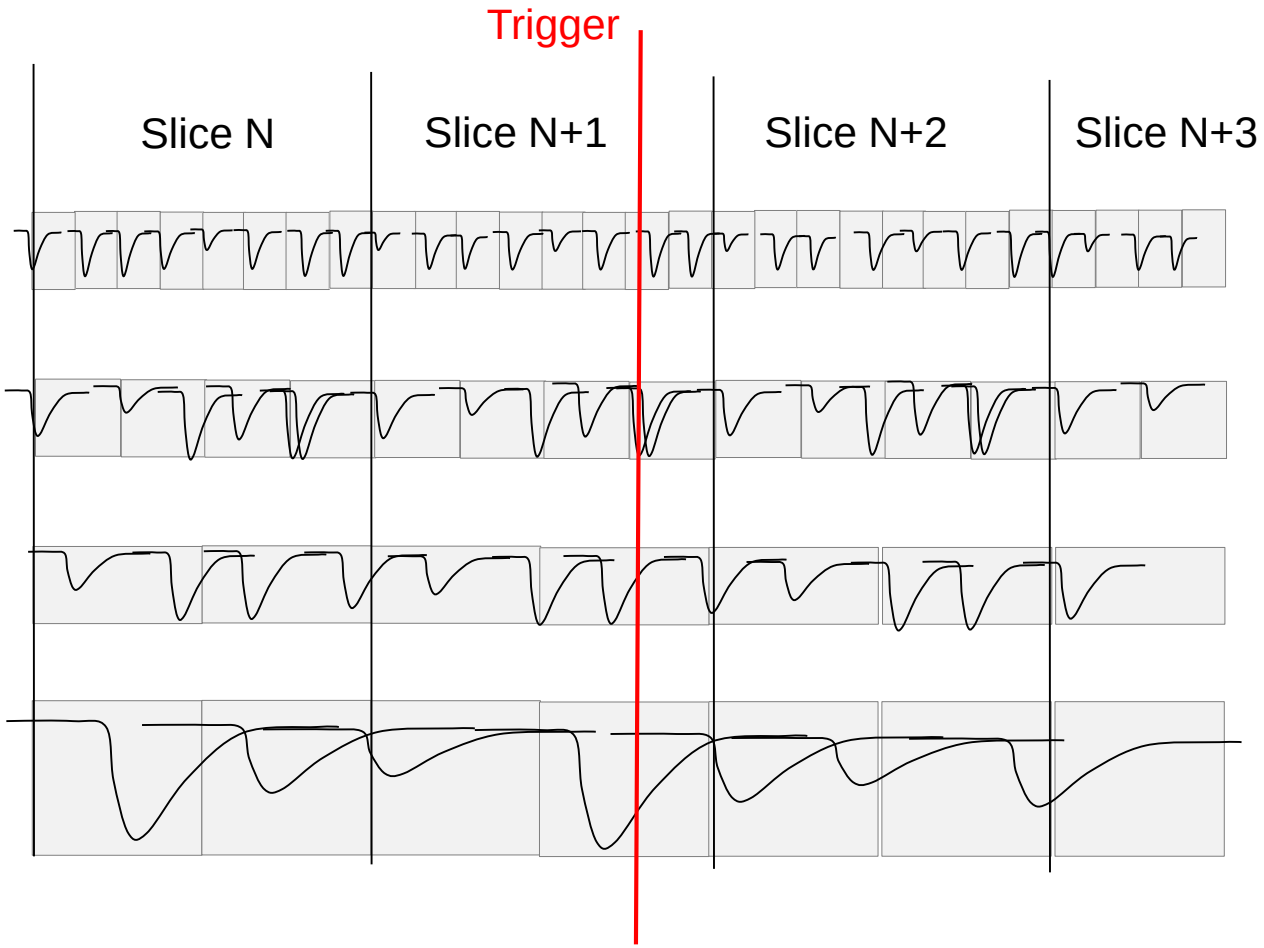
Event is substituted by Time Slice

- Time slice signal is generated with fixed time interval of 200-1000 us
- hits and detector signals of one slice are combined in a one “event”
- Slice length to be optimized to minimize overhead
- Slice length >> detector time resolution
- Slice divided to IMAGEs(gate)
- IMAGE length is constant and individual for each detector

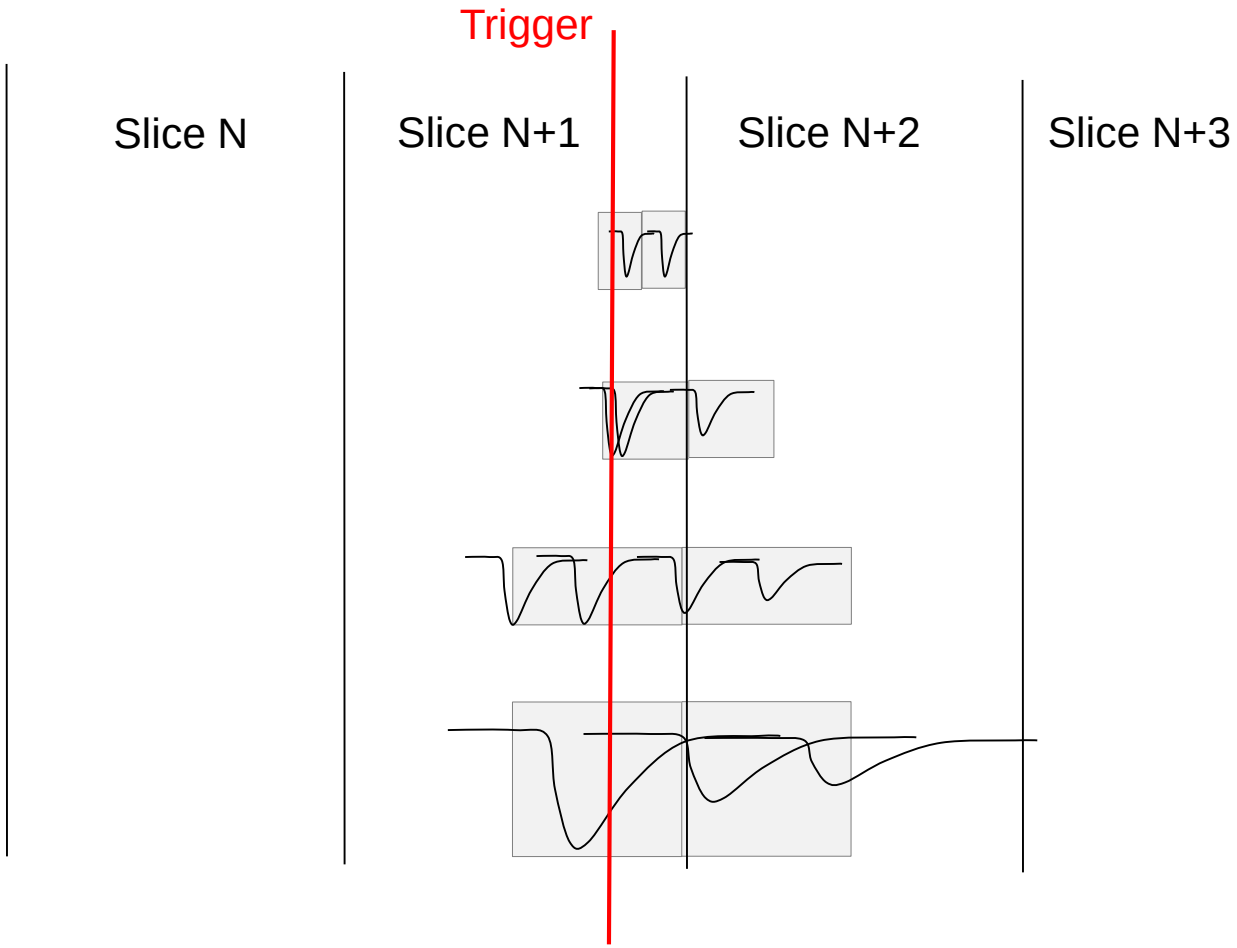
Data Structure of Trigger less DAQ before Trigger



Triggering


Trigger
Slice N
Slice N+1
Slice N+2
Slice N+3
SciFi
GATE 25 ns
Si, MM, GEM
GATE 50 ns
Drift Chambers
GATE 400 ns
RICH MWPC
GATE 400 ns

Triggering



Two consecutive IMAGEs are included in the event

Two Modes of Data Taking

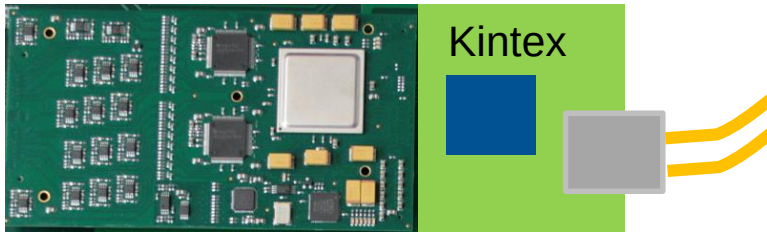
- Trigger less
  - IMAGEs at slice' boundaries are copied to both slices
  - No event definition, no T0
  - Detector alignment
  - Verification of trigger processor

- Triggered
  - Two consecutive IMAGEs of detector information form an event

Front-End Electronics

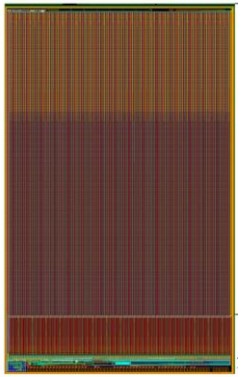
- iFTDC for MWPC, DC, SciFi, CEDAR
  - 64 channels 0.8/0.4 ns bin, 0.25/0.14 ns resolution
  - 32 channels 0.2 ns bin, 80 ps resolution
  - All versions will be available by end of 2019

- MSADC for ECAL, HCAL
  - 16 channel 12 bit @80 MHz
  - Upgrade to Kintex/Zink FPGA, 2020
  - Advanced Signal processing to perform feature extraction, talk Marcin Ziembicki (Warsaw TU, Trieste INFN/ICTP)



Front-End Electronics

- Monolithic Silicon pixel detector MuPix8
  - Developed by Karlsruhe IT for Mu3e experiment @PCI
  - 80x81 um2 pixel size, down to 50um thickness
  - 1x2 cm2 sensor => 2x2 cm2
  - Trigger less read out
  - Being tested now , test beam in fall 2019



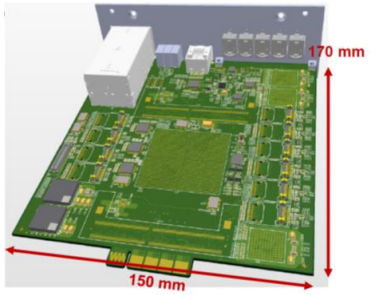
- Micromega, GEM, RICH
  - VMM – under evaluation
  - SAMPA
  - TIGER

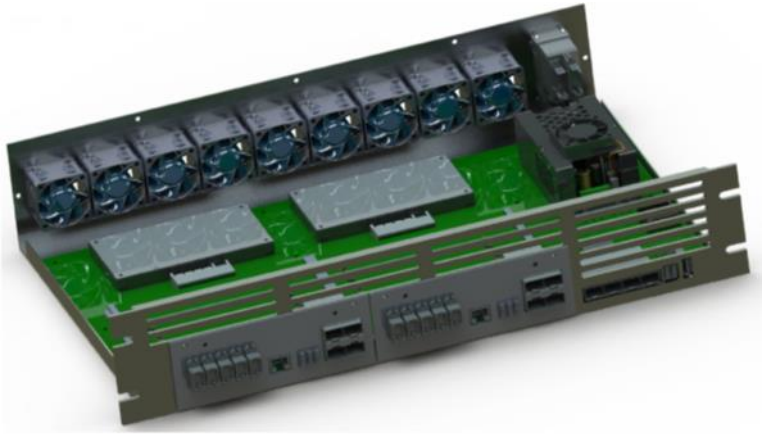
All FEEs will have UDP interfaces for lab tests

DAQ/Trigger Processor Hardware

New DAQ Hardware

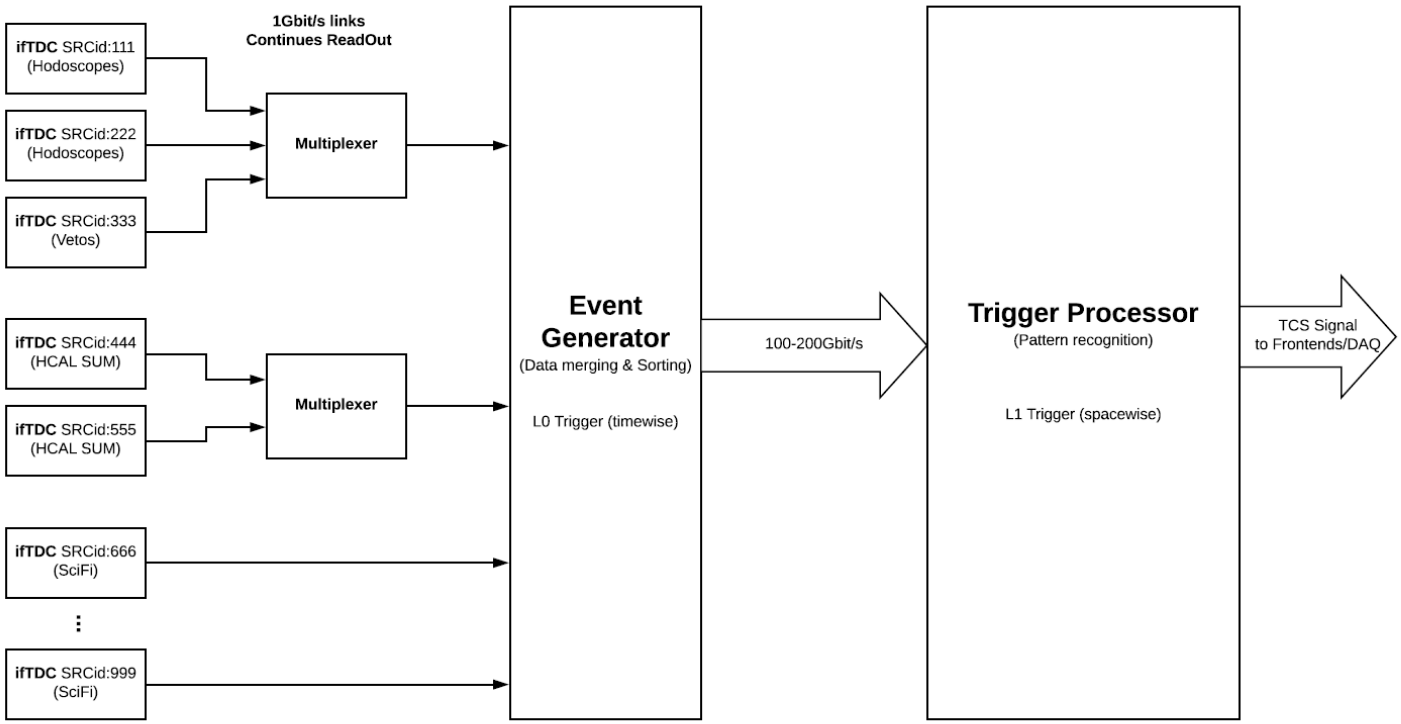
- Xilinx Kintex Ultrascale XCKU095 FPGA
- 32 GB of DDR4 memory
- 60 x 10Gb/s links
- 10 GB/s throughput
- Custom 2U 19” shelf



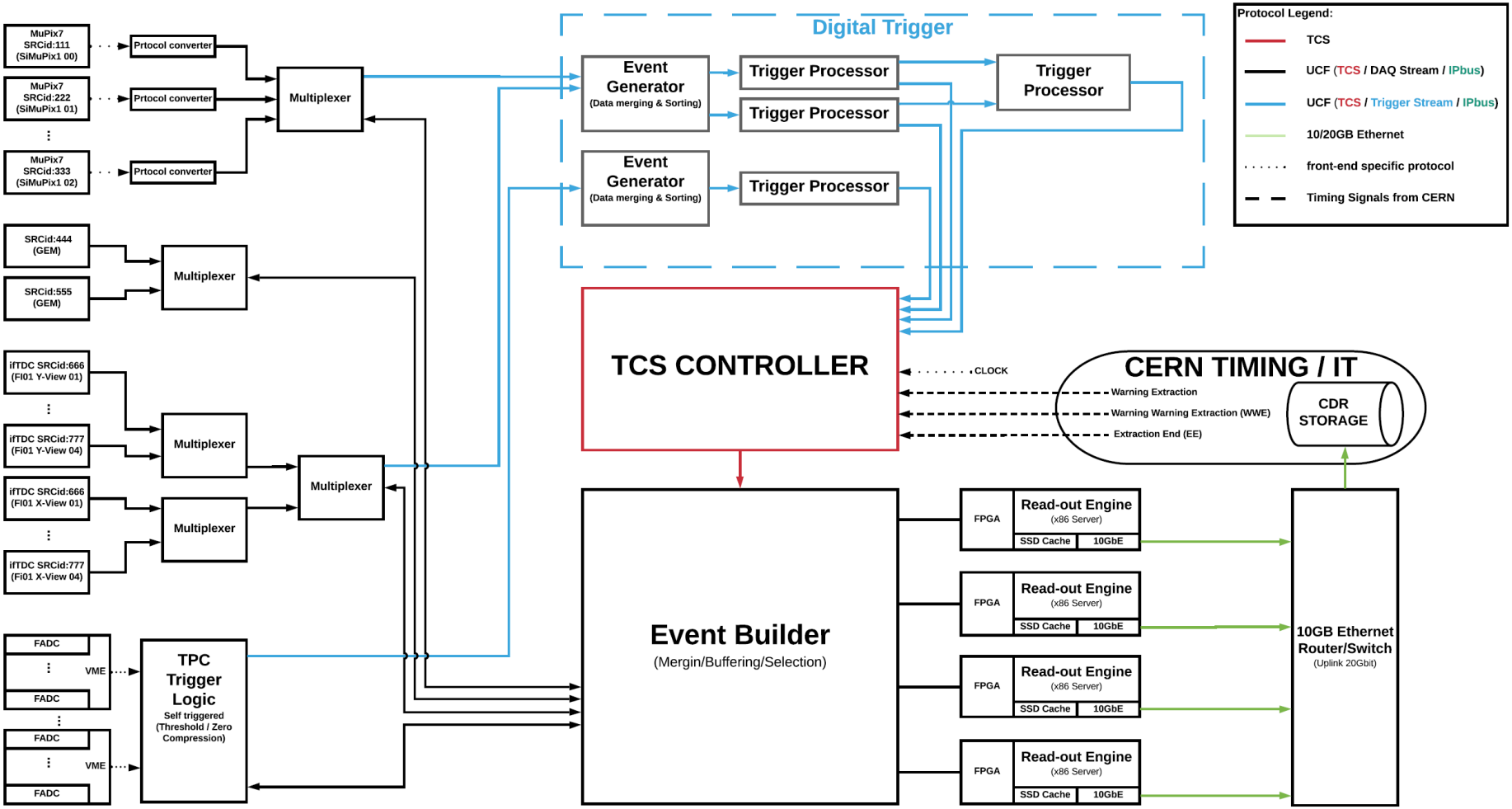


Trigger Processor

Possible Readout Structure



DAQ Architecture



Foreseen Changes in DAQ Architecture

- Trigger less FEEs
- Unified Communication Framework a new protocol for serial links to transmit TCS,Slow Control(IPBUS), and Data with bandwidth from 2-10Gb/s
- TCS (Trigger Control System)
  - Implement command to distribute Time Slices
- New Switch Hardware
  - 10 GB/s bandwidth , scalable to 100 GB/s
- Interface to PCs, expected performance of one server 1GB/s
  - PCIe
  - 10Gb Ethernet
- Digital Trigger Processor

Time line :

- First DAQ test in 2021
- First physics run in 2022 without data reduction i.e. without trigger
- Full performance physics run in 2023

Summary

- Evolution of triggered DAQ to continuous DAQ with built-in trigger processor
- Employing or adapting existing IP cores
- Triggered and non triggered operation modes
- Development of trigger less front-end electronics : iFTDC, Pixel Detector, MSADC
- Development of digital trigger processor
- DAQ bandwidth of 10 GB/s scalable to 100 GB/s,

acquiring big amount of data is not difficult, reduction of data is more challenging

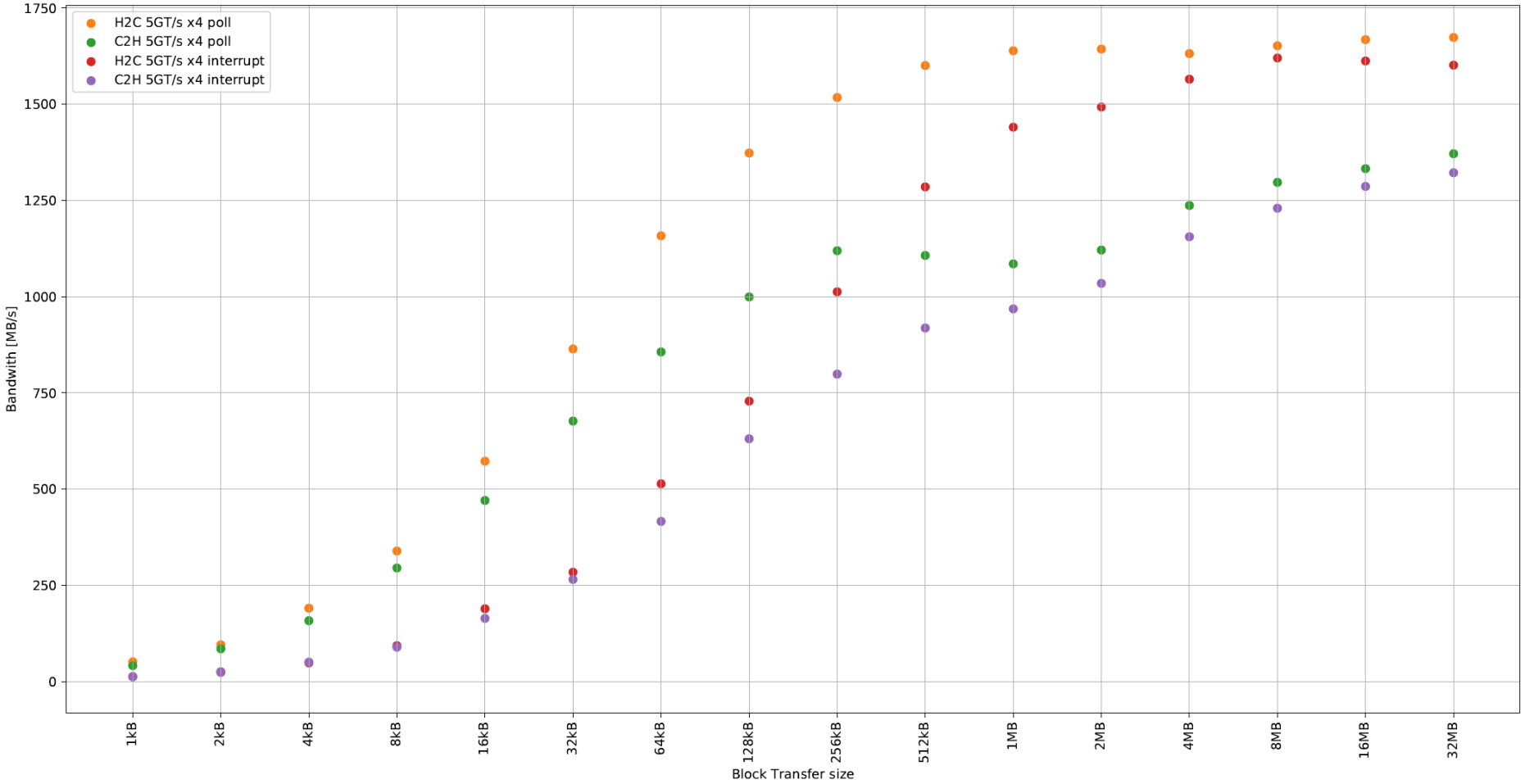
Other Activities

- Performance of RAID controllers, PCIe interface, and Read out process
- Software data generator
- Simulation of DAQ architecture using OMNeT++
- Software verification of digital trigger processor

Performance Tests of Online PC

Verify a possibility to achieve 1GB/s sustained performance of single PC

PCIe Performance with Kintex Ultrascale FPGA



RAID Controller Performance

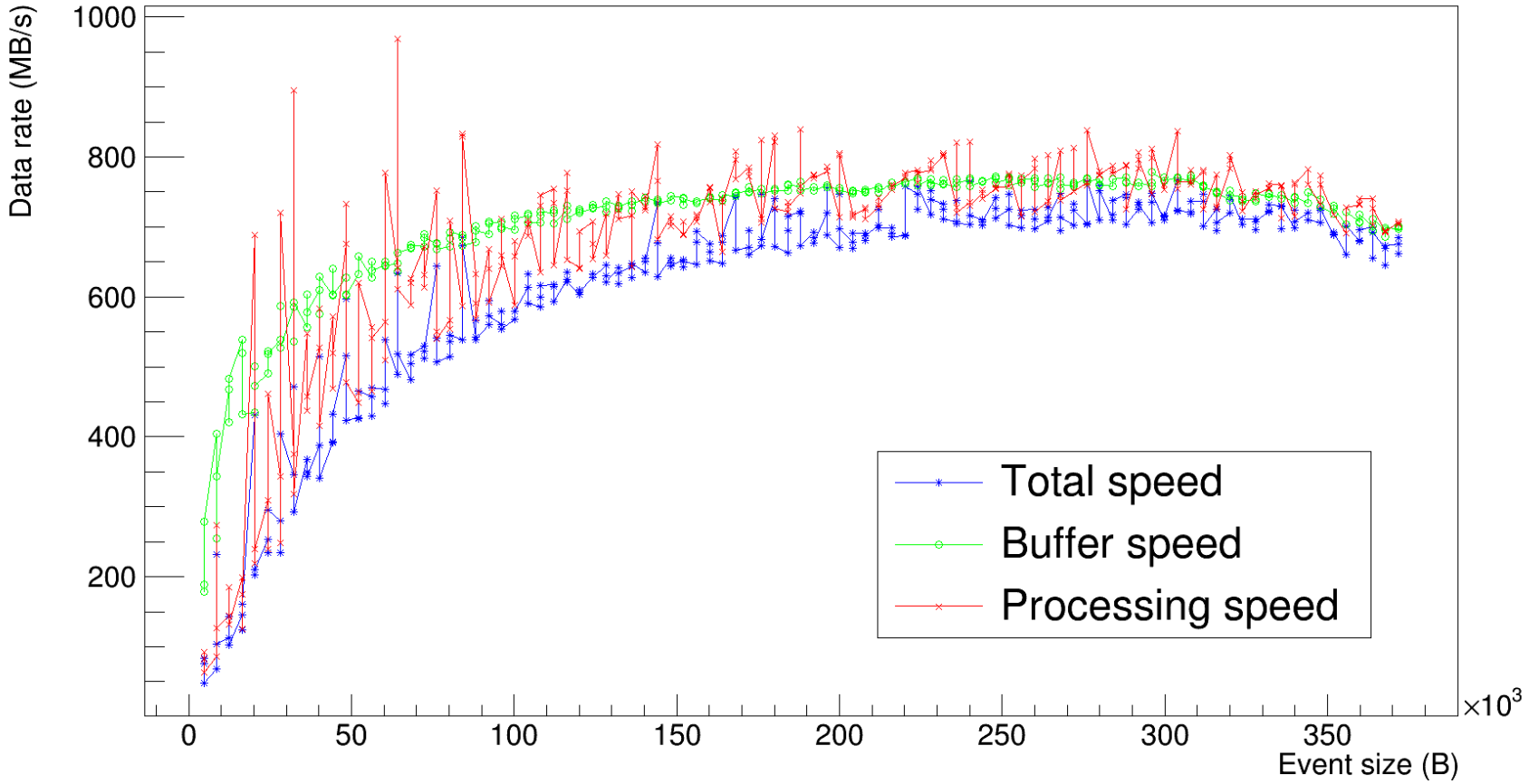
SLC6.9_64bits, 2 x Xeon E5-2620 v2 @2.1GHz, 8 HDDs

RAID Configuration	Write Speed	Read Speed	Copy Speed
RAID10, 7.2TB, ext4	500 MB/s	510 MB/s	230 MB/s
RAID0, 15TB, ext4	724 MB/s	1100 MB/s	342 MB/s
RAID5, 13TB, ext4	681 MB/s	705 MB/s	246 MB/s
RAID6, 10.9TB, ext4	577 MB/s	665 MB/s	243 MB/s
RAID0/1, disks: 0-3, 7.271TB	577 MB/s	576 MB/s	234 MB/s
RAID0/2, disks: 4-7, 7.271TB	568 MB/s	572 MB/s	228 MB/s
RAID0/1 and RAID0/2	560 MB/s	570 MB/s	415 MB/s

Increase performance to 1GB/s

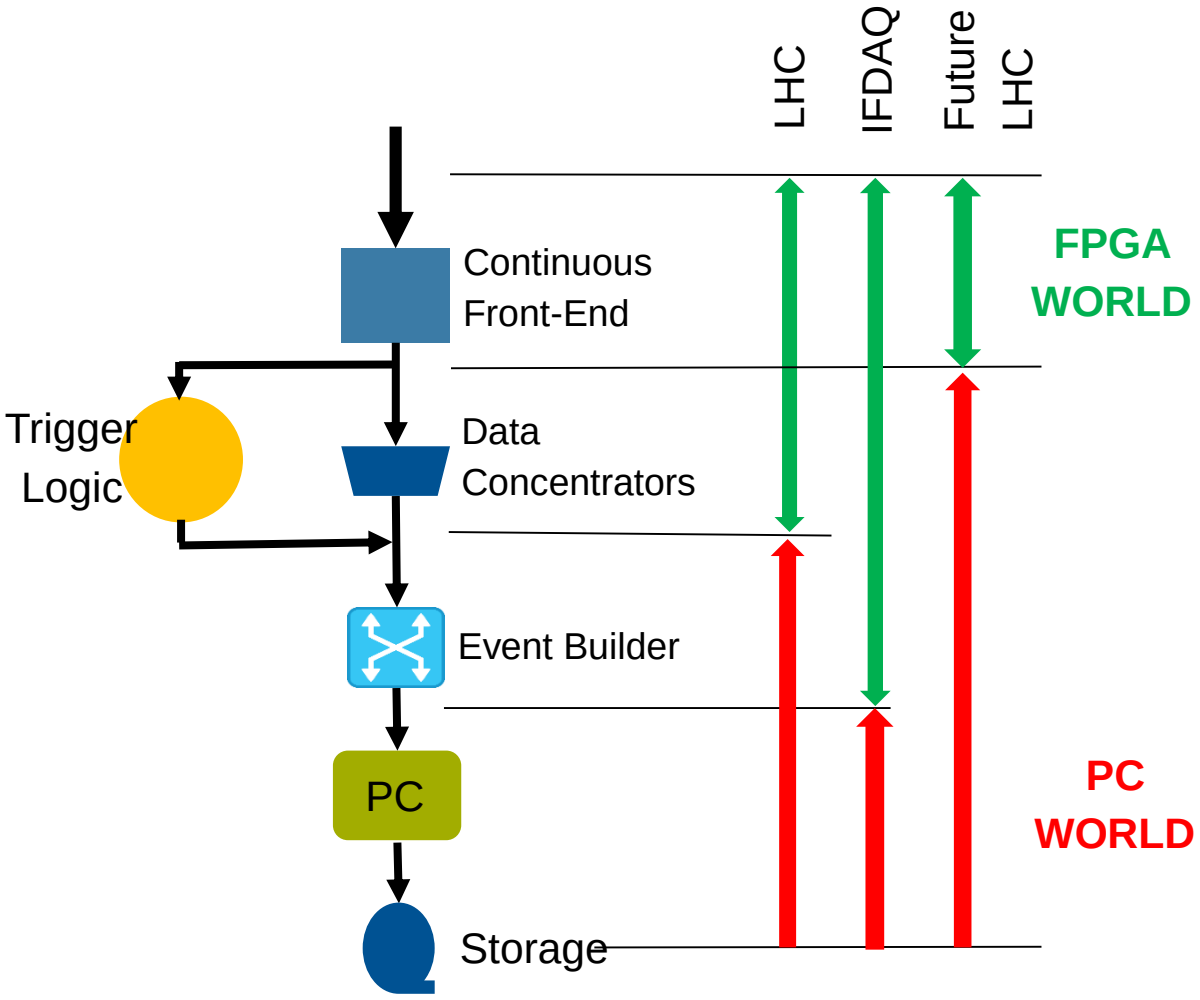
- Increase number of HDDs
- Increase number of RAID controllers

Readout Slave Process Performance



THANK YOU

DAQ Architectures



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iFDAQ Frame work

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Advantages

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Trigger Processor

Develop Trigger Processor frame work for implementation of different algorithms
Frame work includes

- Detector interface, UCF
- TCS receiver
- Chronological sorting of hits
- Forming event candidates
- Trigger interface to TCS