Design of Silicon Module prototype for Vertex Detector SPD

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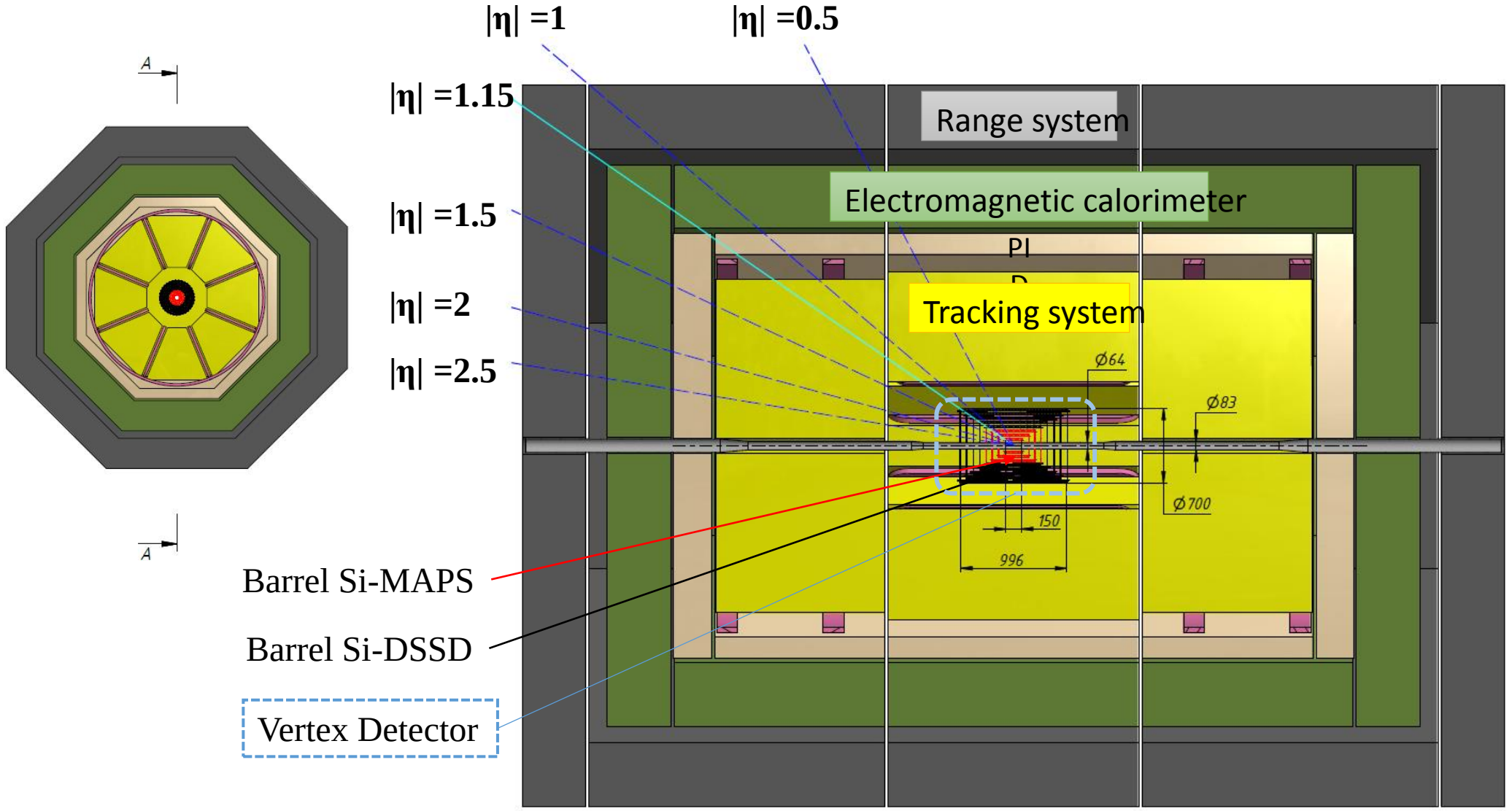
Main goal of prototype

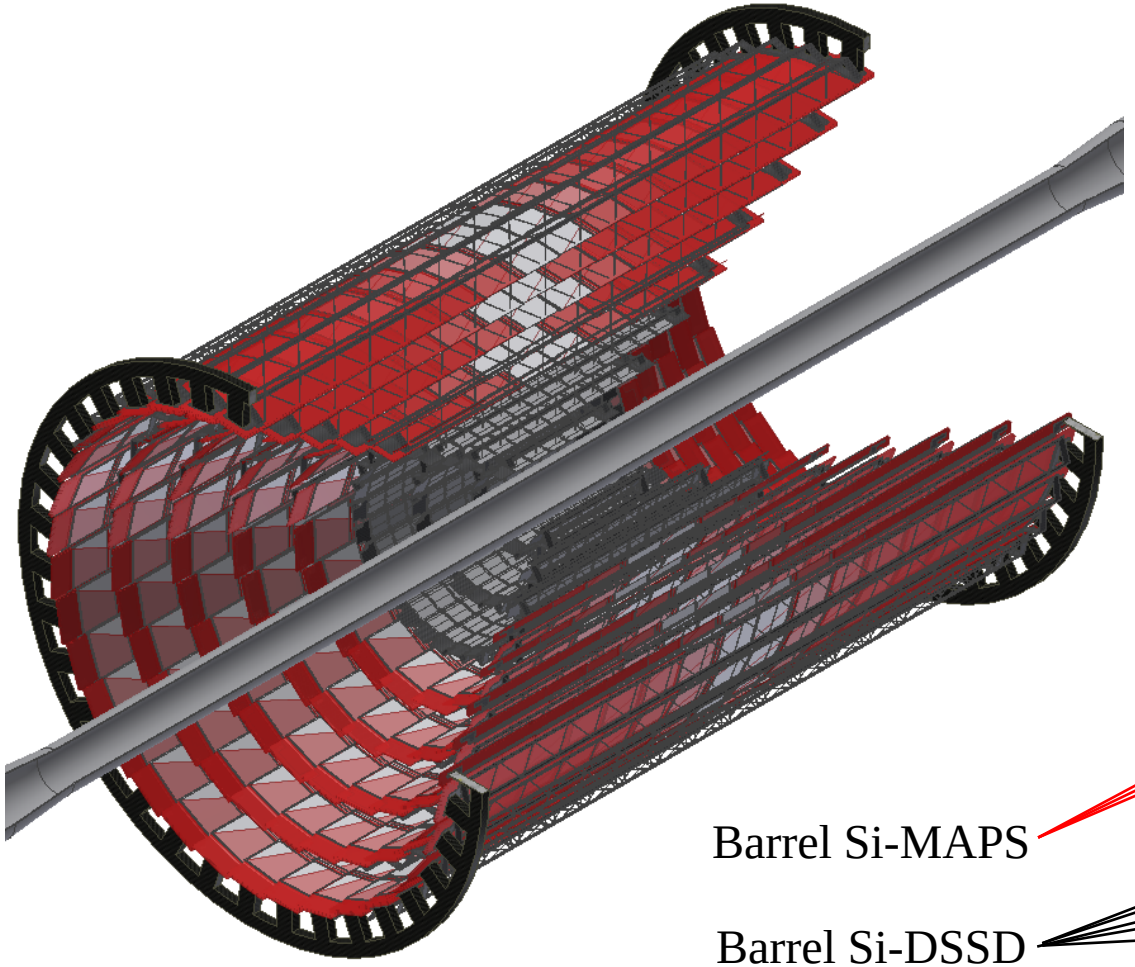
From general conditions of SPD facility it's necessary to minimize material budget over the track paths. That's why the main goal of prototype is to study possibility of production double-sided silicon strip detector (DSSD) module which connects to front-end electronics via thin low-mass microcables and test it for satisfaction m.i.ps detection (noise, cross-talks, common noise).

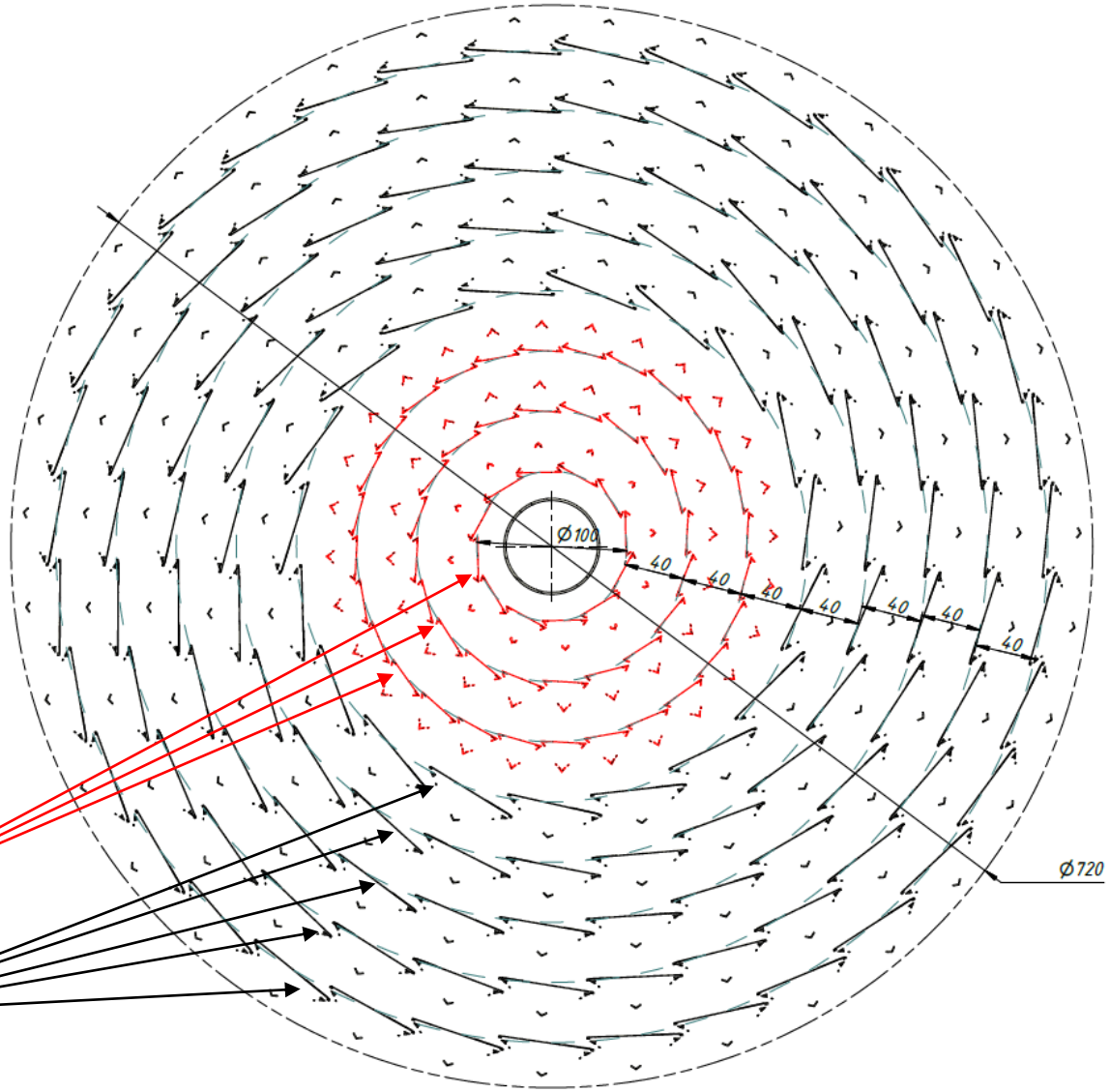
SPD facility



General view $r\varphi$-plane (left) and rz-plane (right) of the SPD detector

Vertex Detector Layout





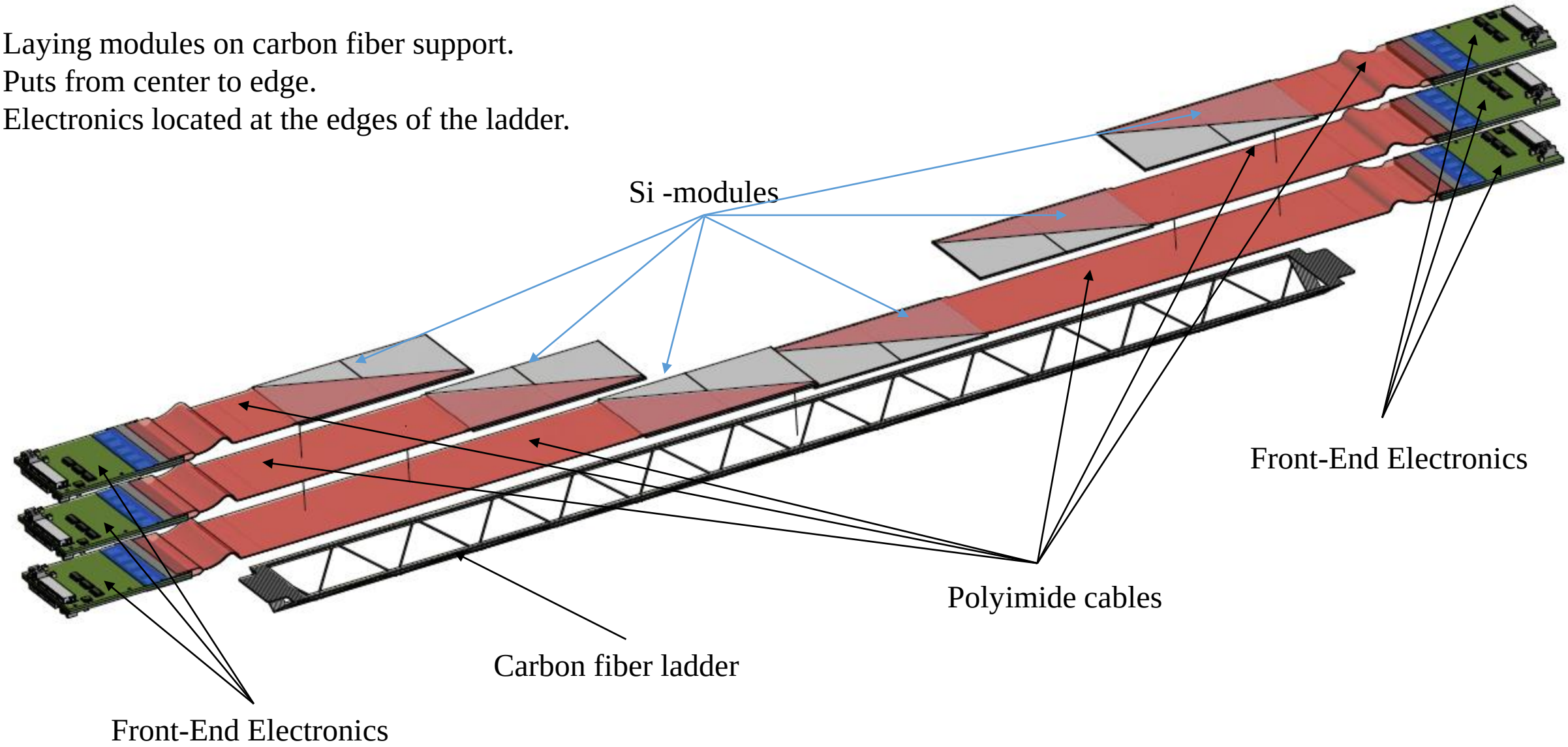
Barrel Si-MAPS

Barrel Si-DSSD

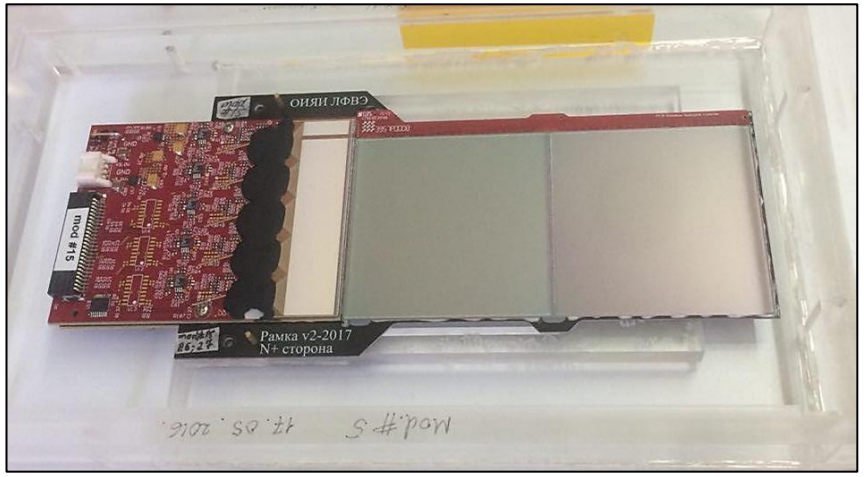
General view of Vertex Detector (left) and $r\varphi$-plane (right)

View of carbon fiber ladder with Si-modules

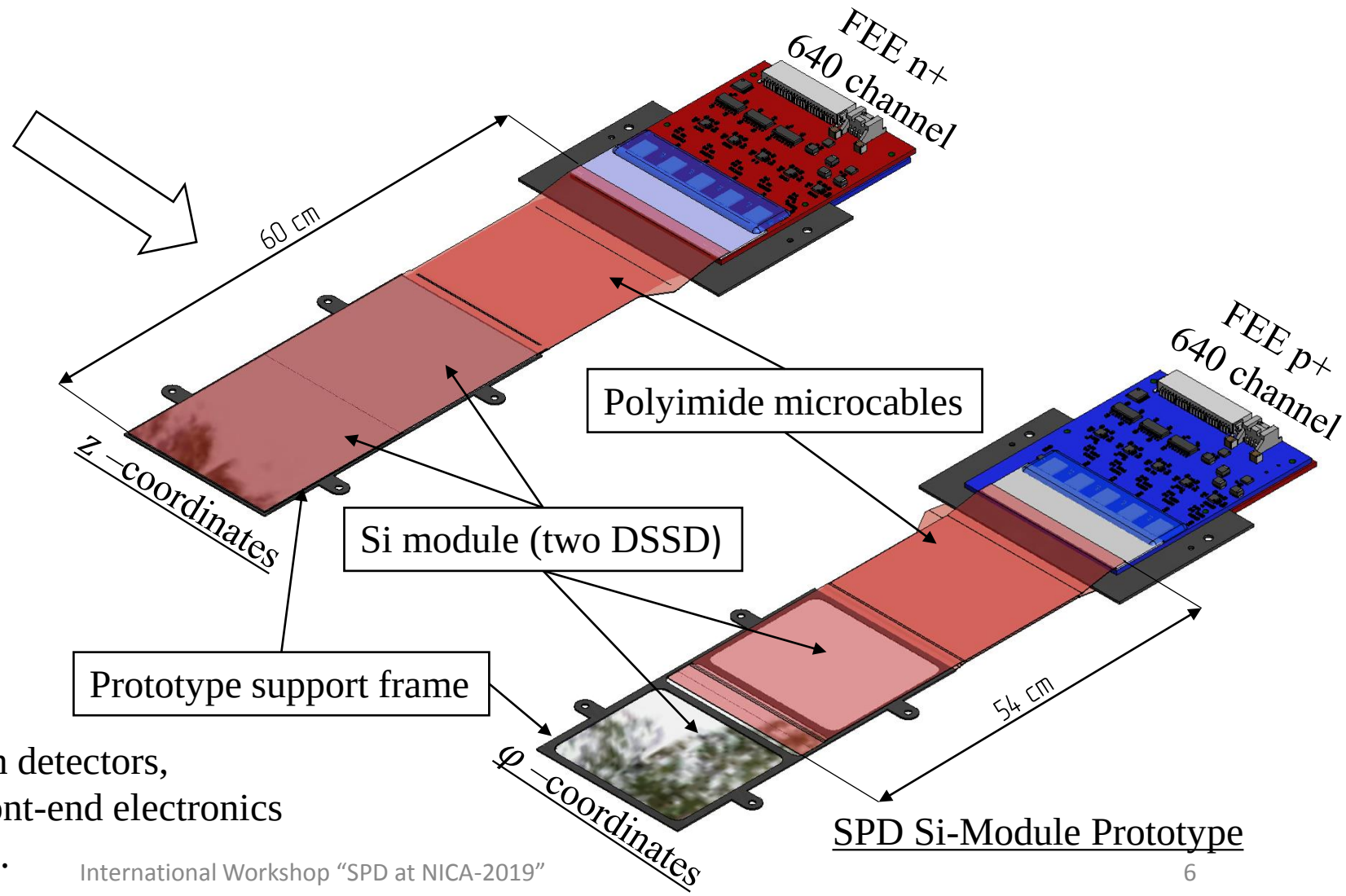
Laying modules on carbon fiber support.
Puts from center to edge.
Electronics located at the edges of the ladder.



Module prototype



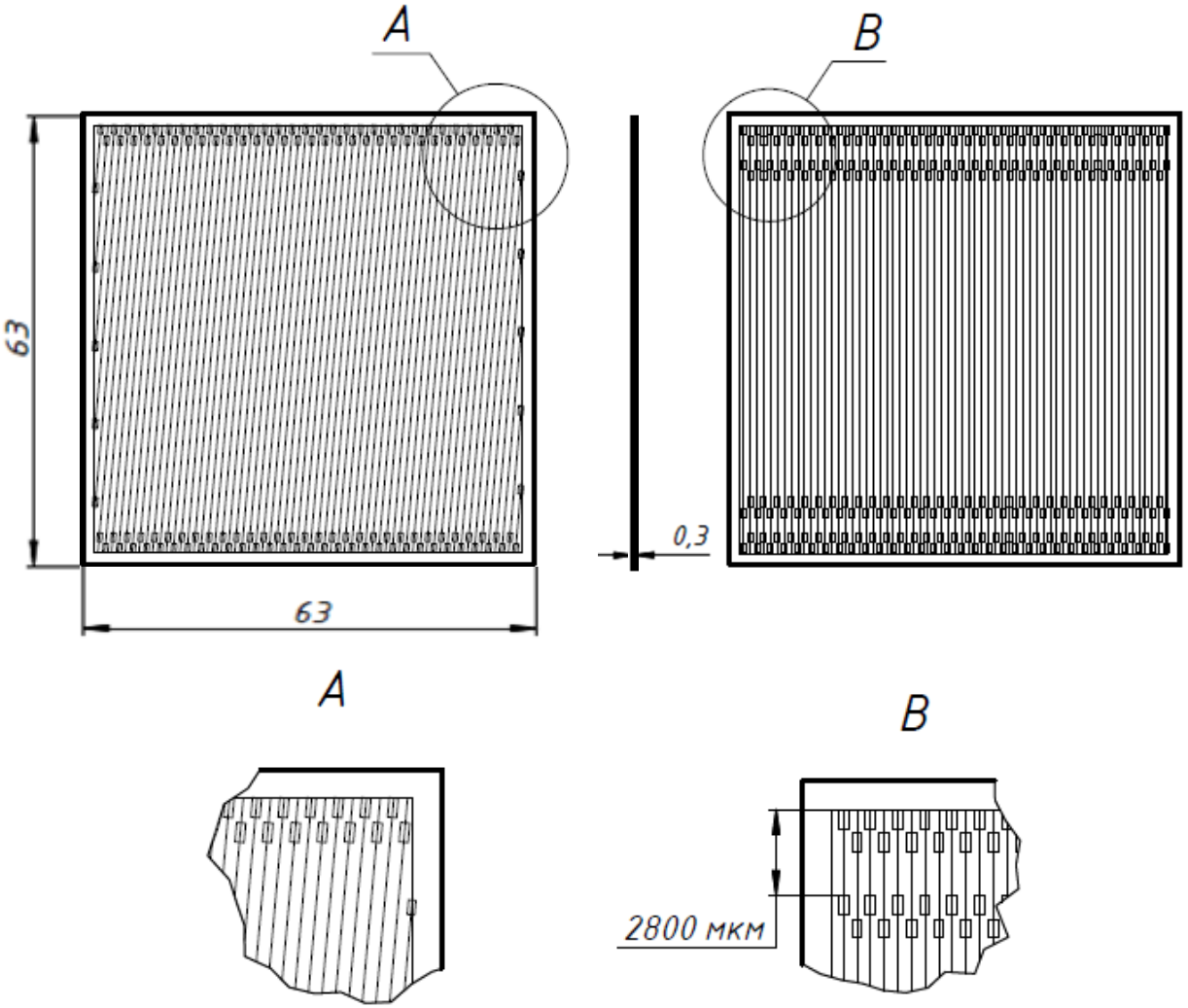
BM@N Si-Module



SPD Si-Module Prototype

The module consists of two silicon detectors,
glued to the frame and connected with front-end electronics
via thin polyimide cable.

Detector’s topology



DSSD prototype (BM@N version)

- Size: 63x63x0,3 mm^3 (on 4” – FZ-Si wafers)
- Topology: double side microstrip (DSSD) (DC coupling)
- Pitch p^+ strips: 95 μm;
- Pitch n^+ strips 103 μm;
- Stereo angle between p^+/n^+ strips: 2.5^0
- Number of strips: 640 (p^+)× 640(n^+)

Today we have enough amount detectors of this type – good point to start prototyping

Low-mass microcables

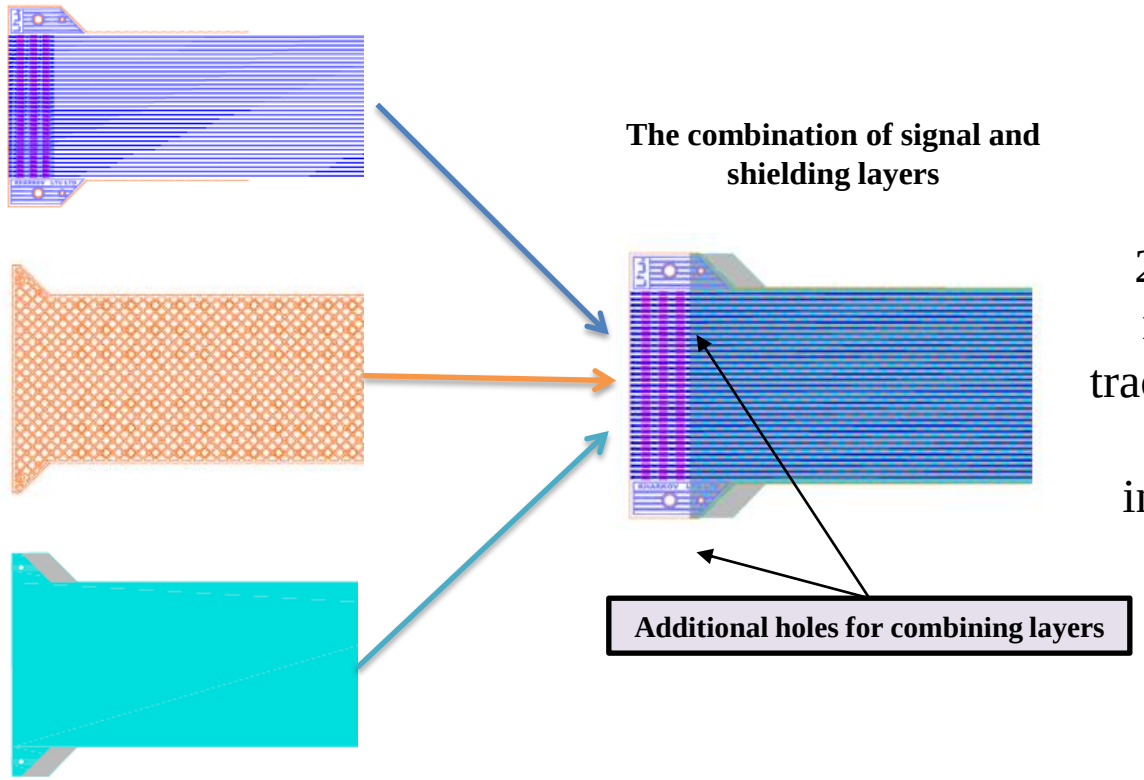
Manufacturing: LED Technologies Ukraine. Ukraine, Kharkiv
viatcheslav.borshchov@cern.ch, maksym.protsenko@cern.ch

Maximum cable length 600 mm

FDI-A-24
Signal layer
Al 14 μm ($x/X_0=2{,}46\cdot10^{-5}$)
Polyimide 10 μm ($x/X_0=5{,}83\cdot10^{-5}$)

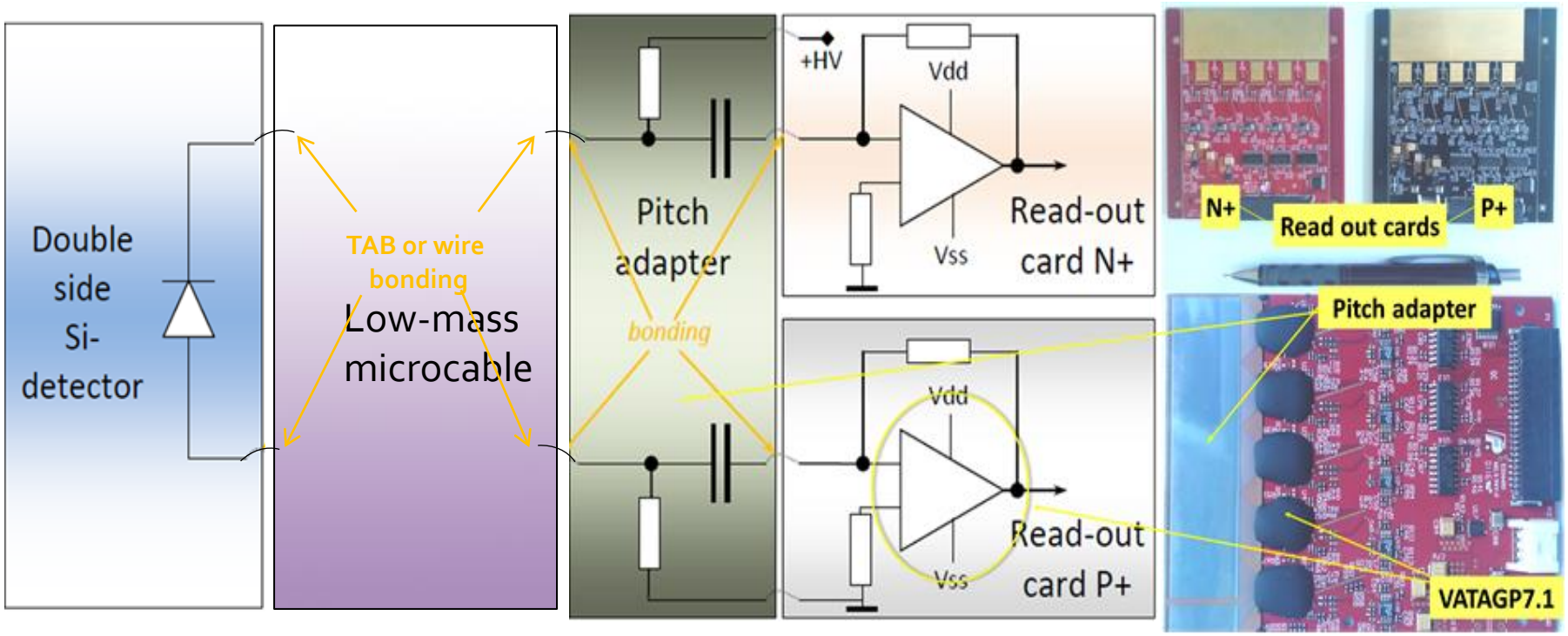
Polyimide layer
(perforated or solid)
Polyimide 50÷100 μm
($x/X_0=(1{,}23\div2{,}46)\cdot10^{-4}$)

Shielding layer
Al 14 μm ($x/X_0=1{,}2\cdot10^{-4}$)



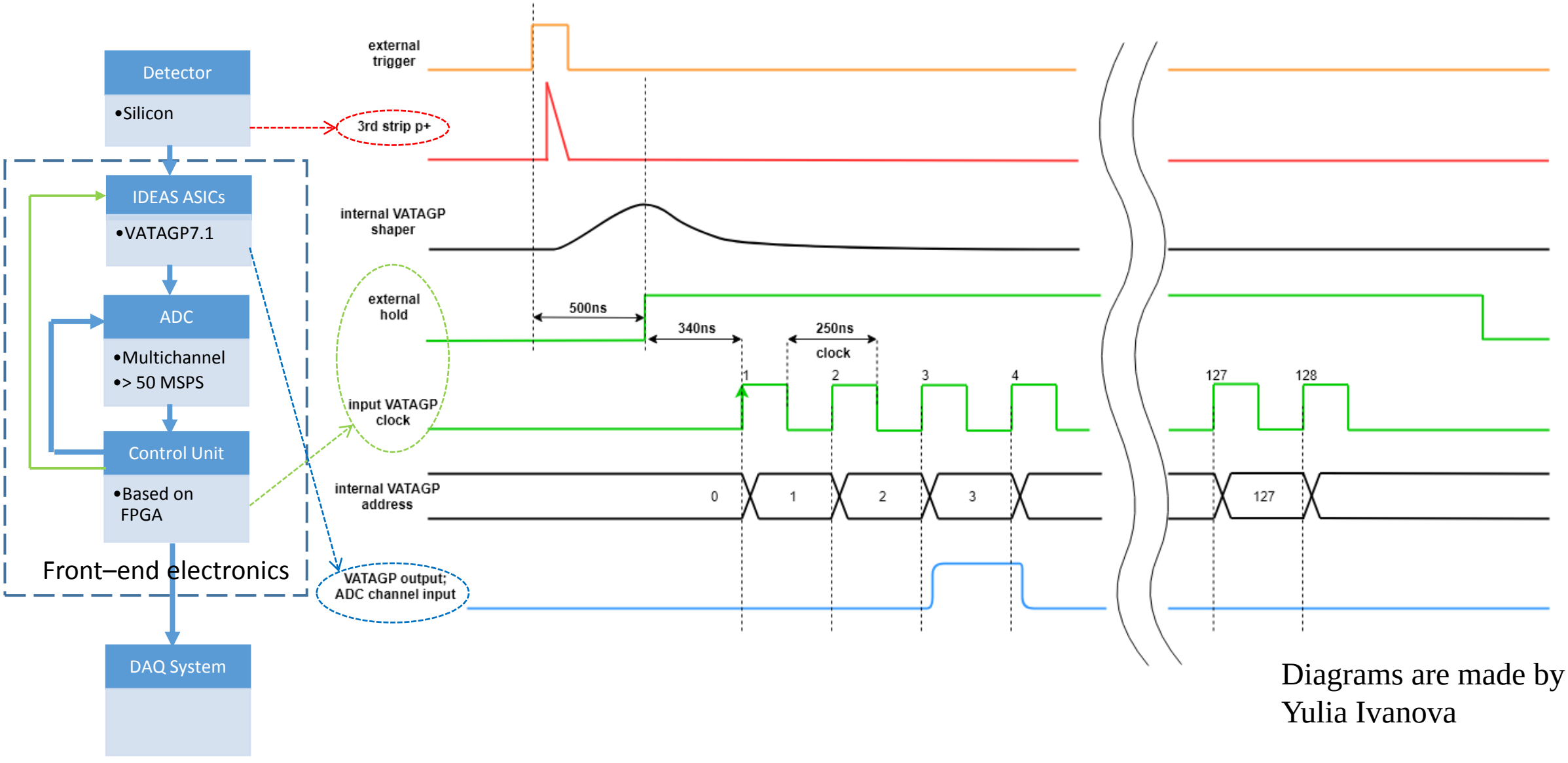
2 variants for wire and TAB bonding
number of layers, their thicknesses,
traces pitch, number of bonding windows
and topology of signal layer
in the phase of negotiation with LTU

Pitch adapter



DSSD with DC topology doesn't contain integrated resistors and capacitors (RC), therefore external R, C are required to supply bias voltage to each strip and to electrically decouple the DC current from the electronic inputs. This role is performed by Pitch Adapter (PA) with a topology of two types for p+ and n+ sides of the detector. In addition, PA has topology of contact pads similar to chips located on the side of electronic chips. PA modules are made on sapphire plates with an epitaxial layer of silicon (SOI). Integrated poly silicon bias resistors have a value of 0.7 – 1.0 MΩ, decoupled capacitors have a value of 140 pF. PA is assembled together with read-out ASICs on the read-out card. Positive polarity signals come from detectors to P+ read-out card (black PCB) while negative signals come to N+ read-out card (red PCB).

Serial read-out diagram



Diagrams are made by Yulia Ivanova

Parameters of read-out chips

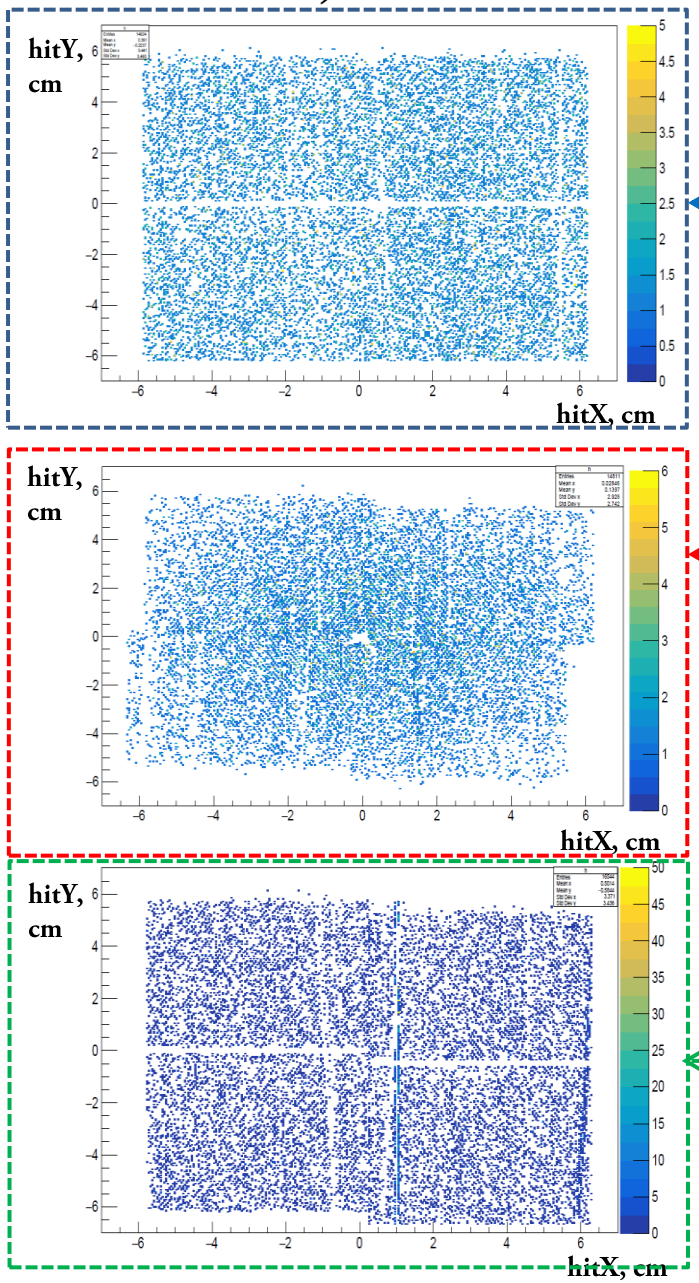
	ASIC VATAGP7.1
Number of CSA	128 channels
Input charges (dynamic range)	±30 fC
Peaking time (slow shaper)	500 ns (typ.)
Peaking time (fast shaper)	50 ns
Noise (ENC)	70e +12e/pF (typ.)
Lowest threshold (no capacitance)	0.12 fC
Voltage supply	+1.5V, -2.0 V
Gain from input to output buffer (diff. output currents)	16.5 μA/fC
Output Serial analog multiplexer clock speed	3.9 MHz
Power dissipation per channel	2.2 mW

Test plans of prototype

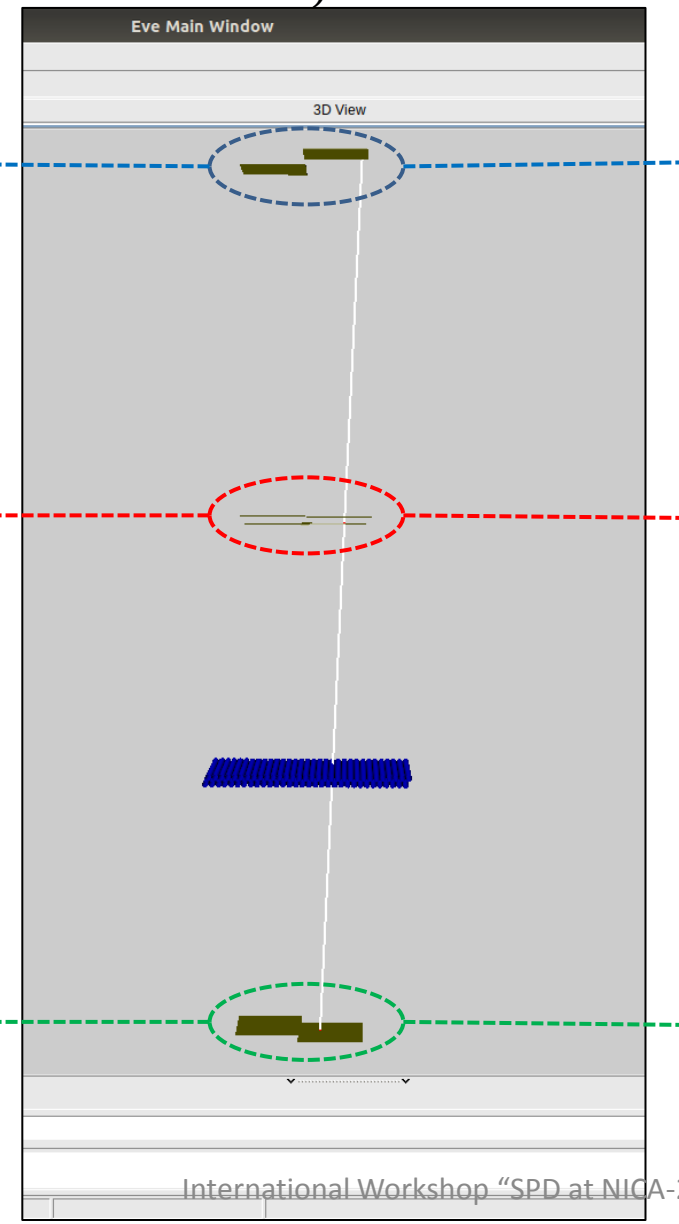
1. Scan I-V and C-V for DSSDs and PAs before assembly;
2. Make pedestal run for Front-end electronics;
3. Scan I-V and C-V of Si-module (DSSD+cables+PA+FEE) after assembly;
4. Test runs with m.i.p (cosmic);
5. Compare with BM@N module results.

BM@N Si-modules in muon stand (miniSPD)

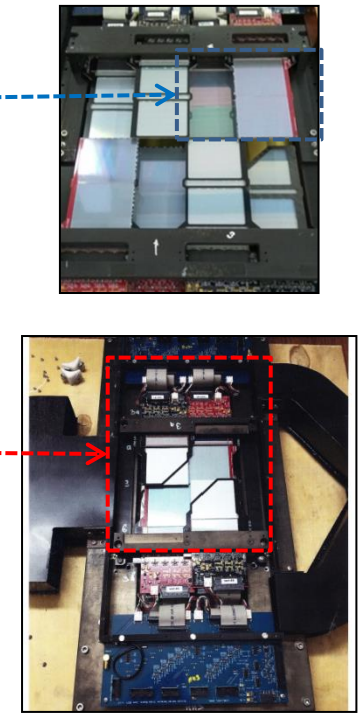
a)



b)



c)



d)

a) Hits plots in BM@N Si-modules;
b) Reconstructed track in miniSPD setup;
c) BM@N Silicon modules;
d) Photo of miniSPD setup.

Muon stand made in cooperation with SPD Straw group

Summaries

- First version of Silicon Module prototype for Vertex Detector SPD is going to be based on the BM@N modules (DSSD, 300 μm, 2.5° stereo angle between strips, DC coupling). Now there are enough amount detectors and pitch adapters for the prototype;
- To reduce material budget in tracker volume it was decided to take out front-end electronics via thin low-mass microcables. 2 variants cables bonding (TAB and wire), topologies in the phase of negotiation with LED Technologies Ukraine;
- First version of FEE is going to be based on commercially available ASICs VATAGP7.1 (IDEAS, Norway). There are enough amount these ASICs and PCBs for the prototype;
- Drawings of prototype support frames in progress.

Welcome everyone to join the Vertex Detector SPD collaboration!