TGC Charge Monitor board. (TGC CHMon. board)

S.Kuleshov with G.Mikenberg and A.Abusleme

The project for the Chilean Cluster

Feb.19th of 2019

DAQ group of the Chilean Cluster

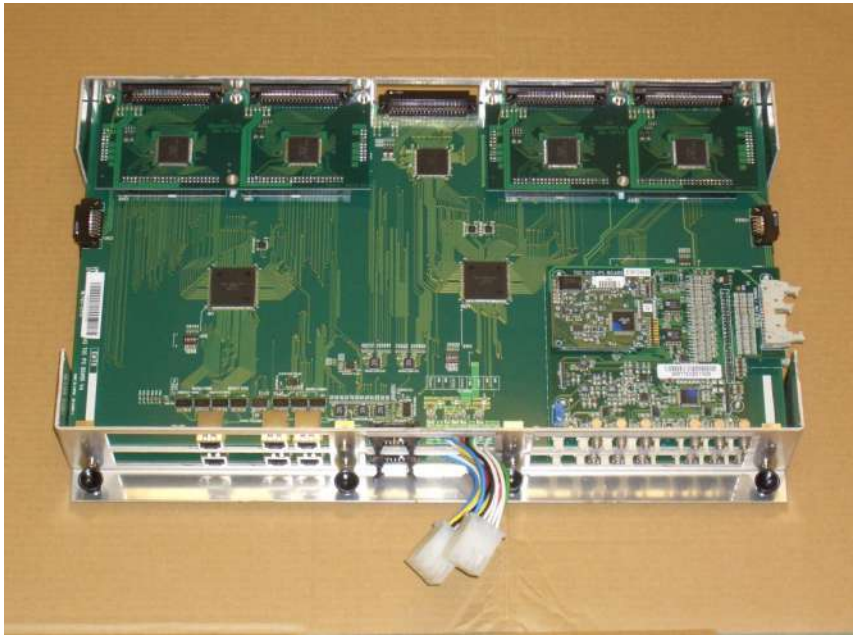
- Electronic department and physics department of Universidad Andrés Bello (2 professors, 1 young scientist, 2 electronic engineers, 1 phd. student, 2 technicians, 4 students). The president and management of the university are willing to create a center for work on Phase II upgrade of ATLAS.
- Electronic department of PUC (Santiago) (1 professor, 3 students)
- Electronic department of UTFSM (2 professors, 2 students)
- Detector laboratory of UTFSM (1 scientist, 2 electronic engineers, 1 phd student, 2 students)
- G.Mikenberg visit PUC, UTFSM and UNAB in January 2019. During discussion about a possibility to make a TGC charge monitor we decided that a monitor board with DRS4 chip could be a good solution.
- We think that a possibility to get "oscilloscope picture" from selected channels of TGC could give extremely important information information during high luminosity runs.

Phase-2 DCS for TGC

Osamu Sasaki (KEK)

01/10/2018

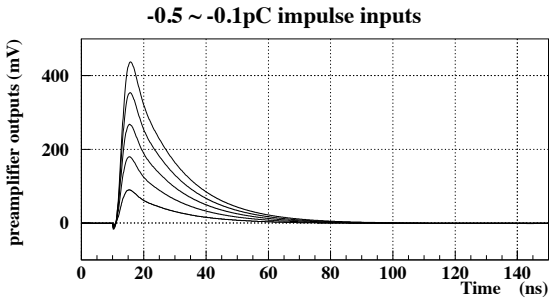
Current TGC DCS-PS board



- TGC DCS eLMB boards on all PS-Boards
  - DAC for Vth, LV/temp. monitoring (on board)
    - Implement on new PS-Boards, no DCS.
  - position sensors and temp. sensors of TGC's
    - No practical use in RUN1/2, to be removed.
- CCMC (Chamber Charge Monitor)
  - One analog output per TGC chamber (gap)
    - Lemo output from pre-amp. of the ASD board
    - No practical use in RUN1/2
  - If the CCMC function is really needed, We will attempt, in the future, a design for a new circuit to measure the lemo outputs of the BW TGC independent of the PS-board.

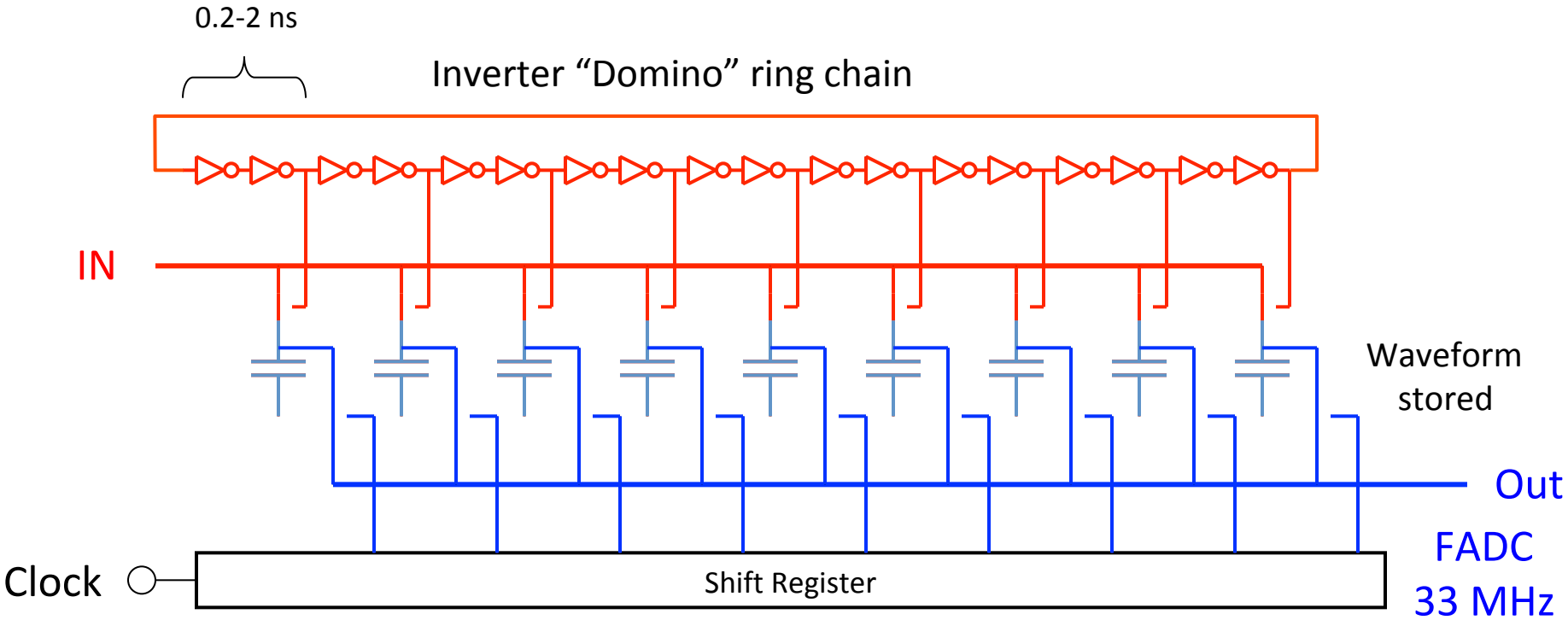
We are proposing to make TGC CHMonitor board, based on DRS4 chip.

Do we need TGC charge monitor?



- Time −over-threshold method needs information about base line of the amplifier at some intensity level.
- The gain measurement needs an information about pedestal.
- Inclusive spectra of pulses could give very important information (gamma, neutron rates, leakages and so on).
- Secondary pulses.
- Ideally we need an oscilloscope picture with 1 µS window and about 1 nS time step. I
- The dead time is not important for a monitoring board and we could minimize price of FPGA for this board.

Switched Capacitor Array

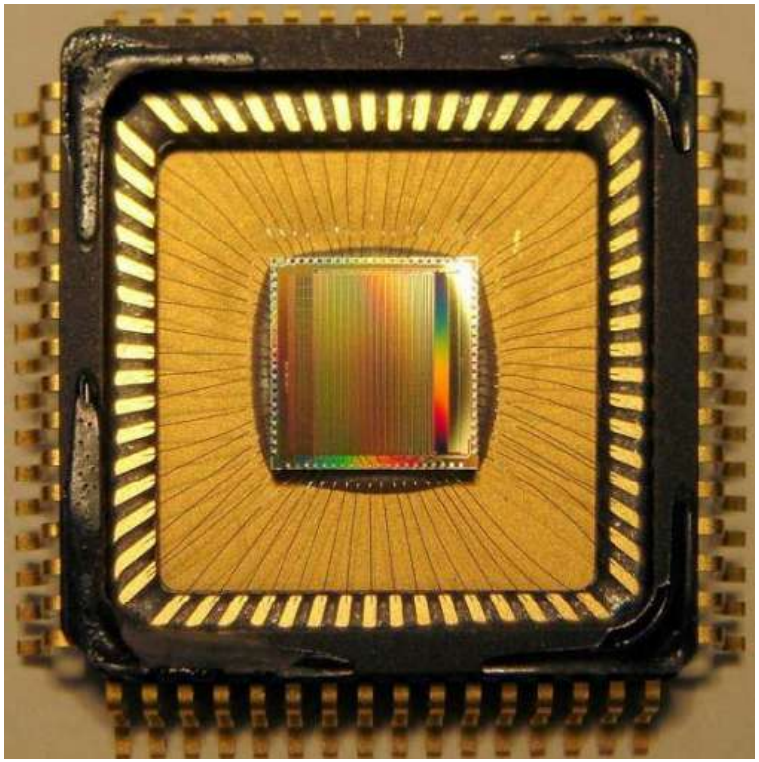


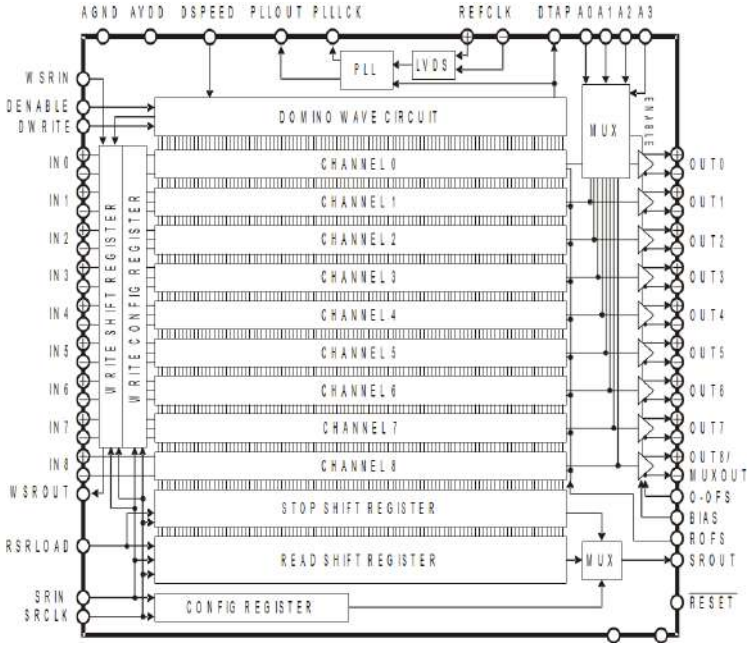
“Time stretcher” GHz → MHz

DRS4

DRS4 (Domino Ring Sampling) is a chip developed in PSI, Switzerland, it features:

- **A**pplication-**S**pecific **I**ntegrated **C**ircuit (ASIC)
- **S**witched **C**apacitor **A**rray (SCA) - fast analog buffer
- Analog sample rate up to 5 GS/s
- Analog bandwidth of 950 MHz
- 8+1 channels per chip
- Memory depth of 1024 cells per channel
- Time window of 200 ns at full sampling speed



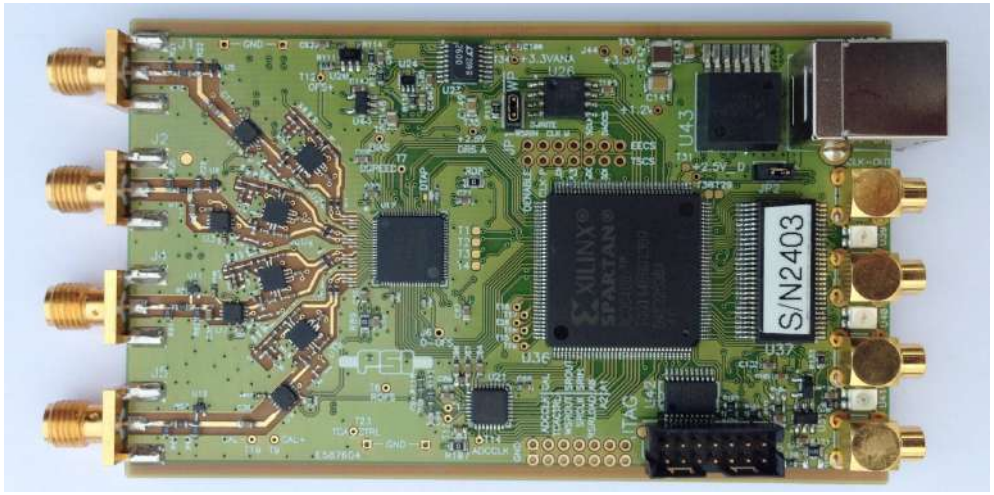


CAEN DRS based digitizers

- 16-32 channels per module
- VME, NIM and desktop versions
- USB, CAEN CONET (optical link) and VME64/VME64X readout
- 0.75-5 GS/s sampling rate
- 12 bit ADC
- Memory buffer for 128 or 1024 events
- Multi board synchronization available for VME modules
- Pricing starts at 6000 EUR for smallest memory option

DRS4 evaluation board

- 4 channels, USB powered, Plug and Play
- 750 MHz analog bandwidth
- Up to 5 GS/s sampling rate
- 14 bit ADC
- On-board DAC and oscillator for time and voltage calibration
- Possible to synchronize multiple boards (master/slave mode)
- Cost: around 1200 EUR - order of magnitude lower that scope with similar specs



https://www.psi.ch/drs/evaluation-board

https://www.psi.ch/drs/drs-chip

Quotations for the Detector Laboratory of UTFSM

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www.psi.ch

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Universidad Tecnica Federico Santa Maria
Attn: Rimsky Rojas
Avenida Espana 1680, Valparaiso
Chile.

Villigen PSI, September 17, 2018

Offer No. 2018/180

Dear Mr Rojas

We have the pleasure in quoting the following :

Item No.	Qty	Description	Price/pc		Total	
1	2	Evaluation Board DRS4 V5 Scientific Use Only	EUR	1'170.00	EUR	2'340.00
		Total			**EUR**	**2'340.00**

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Villigen PSI, September 17, 2018

Offer No. 2018/194

Dear Mr Rojas

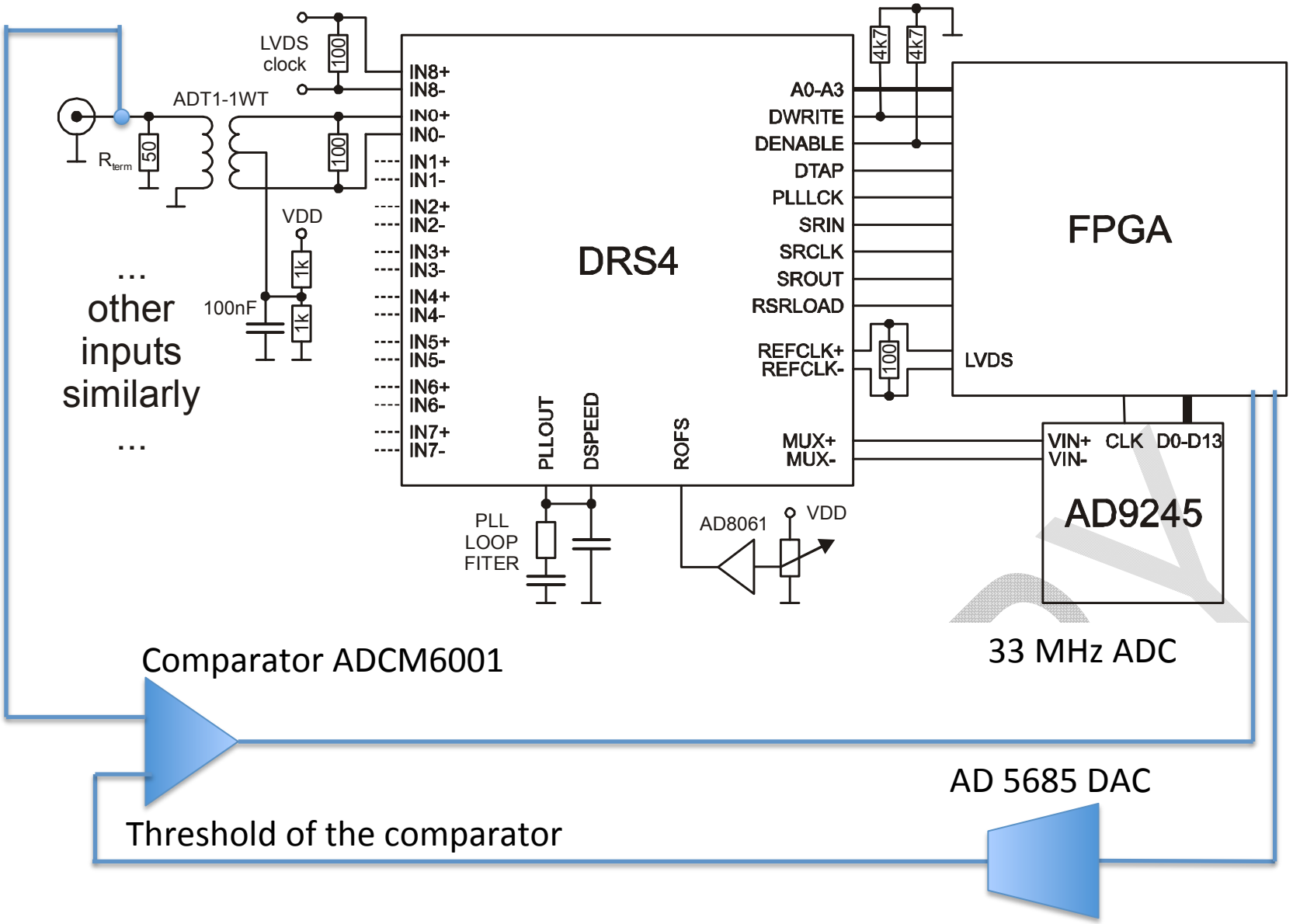
We have the pleasure in quoting the following :

Item No.	Qty	Description	Price/pc		Total	
1	80	Waveform Digitizing Chip (DRS4) 9 channel, 5 GSPS; Switched Capacitor Array Scientific Use Only	EUR	103.00	EUR	8'240.00
		Total			**EUR**	**8'240.00**

Prices for Waveform Digitizing Chip (DRS4) are as follows:

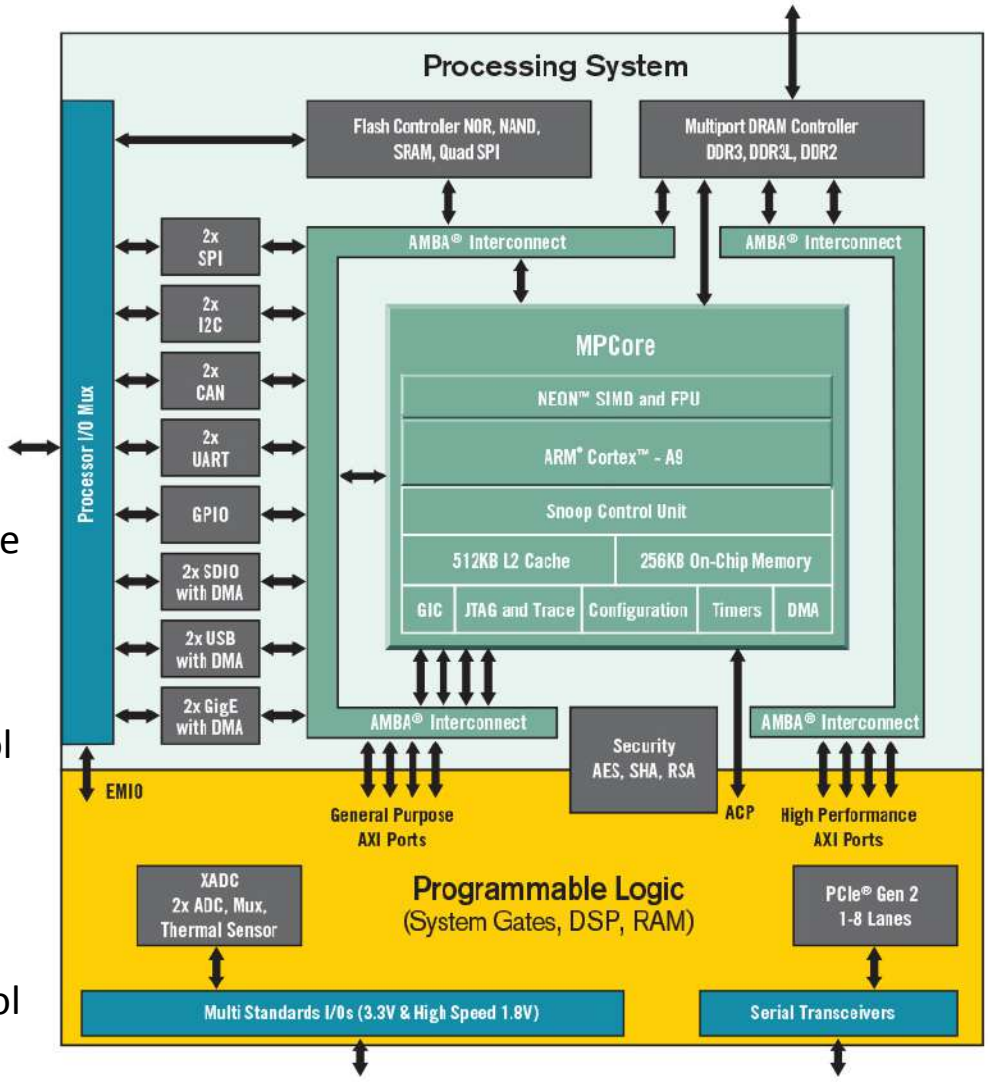
1 - 9	182	EUR/pc
10 - 99	103	EUR/pc
100 - 249	78	EUR/pc
250 - 999	60	EUR/pc
1000+	47	EUR/pc

Typical mode of operation of DRS4 + additional components for the monitor board .



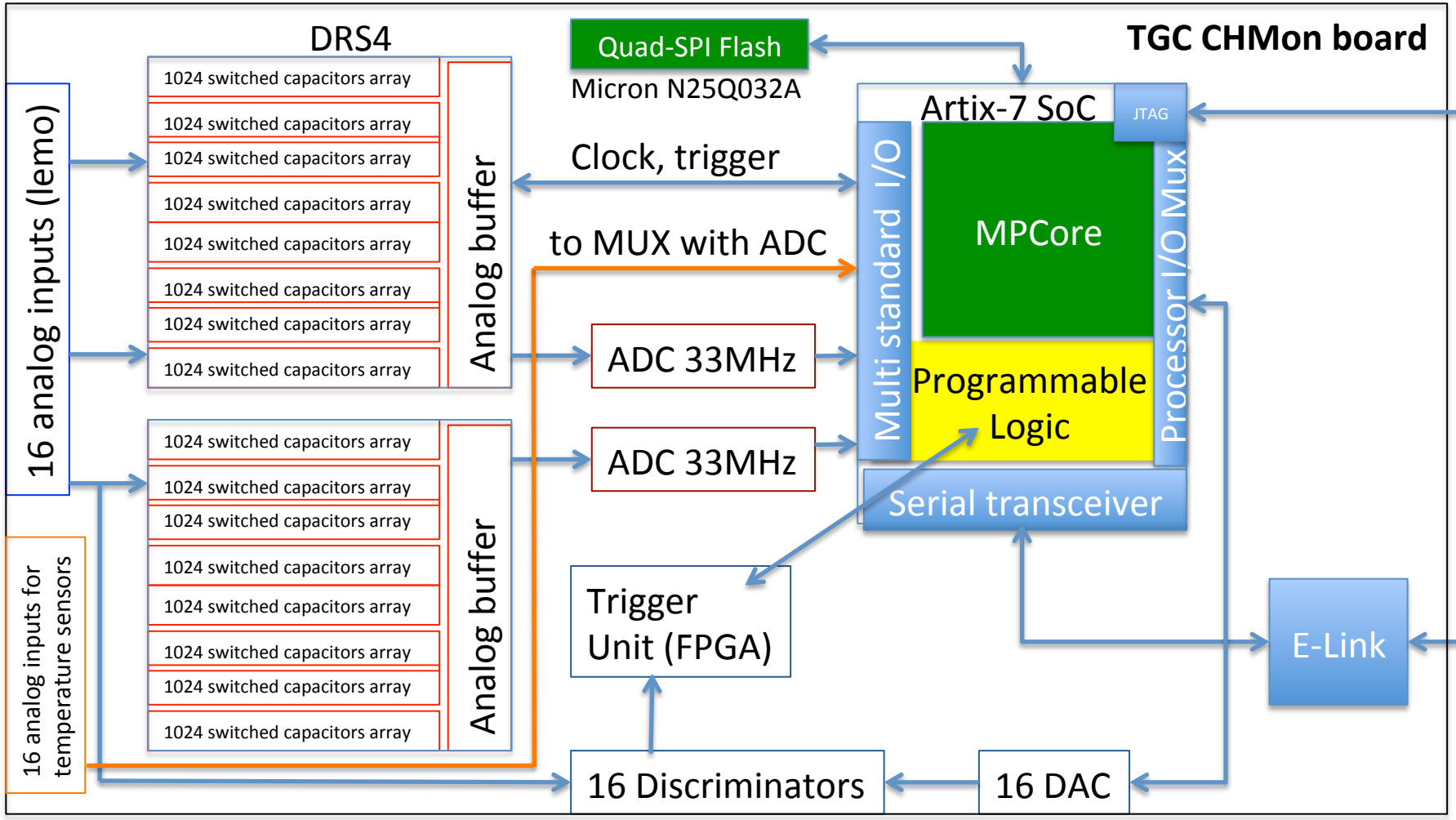
XILINX Zynq-700S SoC

- Zynq-7000S devices feature a single-core ARM Cortex™-A9 processor mated with 28nm Artix®-7 based programmable logic, representing the lowest cost entry point to the scalable Zynq-7000 platform.
- Programmable Logic (FPGA) will be used as: the trigger unit; the controller for 2 DRS4 chips; the controller for 2 external ADC (33 MHz); FIFO for the external ADC; serial transceivers for E-Link
- Internal Analog Multiplexer (16 ch.) and internal 12 bit ADC will be used for digitizing signals from external temperature sensors (16)
- The single-core ARM Cortex™-A9 processor will be used for TGC signal shape analysis and temperature sensors signal analysis
- 16 TGC signal shapes (oscilloscope pictures) will be stored and could be transferred to the Control Network via E-Link
- TGC pulse charge (or average value for a set of signals) will be sent to the Control Network via E-Link
- Temperature of sensors will be sent to the Control Network via E-Link.



TGC CHarge Monitor board and ELMB++

- The TGC CHMon board has E-Link communication.
- Since the FPGA's memory is volatile, it relies on the Quad-SPI flash memory to store the configuration between power cycles (https://reference.digilentinc.com/_media/cmod_a7/cmod_a7_rm.pdf).
- An initial programming goes trough JTAG before an installation on the detector. A modification could be done through E-Link.
- Processor part with Linux OS

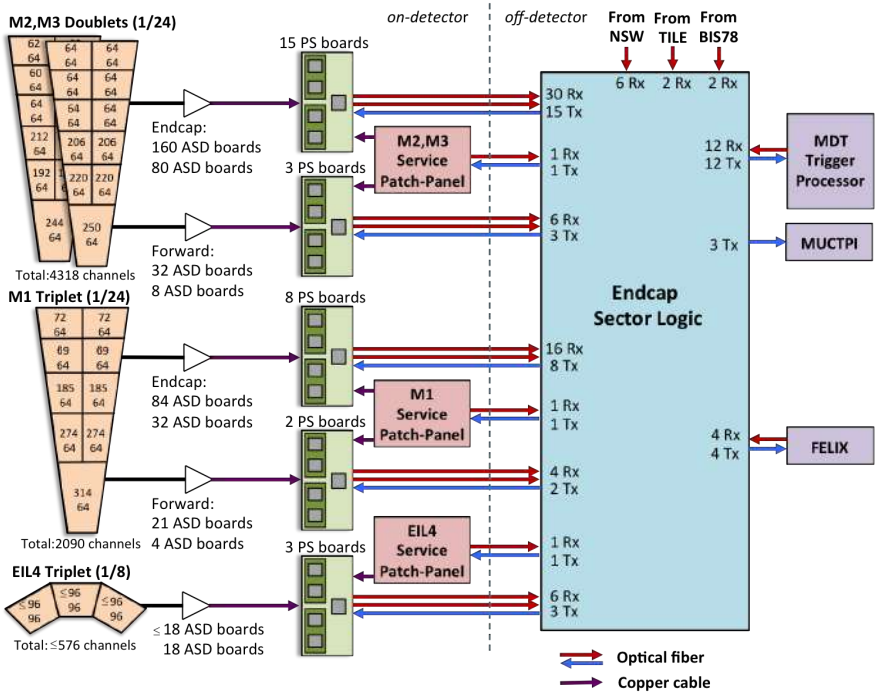


16 channels TGC Charge Monitor board

For the case of the 432 Triplets (1296 chambers), one unit of 15 inputs will serve 5 triplet, while the other (12 inputs) will serve 4 triplets. For the case of the the 1056 doublets (located on each side as 2 unseparated wheels of doublets), one could install such boxes, where 2 units will be serving 16 channels (8 doublets) and one serving 12 channels (6 doublets)

Since in both cases, the subdivision in the azimuthal angle is 24 and there are 2 sides, this gives the total number of boxes ((2+3)X24X2)=240 + optional 10 (2x2) for EIL4 Triplet

TGC System



Re-used

BW TGC's

23k ASD Boards

Cables from ASD boards to PS boards

New

EIL4 TGC

PS boards

SPP boards (auxiliary board to control/configure PS boards)

Patch-Panel ASIC's

5k optical fibres

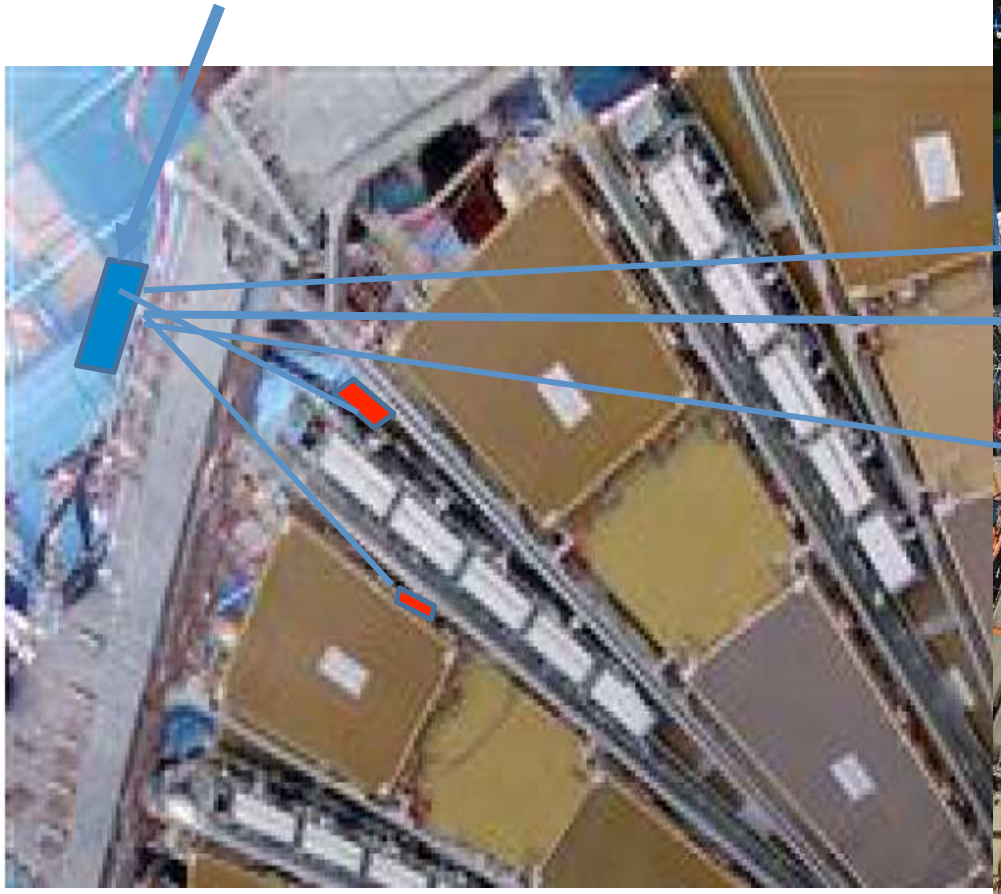
Sector Logic (TDAQ part)

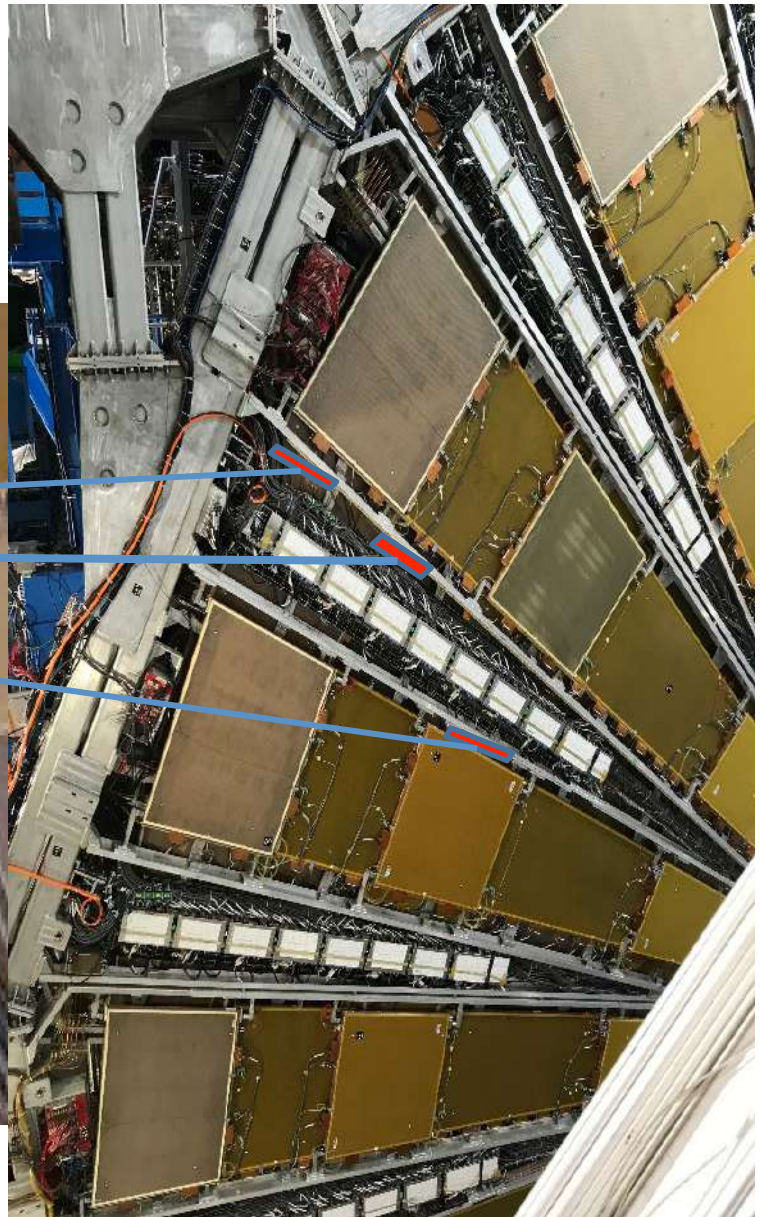
Charge Monitoring system for the ATLAS BW

- The new Charge Monitor system will use the already existing charge amplified signals reaching the present Service Patch Pannels (5 for triplets in TGC1 and 8.5 for the doublets in TGC2 and TGC3).
- For the above cases, in each of the 24 sectors of each side (A and C), 2 small Charge Monitor boxes (one serving 15 and another 12 channels) will be installed in TGC1 and 3 Charge Monitor boxes (2 serving 16 channels and one 12 channels) next to the Service Patch Panels.
- The output from the Charge monitor will be the sum of the charges for a coincidence of 2/3 inputs after subtracting the charge before the pulse.
- The Charge monitoring unit will also contain in the FPGA the possibility to communicate using the Elink protocol with the ELMB++Hub, as well as boot loader.
- 12 ELMB++Hubs will communicate with an ELMB++ receivers in USA (therefore 4 such receivers are needed).

Position of Charge Monitor in TGC1 and TGC3

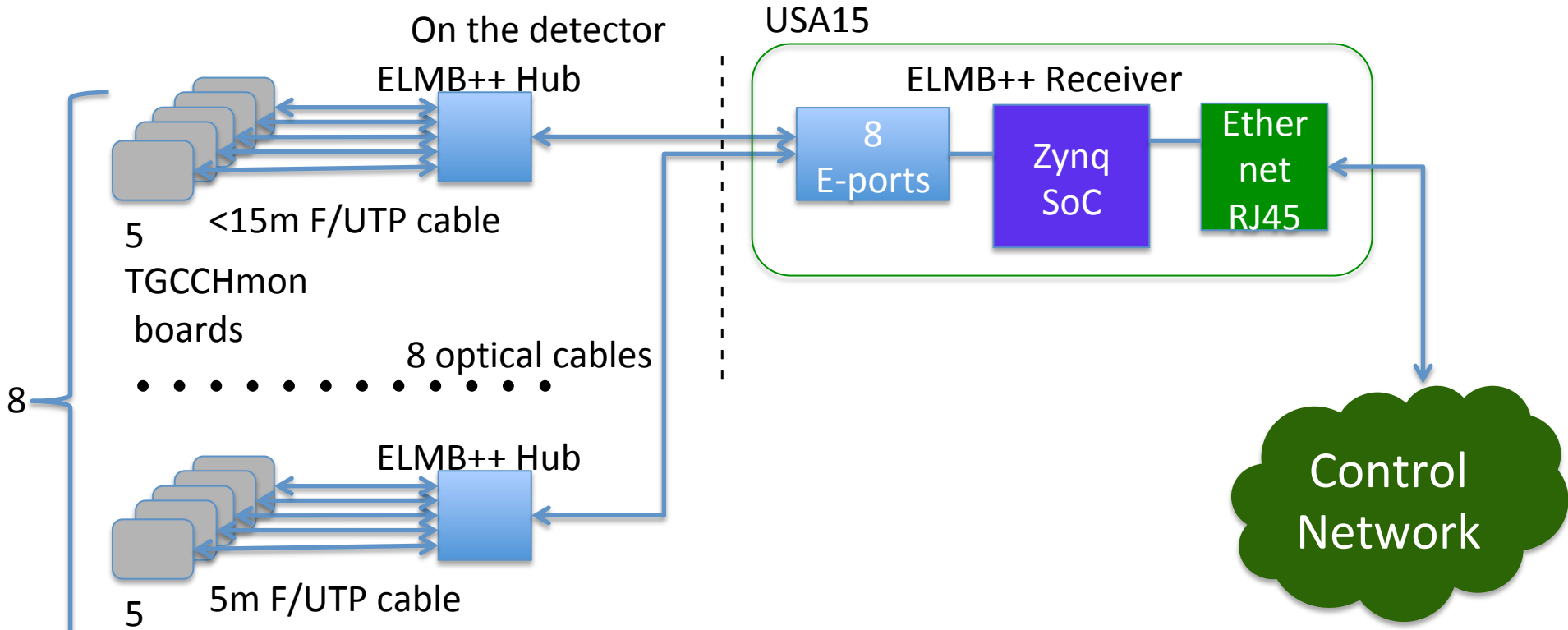
ELMB++ hub (input lines <15m)





ELMB++ network with TGC CHMon boards

- TGC CHMon board will work via E-Link with the ELMB++ Hub
- E-Link cables from TGC CHMon. to ELMB++ Hub is about 15 m or less
- 5 TGC CHMon boards are joined with 1 ELMB++ hub via E-Link cable
- 8 ELMB++ hubs are connected via optical cable to 1 ELMB++ Receiver in USA15



24 hubs and 4 receivers per Wheel (1 hub for EIL4 is optional)
Total: 48 hubs (+2 for EIL4) and 8 receivers
Cables: 244 15 m F/UTP cables and 8 ??? m optical cables

The project budget.

- 20 pre-production TGC CHMon boards + 244 TGC CHMon boards = 314.4K CHF
- 48 ELMB++ Hubs= 48 x 500 CHF=24K CHF
- 8 ELMB++ Receivers= 8 x 2K CHF=16K CHF

Total: 354.4K CHF

Conclusions:

- The Chilean Cluster is creating a team for participation in Phase II upgrade inviting electronic engineers and scientists from UNAB, PUC (Santiago), UTFSM. This part of the Chilean Cluster is not involved in the NSW project. UNAB will create a team of technicians for work on NSW assembling and installation, the same team will participate in installation of equipment for Phase II later.
- Proposed TGC charge monitor could be used for TGC gain control and for analysis of base line, pulse shape and TGC pulses spectrum. It could be very useful for work at high luminosity.
- This monitor could be used for temperature control of each TGC as well.