



## VMM3a for GEM readout status Vitalii Burtsev on behalf of BM@N collaboration 4th Collaboration Meeting of the BM@N Experiment at the NICA Facility

14 October 2019

#### VMM3(a) pinout



Figure 7: VMM3a pinout (top view)

### VMM Architecture and highlights



- Peaktime (200, 100, 50, 25 ns)
- Gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)
- Neighbor logic
- Both input charge polarity

- TAC slope adjustment (60, 100, 350, 650 ns)
- Low power 10mW/ch
  - 64 input ch/ASIC

### Viking and VMM3a chip comparsion

	VMM3a	VA162	VA163
Input channels	64	32	32
Input charge	-2 to 2 pC	-1.5 pC to +1.5 pC	-750fC to +750 fC
Shaping time	25 to 200 ns	2 to 2.5 us	500 us
Noise	500e ENC at 25pF	2000e ENC at 50 pF	1797e ENC at 120pF
Gain	0.5 to 16 mv/fC	0.5 uA/fC	0.88 uA/fC
Total power max	640mW	66mW	77mW

#### VMM3a time resolution



#### VMM3 based CSC readout



#### **VERSO GUI**

	VERSO - v4.4.0	×
Run Status     Start Run       Run #     0 ≑       ✓ Write Ntuple     Write Raw       VMM2     VMM3       L0 R/O     DataFlow	Setup Config Output /home/azzz/Downloads/20180723_testConfig_board103_cosmic_tailCancellation.xml	2 ine 15 EN
$\begin{tabular}{ c c c c c } \hline Counters & 0 & Clear & \\ \hline Triggers & 0 & Clear & \\ \hline Tree Flush & -1 & No Config & \\ \hline Tree Flush & -1 & No Config & \\ \hline \hline Tree Flush & -1 & No Config & \\ \hline \hline Tree Flush & -1 & No Config & \\ \hline \hline Tree Flush & 0 & 2 & \# FEBS 1 & \\ \hline \hline Comfigure & \\ \hline \hline FEB Select & All & \hline & Configure & \\ \hline VMM & \textcircled{O} & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 \\ \hline Select & \textcircled{O} & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 \\ \hline \hline Trigger & Mode & Acquisition & \\ \hline Latency & x62ss & External & \\ \hline B & & & & & & & \\ \hline Red & & & & & & & \\ \hline Set & & & & & & & & \\ \hline & & & & & & & & & \\ \hline & & & &$	Messages         Global Registers 1         Global Registers 2         Channel Registers         Calibration         Set IP           Message Reportin         Maiting for open communication with FEB         Setting configuration file to: /home/azzz/Downloads/20180723_testConfig_board103_cosmic_tailCancellation.xml         Setting configuration file to: /home/azzz/Downloads/20180723_testConfig_board103_cosmic_tailCancellation.xml           VERS0         Info         SocketHandler::loadIPList         SocketHandler::loadIPList         > 192.168.0.2           VERS0         Info         SocketHandler::enddSocket         VMMSocket::Print         Name         : FEC           VMMSocket::Print         Sound to port : 6007         Status         : 4	
CKTK & X CKBC Freq. (M         7 ♦ 40 ♥         Defaults         CKTP         Number of Pulses to S:         -1 ♦         Skew (steps)         Period         0 ♦ × 1ns         30000 ♦ × 200ns         Width         4 ♦ × 500ns         Defaults         Defaults         Set         Monitor Sampling       50 ♀         Incidence Angle       0 ♦	Bottom Verbose FEC Response Clear	

#### **Global registers**

	VERSO - v4.4.0 _ ×
Run Status     Start Run       Run #     0 ÷       ✓ Write Ntuple     Write Raw       VMM2     VMM3       L0 R/O     DataFlow	Setup  Config thome/azzz/Downloads/20180723_testConfig_board103_cosmic_tailCancellation.xml
Counters Triggers 0 Event Stop -1 Tree Flush -1 No Config	Messages       Global Registers 1       Global Registers 2       Channel Registers       Calibration       Set IP         Global Configuration Registers       Test Pulse DAC [sdp10]       0       Ch. Polarity [sp]       Positive       Ch. Gain [sg]       3.0 mV/fC       Peak Time [st]       200 ns       Image: Ch.
Communication         All Boards Alive           IPv4 192 168         0         2         # FEBs 1         ≠           Configure	Threshold DAC [sdt10] 380
Trigger         Mode         Acquisition           Latency         Pulser         ACQ On           128 ♦ x6.25ns         External         ACQ Off           Bat ⊕ x6.25ns         External         External           Dead Time         65533: ♦ x8ns         Set           6 ↓ ₱ 24 ♦         Set         Set	ADC Enable 6-bit mode [s6b] Disabled • 8-bit mode [s8b] Disabled • Hi. Res. (10-bit/8-bit) [s10b] Enabled • Direct Timing Output Enable [sttt] Disabled • Mode TtP (Thresh-to-P • [stop 0 • [stot] 0 •
CKTK & CKBC         CKTK Max       CKBC Freq. (M $7 \Rightarrow 40 \twoheadrightarrow$ Defaults         CKTP         Number of Pulses to S <sup>1</sup> -1 $\Rightarrow$ Skew (steps)       Period $0 \Rightarrow 1 \text{ ns}$ 30000 $\Rightarrow 1 \text{ solution}$ Width $4 \Rightarrow x 500 \text{ ns}$ Defaults	Address in Real Time (ART) Enable ART [sta] Enabled   Detect Mode [stam] Timing at Threshold   ADC Conversion 10-bit time [sc10b] 200 ns   B-bit time [sc8b] 100 ns   G-bit time [sc6b] Low   Dual Clocks Enable
Defaults     Set       Monitor Sampling     50 \$\overline\$       Incidence Angle     0 \$\overline\$	Data [sdcks]     Disabled     ART [sdcka]     Disabled     6-bit [sdck6b]     Disabled     Image: matching state st

FPGA Reset

VMM Hard Reset

#### **Global registers**

	VERSO - v4.4.0 _ ×
Run Status     Start Run       Run #     0 +       ✓ Write Ntupk     Write Raw       ✓ Write Ntupk     Write Raw       ✓ WM2     VMM3       L0 R/O     DataFlow	Setup       Image:
Counters Triggers 0 Hits 0 Event Stop -1	Messages         Global Registers 1         Global Registers 2         Channel Registers         Calibration         Set IP           Global Configuration Registers
Communication pen Communicatio	Direct Out I/Os [stvs]       Disabled <ul> <li>ART flag sync. [ssart]</li> <li>Disabled</li> <li>Skip Channels 16-47 [s32]</li> <li>Disabled</li> </ul> Tail cancellation [sttc]       Enabled          Fast recovery [srec]       Disabled          Bipolar shape [sbip]       Disabled            Auto-reset [stcr]       Disabled          Reset at 6b compl. [strst]       Disabled          Time ramp at thresh. [srat]       Disabled
IPv4 192 168 0 2 # FEBs 1 ≑           Configure           FEB Select All ▼         Configure           VMM         1 2 3 4 5 6 7 8	100 Ohm SLVS Termination On CKBC [slvsbc] Disabled  On CKTP [slvstp] Disabled  On CKTK [slvstk] Disabled  On CKDT [slvsdt] Disabled
Select Mode Acquisition Latency Pulser ACQ On Latency External ACQ Off Lat Extra CKBC	On CKART [sivsart] Disabled * On CKTKI [sivstki] Disabled * On CKENA [sivsena] Disabled * On CKeb [sivseb] Disabled *         L0         L0 core [sL0ena]         Disabled (Reset) * Mixed signals in L0 [sL0enaV]         Disabled * L0 BC offset [looffset] (0-4095)
88         ♦)         x6.25ns         Fixed Window           Dead Time         6553E         ♦)         x8ns           # CKBC ART I/O         6         ₽         24         ₽	Ch. tagging BC offset [offset (0-4095) 0 Ch. tagging BC rollover [roll (0-4095) 4095 Trig, window size [window] (0-7) 7 Max hits per L0 [truncate] (0-63) 63 + L0 to skip on overflow [nskip] (0-127) 0 Clocks w/ L0 disabled [sL0cktest] Disabled •
CKTK & CKBC CKTK Max CKBC Freq. (M 7	Invert BCCLK [sL0ckinv] Disabled • Invert DCK [sL0dckinv] Disabled • BCID skip [nskipm] Disabled •
Number of Pulses to S         -1 ⊕           Skew (steps)         Period           0 ⊕ x 1ns         30000 ⊕ x 200ns           Width         4 ⊕ x 500ns         Defaults           Defaults         Set	Hard Reset [reset]     Disabled
Monitor Sampling         50 ⊕           Incidence Angle         0 ⊕           EPGA Reset         VMM Hard Reset	

### Triggger and MO signal



# Kintex7 based 128ch GEM evaluation board



## THANK YOU FOR YOUR ATTENTION

ENC at 200ns



#### ENC with 200pF is ~2.1ke, 25pF is ~500e





#### ENC with 220pF and 50ns is ~4.5keand for 100pF is 2.8ke 4th Collaboration Meeting of the BM@N Experiment at the NICA Facility

## The analog pedestal distribution versus the channel

