

BMN & MPD Data Acquisition in 2018

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BMN & MPD DAQ Collaboration

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The first Collaboration meeting of the MPD and BM@N
experiments at the NICA Facility

Outline

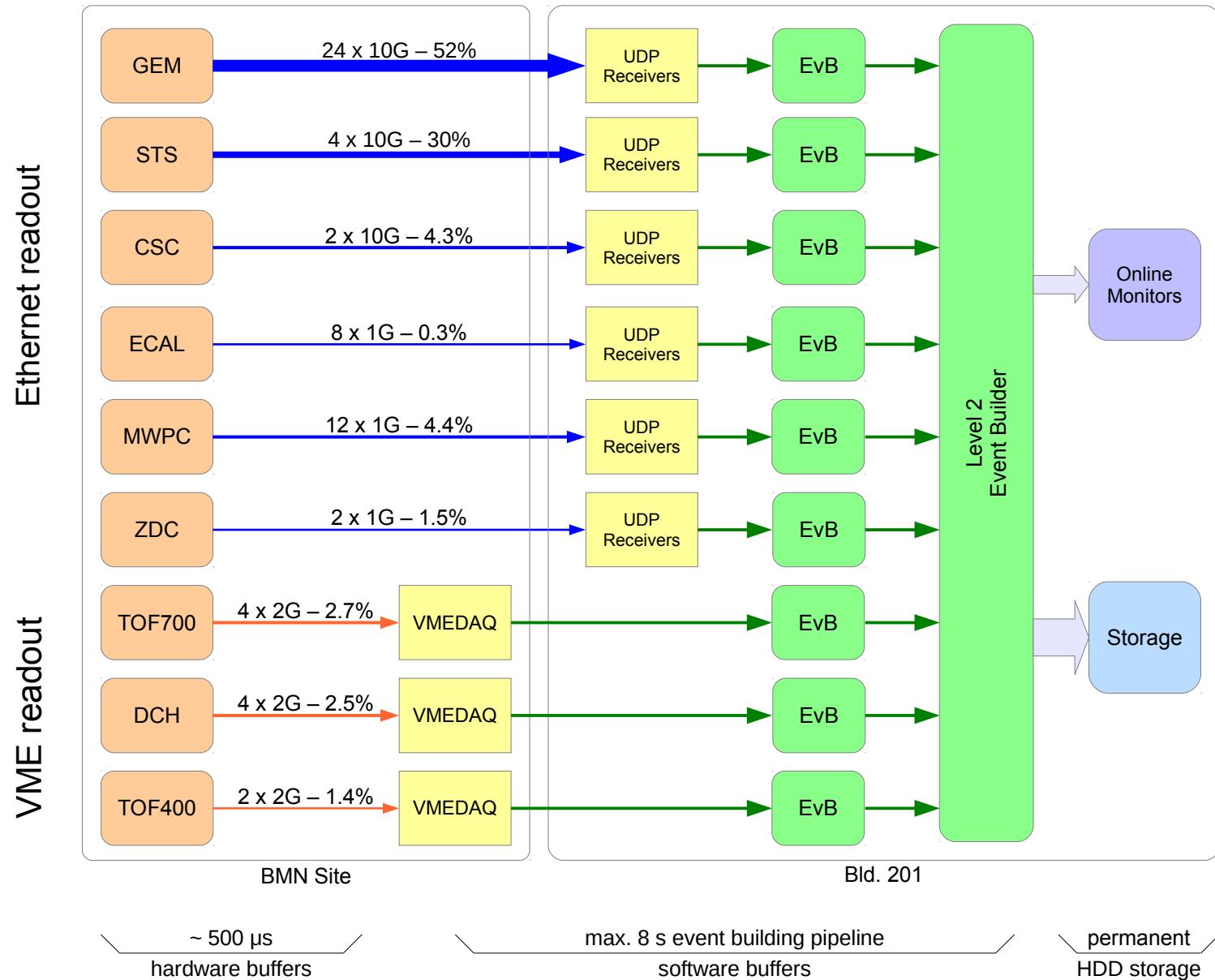
- ▶ DAQ parameters
- ▶ DAQ performance in 2018 BMN Run
- ▶ Time Synchronization and Run Control
- ▶ Readout Electronics
- ▶ Data transfer, processing, storage
- ▶ IT Infrastructure

* *More details in MPD DAQ TDR*

BMN DAQ parameters

| | March 2017 | Mar–Apr 2018 | 2020 – 2021 |
|----------------------------------|--------------------|-------------------------|---------------|
| Raw event size, Bytes | 120 000 | 225 000 | ~ 300 000 |
| Trigger rate | 5k | 10k | 20k / 50k |
| Before / After Protection | none | 3 μ s / 0.5 μ s | |
| DAQ missed triggers | > 50 % | < 15% | |
| GEM / STS / CSC zero suppression | none (Off-line) | none (Off-line) | On-line |
| Event readout time | 100 – 300 μ s | 35 μ s | 15 μ s |
| Total raw data volume | 7.6 TiB | 66.4 TiB | 150 – 500 TiB |
| DAQ FLP network bandwidth | 20 Gb/s | 90 Gb/s | 800 Gb/s |

BMN DAQ setup in March 2018



Readout and Control Electronics

| Detector | DAQ Function | Readout card | Standard | Readout |
|---------------------------------|--|--------------------------|-----------------|------------------------|
| BMN GEM, CSC, STS (prototype) | Charge, 32 or 128 channel multiplexed readout + waveform digitizer | VME ADC64VE-10GE | VME64x | Ethernet 10G |
| BMN TOF-400, T0 — MPD TOF | Two-edge Pulse Timestamping | VXS TDC72VHE – 25 ps TDC | VXS | VME64 — Ethernet |
| BMN TOF-700 | Two-edge Pulse Timestamping | TDC64VHLE – 25 ps TDC | VXS | VME64 |
| BMN DCH | Pulse Timestamping | TDC64VL – 100 ps TDC | VME64x | VME64 |
| BMN ECal, ZDC — MPD ECal | Charge, waveform digitizer with DSP | ADC64S2 v5.0 | standalone | Ethernet |
| Time Synchronization | WR Time receiver, VME clock distribution | FVME2-TMWR | VXS | Ethernet |
| Control and Monitoring | UT24VE-RC | UT24VE-RC | VME64 | Ethernet |
| Interfaces | VME control and readout | FVME2, PEXML-4 | VME64, PCIe | PCI-Express |

DAQ Electronics – made in Dubna



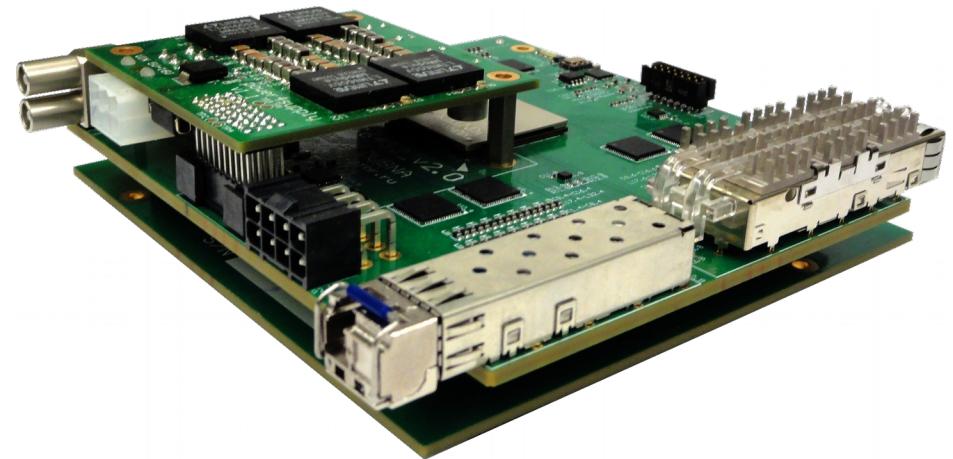
Timestamping TDC – TOF, FFD, T0



PCI-Express Fiber-optical Interface



Trigger Distribution and Control



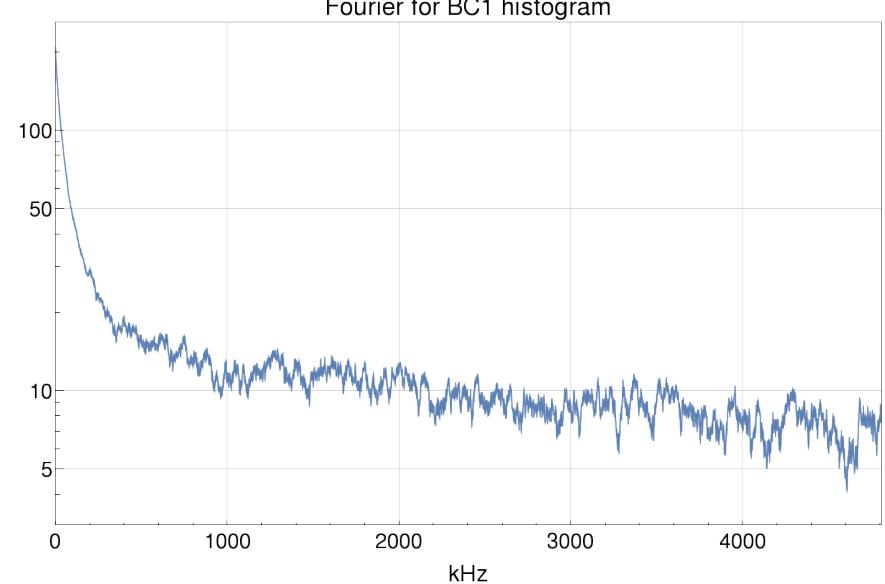
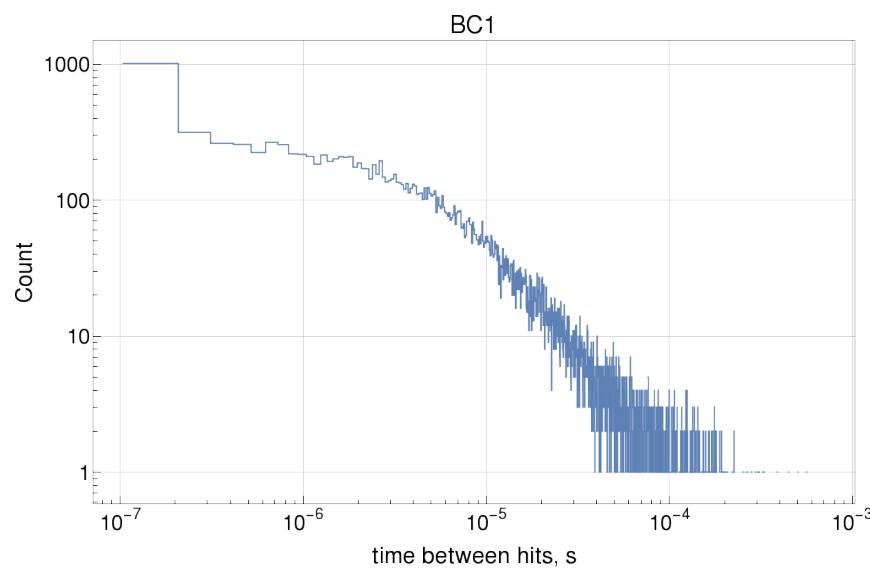
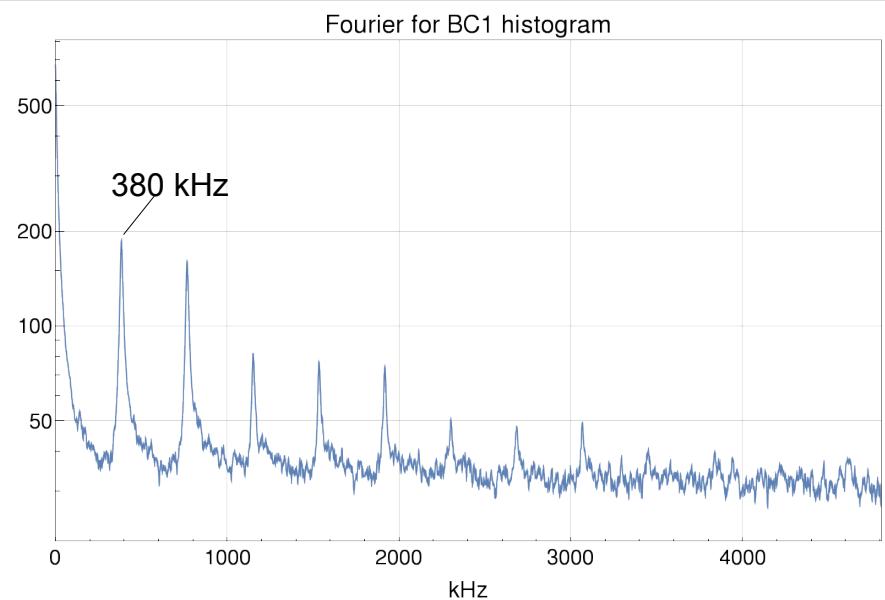
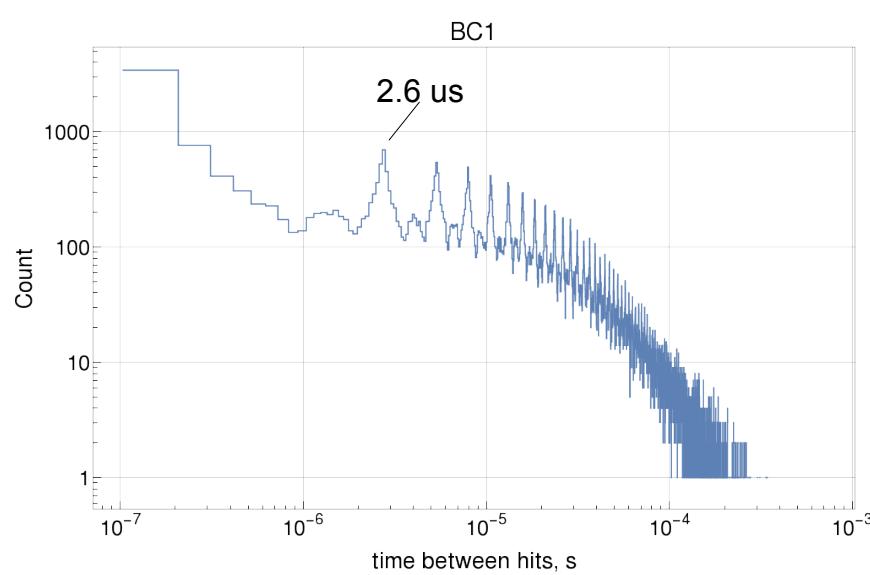
Waveform Digitizer – ECal, ZDC

DAQ Performance in BMN run 2018

- ▶ Improvement in extracted beam structure since 2017 BMN run. Trigger Time Interval Histograms.
- ▶ DAQ channel occupancy, ~ 100 runs processed
- ▶ DAQ event readout (busy) time
- ▶ DAQ efficiency

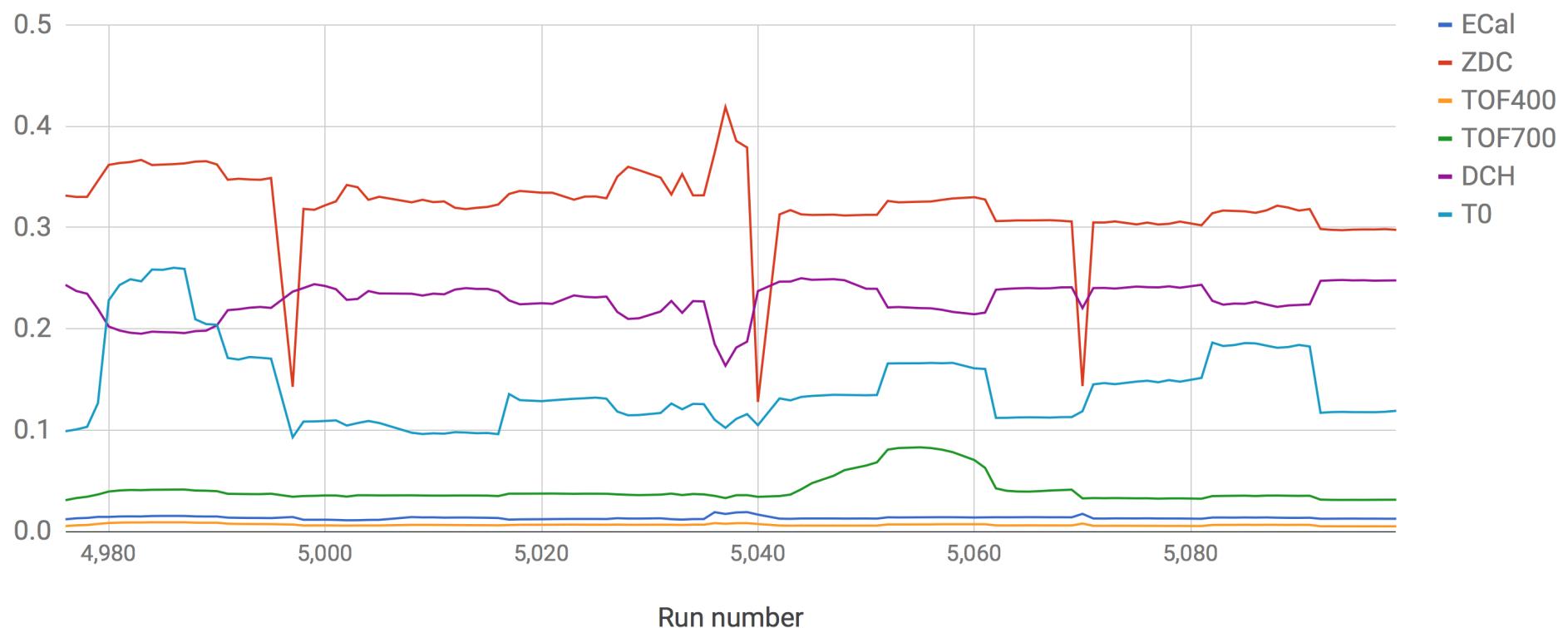
BMN BC1 Time Interval Distribution

measured by MSC16VE hardware histogrammer



BMN – Kr run, DAQ channel occupancy

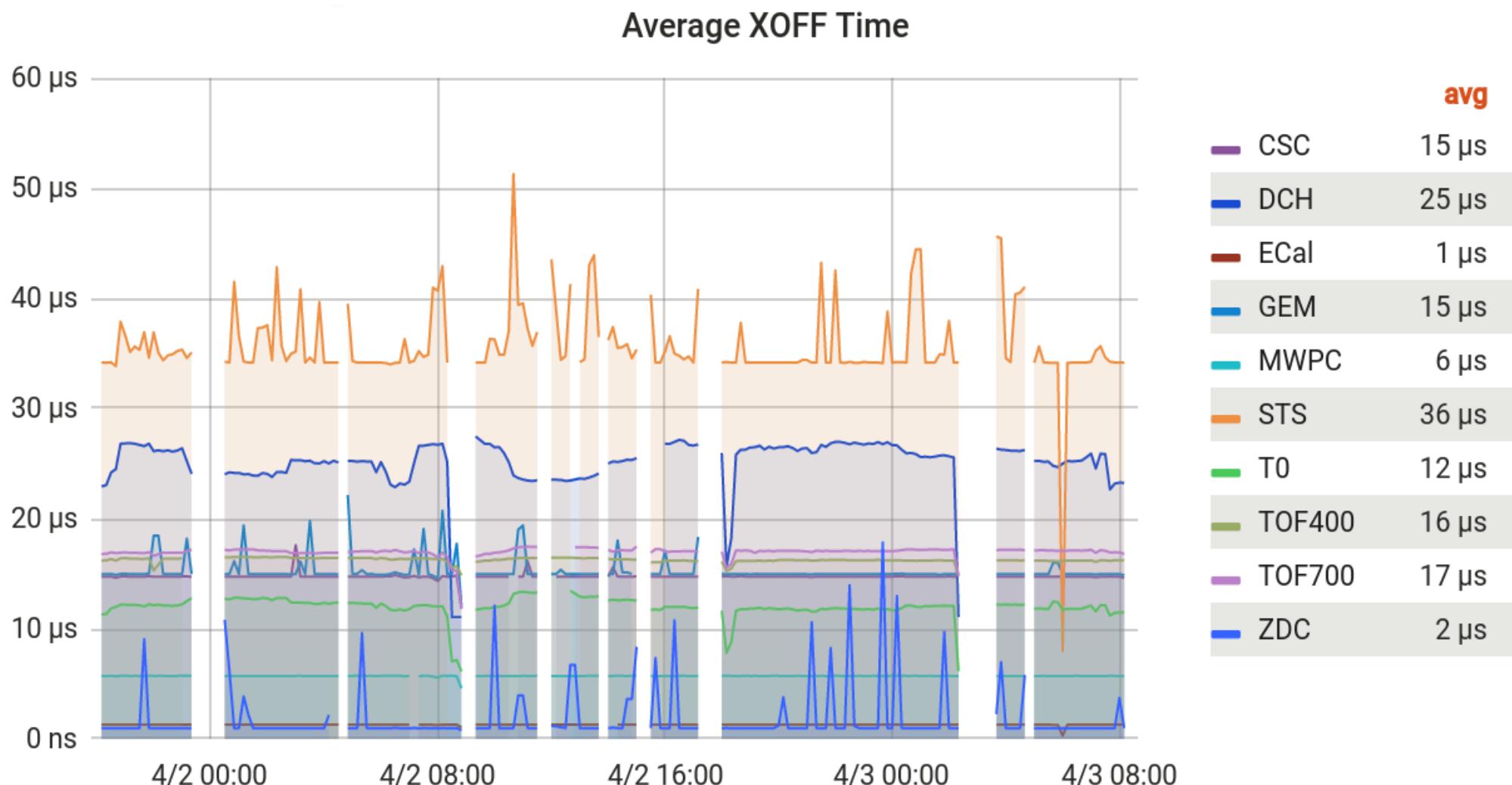
Average Occupancy in Detectors, Krypton run



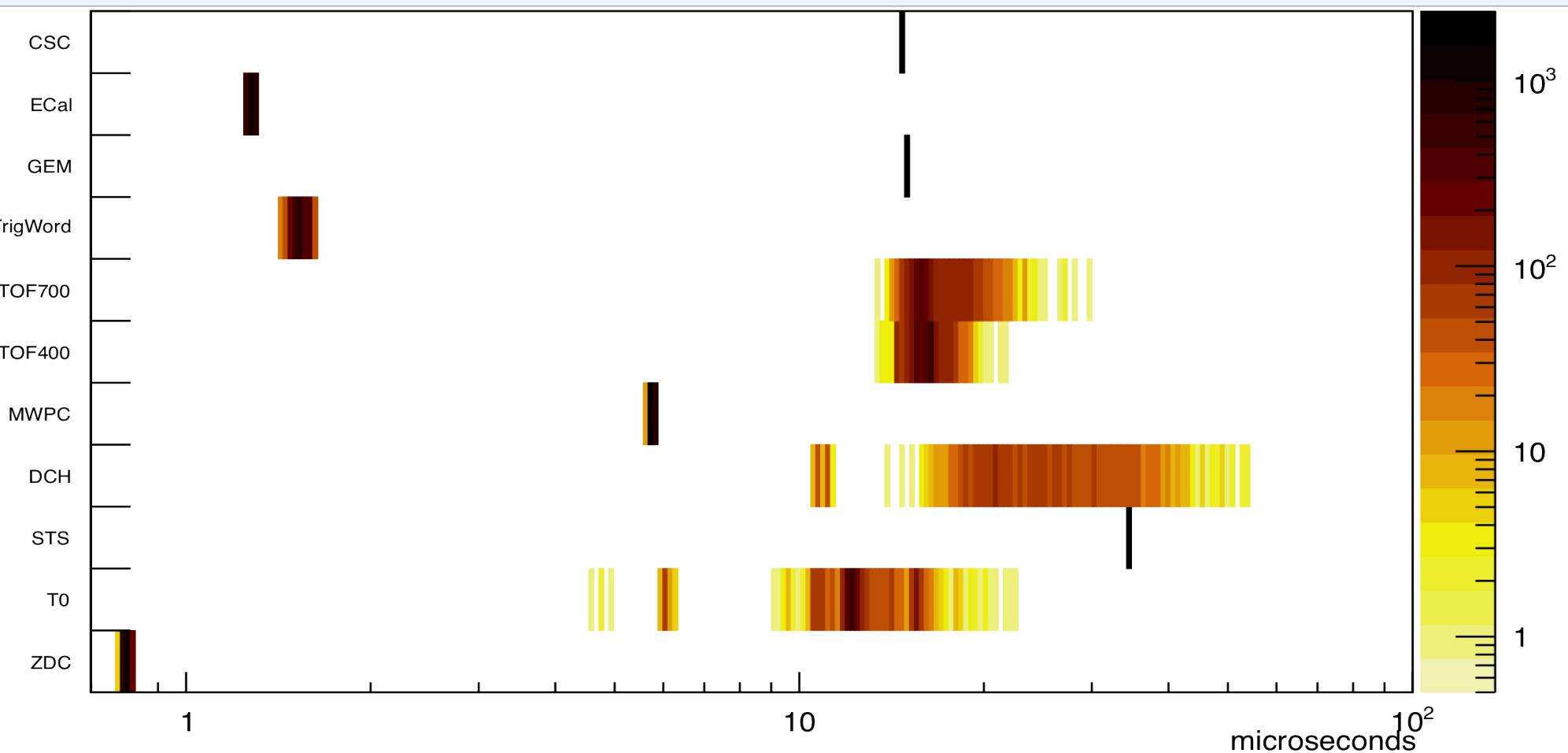
* GEM, STS, CSC – no hardware zero suppression, occupancy 100%

* Data from RAW file analysis

BMN – Kr run, DAQ busy time

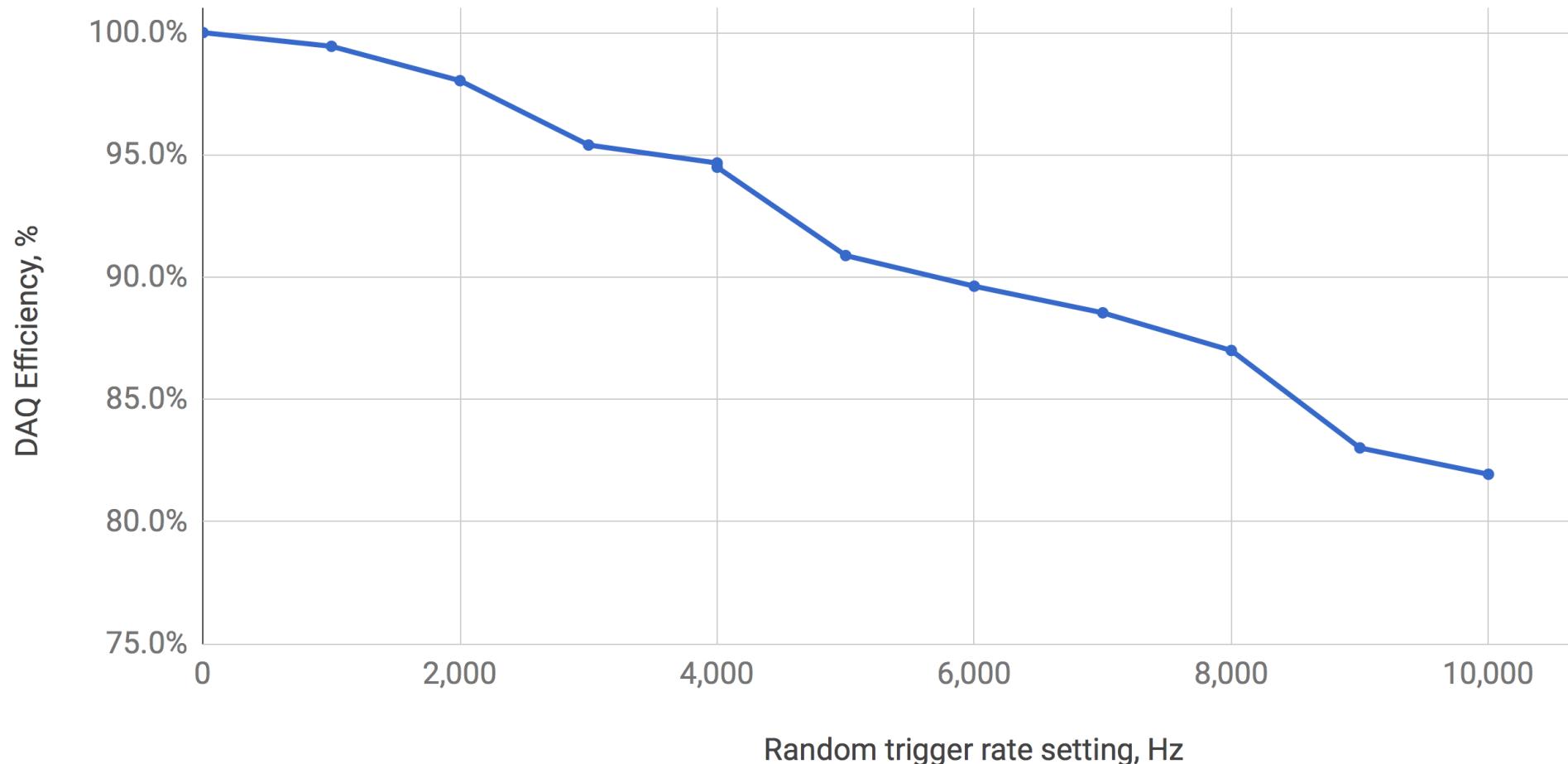


BMN – Kr run, DAQ busy time



- * STS – 35 μ s all channels multiplexed readout at max speed, ASIC limitation
- * CSC, GEM – 16 μ s multiplexed readout
- * DCH, TOF400, TOF700, T0 – enabled HPTDC debug headers / trailers, readout is not pipelined (implementation is planned)
- * MWPC – zero suppression may be implemented in hardware (if necessary)

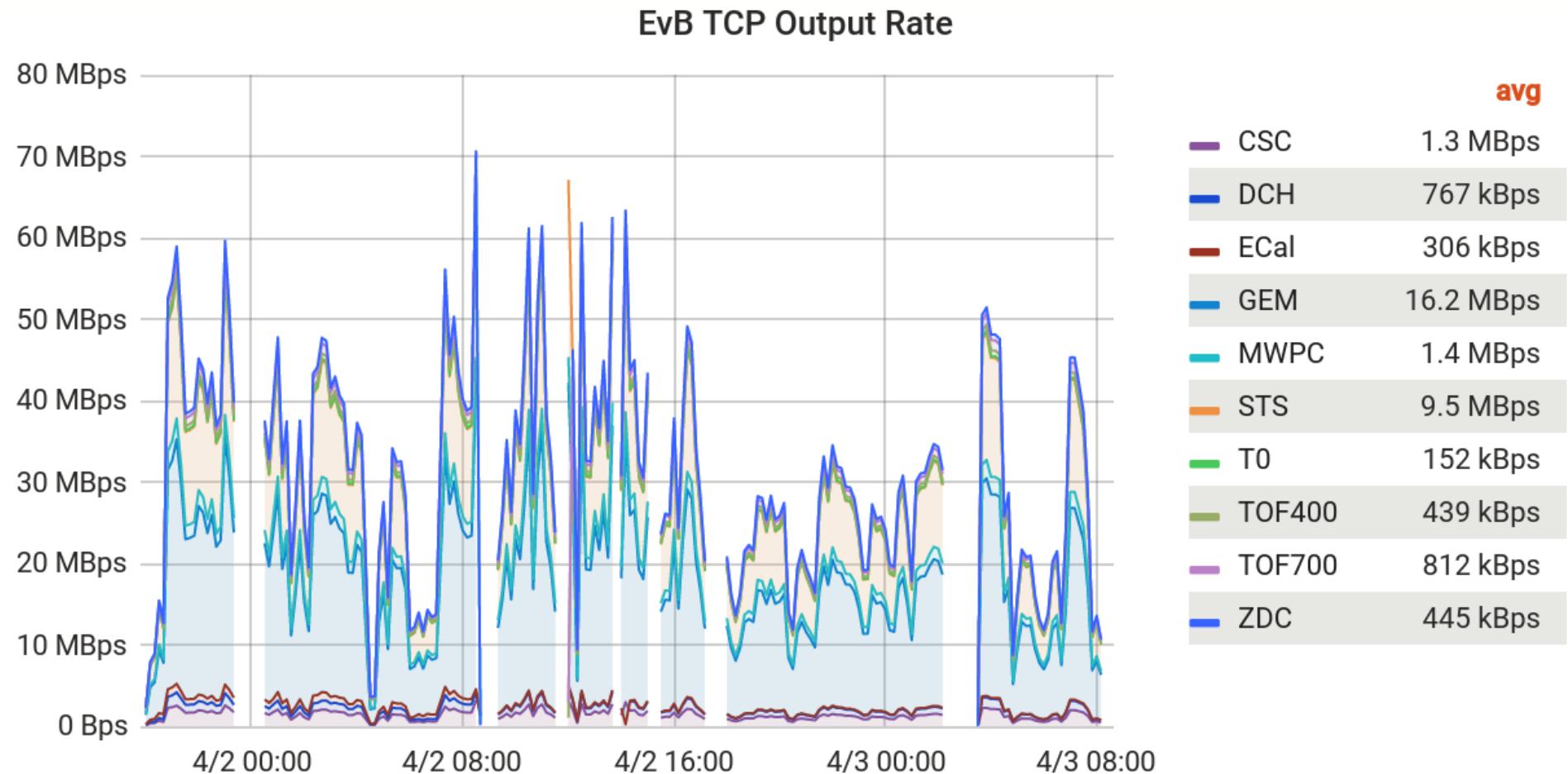
DAQ Efficiency (accepted triggers)



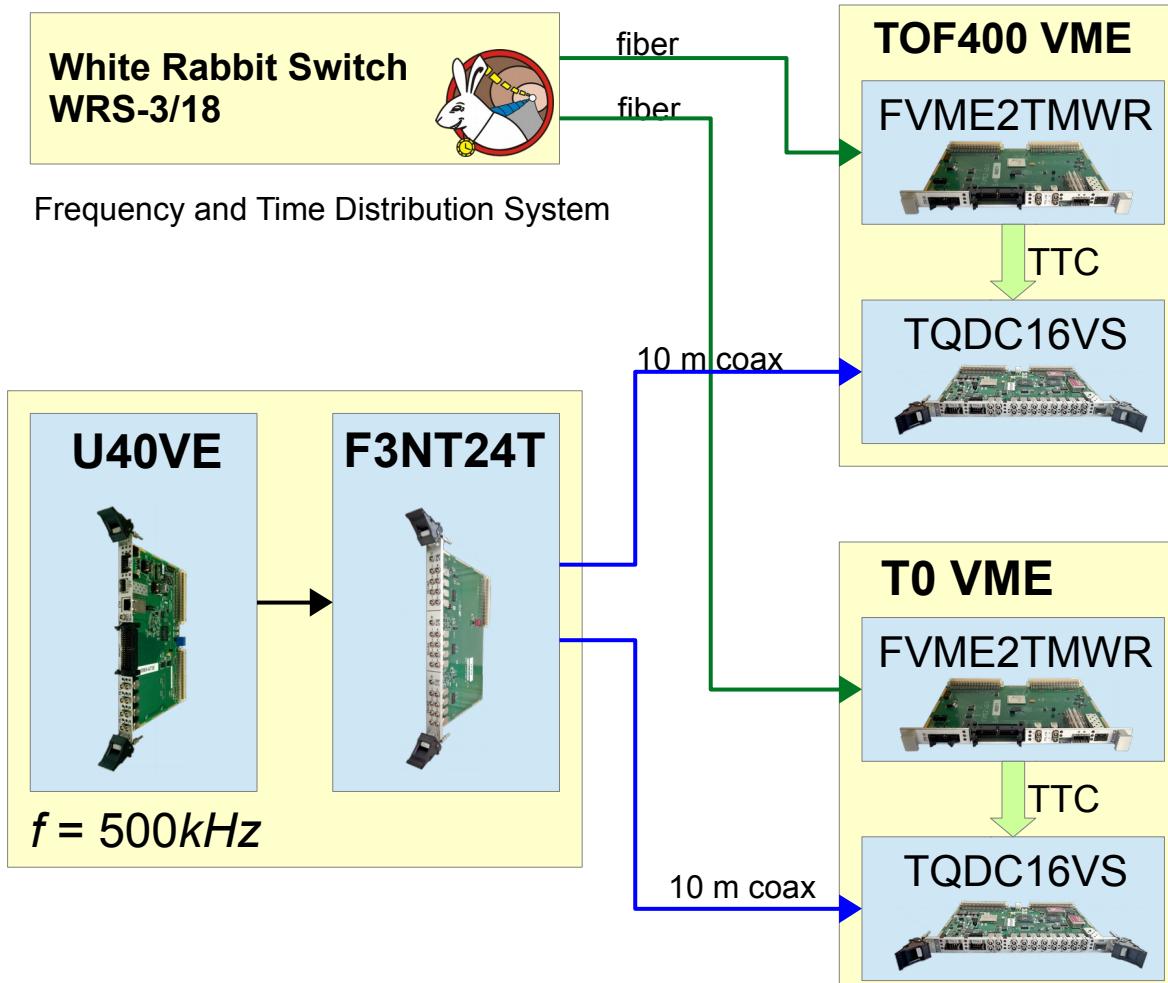
- * Trigger source: UT24VE-RC Random Trigger Generator
- * All detectors enabled
- * No beam, dummy data

- Not 100% efficiency due to trigger throttling
 - * sub-optimal, lossy network (packet drops observed)
 - * insufficient STS readout bandwidth

BMN Kr run – data rate to storage

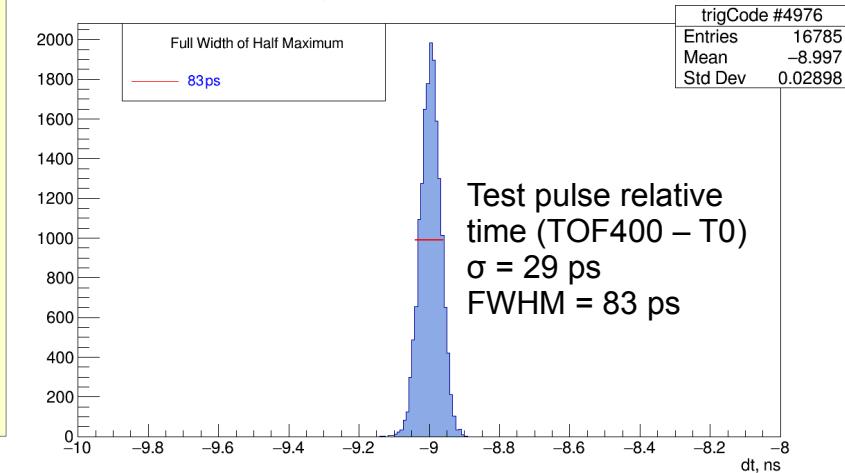


In-Run Time Synchronization Measurement

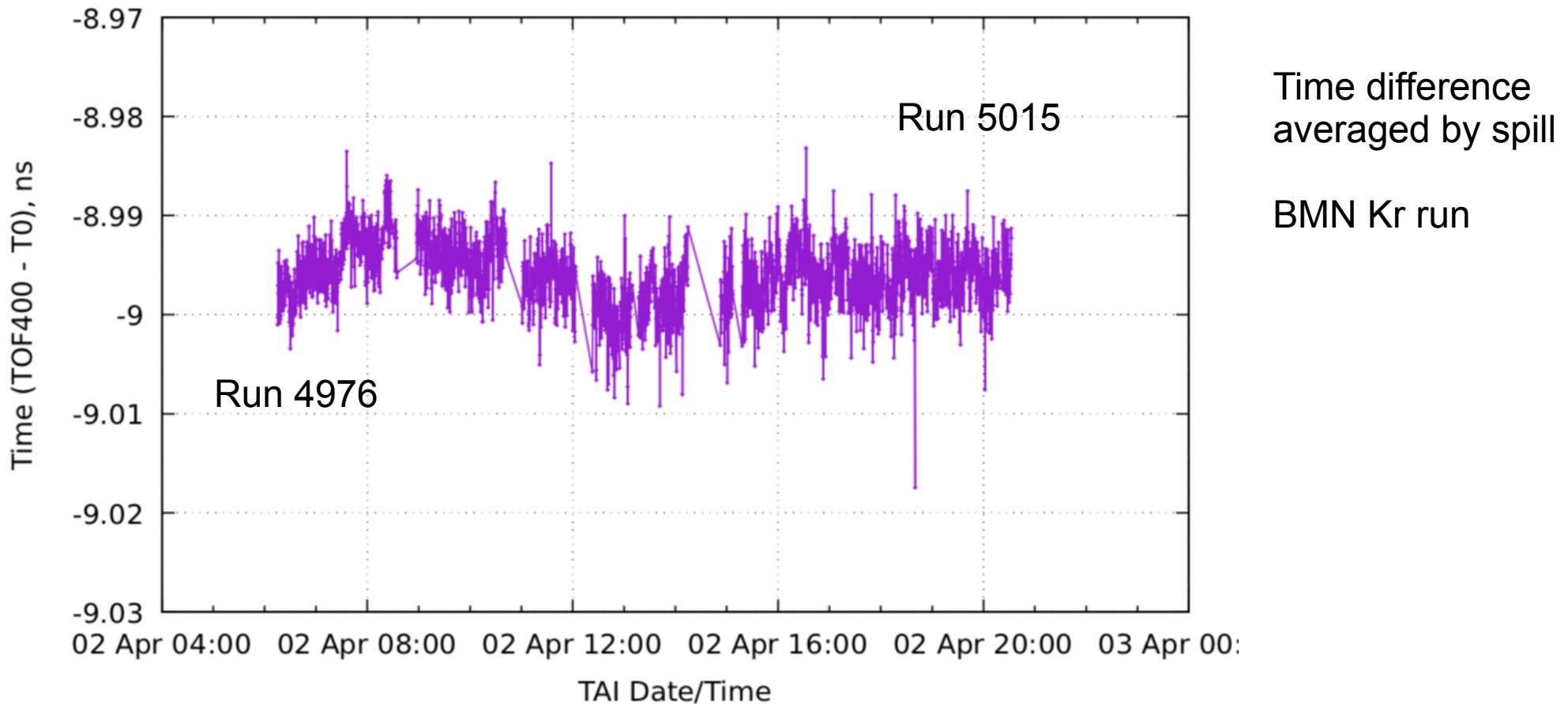


- 1) U40VE used as source of 500 kHz periodical TTL pulses
- 2) F3NT24T — 1-to-8 fanout
- 3) All FVME2TMWR modules sourced from same White Rabbit Switch
- 4) Match window for all TQDC16VS modules set to $2\text{ }\mu\text{s}$

Tof400_Ttl-T0_Ttl (TOF400-1 slot:21 ch:15 - T0 slot:13 ch:15)



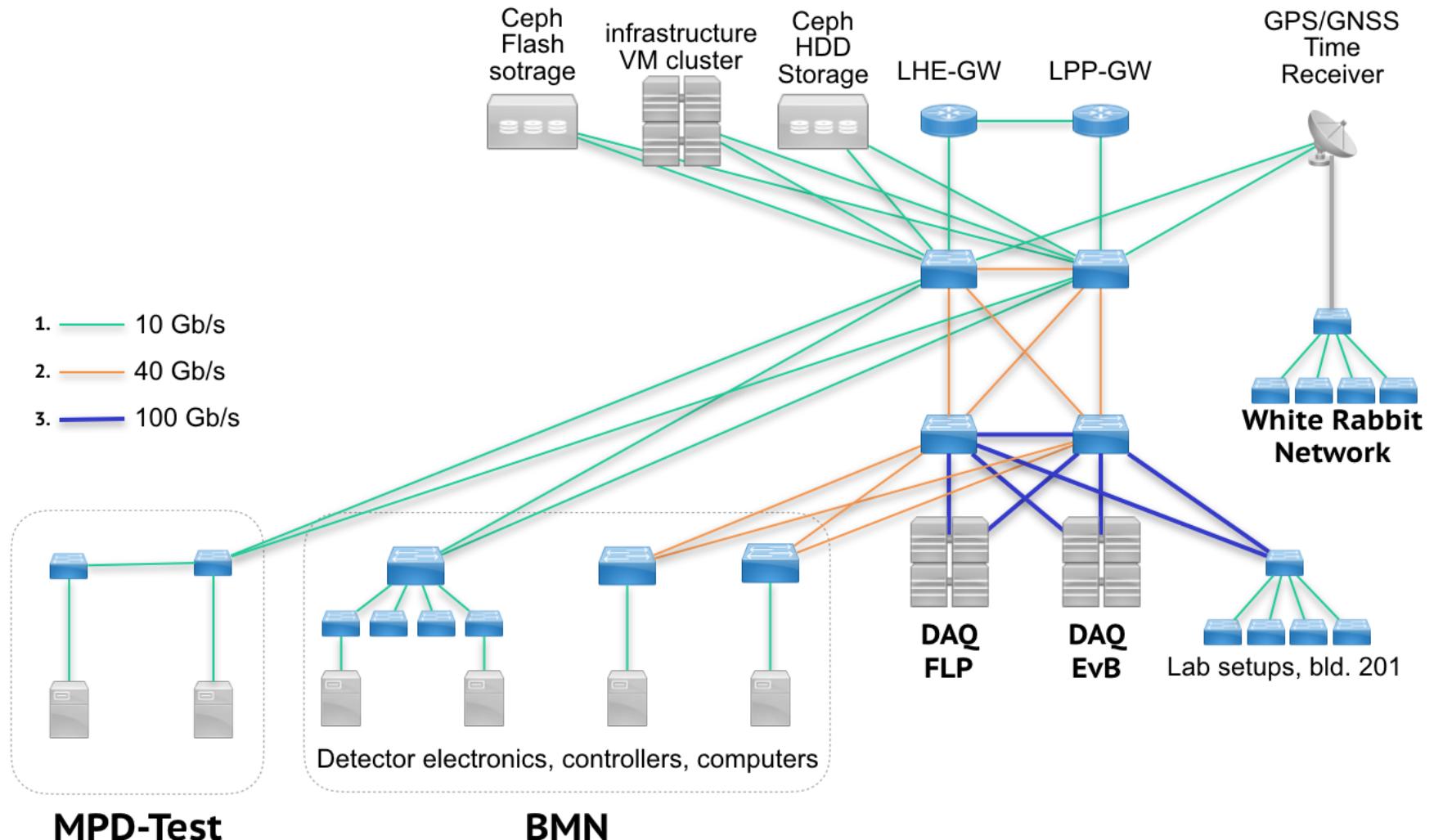
Time Synchronization Measurement



Long-term drift is caused by 25 ps/ $^{\circ}\text{C}$ temperature coefficient of PLL used in TQDC16VS measurement board.

DAQ IT Infrastructure

DAQ Technical Network in 2018



DAQ IT Hardware

FLP, event builder nodes

- ▶ 16 nodes, each equipped with:
- ▶ Two 16-core CPUs (Intel Xeon 2.6 GHz Broadwell)
- ▶ 512 GB RAM (16 GB/core)
- ▶ 2 x 100 Gb/s network

Ceph Flash storage

- ▶ 32 SATA and SAS SSD in 8 nodes
- ▶ 6.5 TB useable space
- ▶ Houses all virtual machine disks

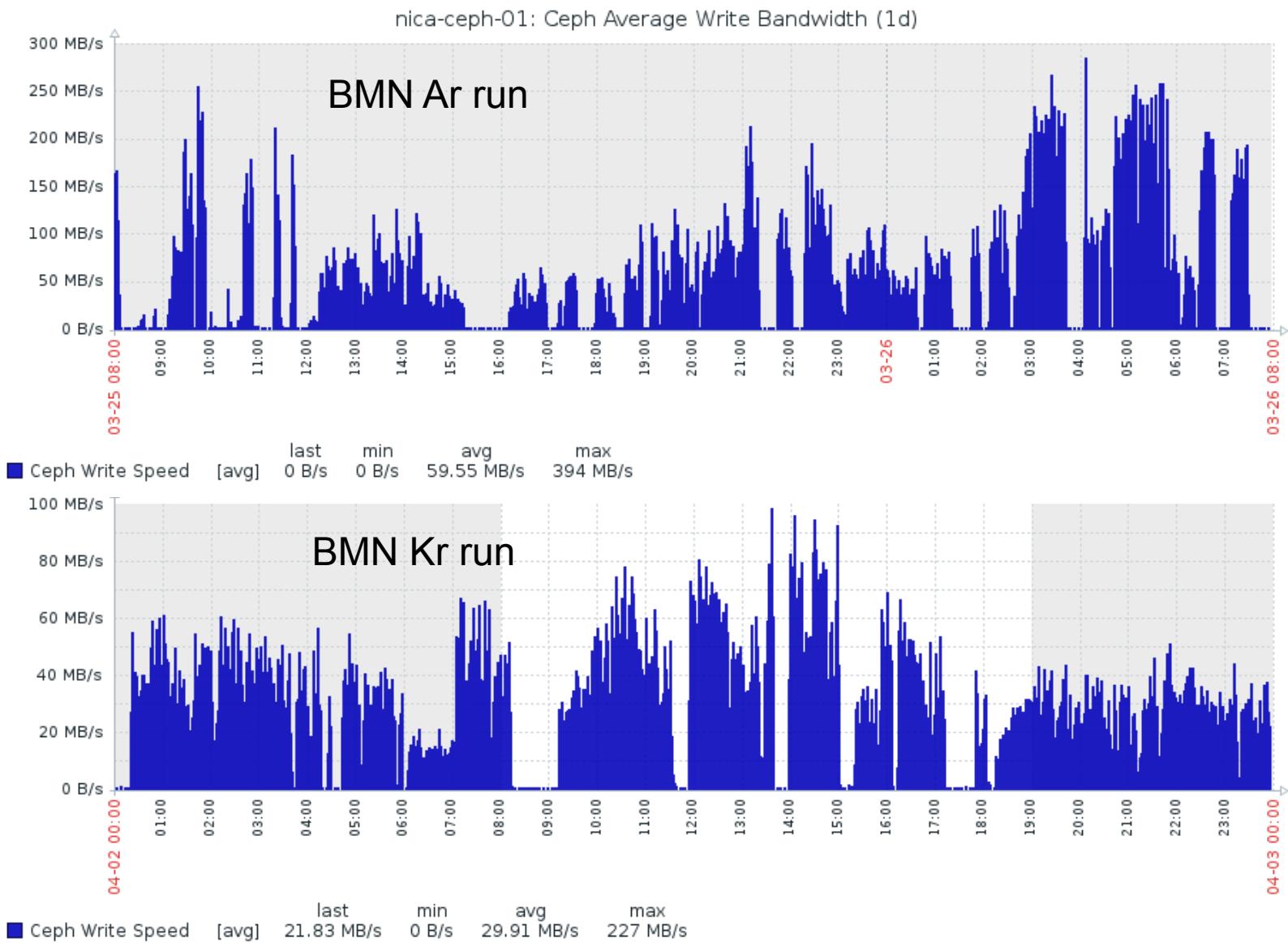
Network

- ▶ Cisco Nexus 5000 / 9000 switches
- ▶ Fault tolerant, redundant topology
- ▶ Bidirectional multicast capable (DAQ software requirement)

Ceph HDD storage

- ▶ 108 disks in 4 nodes
- ▶ 143 TB useable space (3x replicated)
- ▶ 4 GB/s read/write throughput
- ▶ Fault tolerant (multiple HDD failures has occurred while BMN data taking)

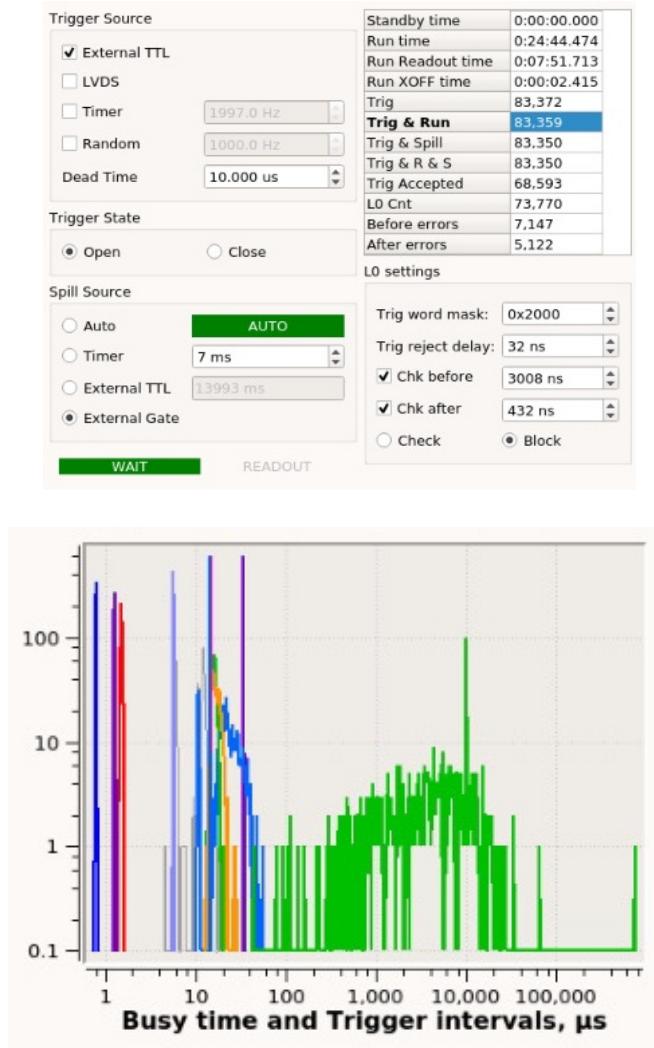
BMN Run 2018 – Storage Write Bandwidth



Thank you!

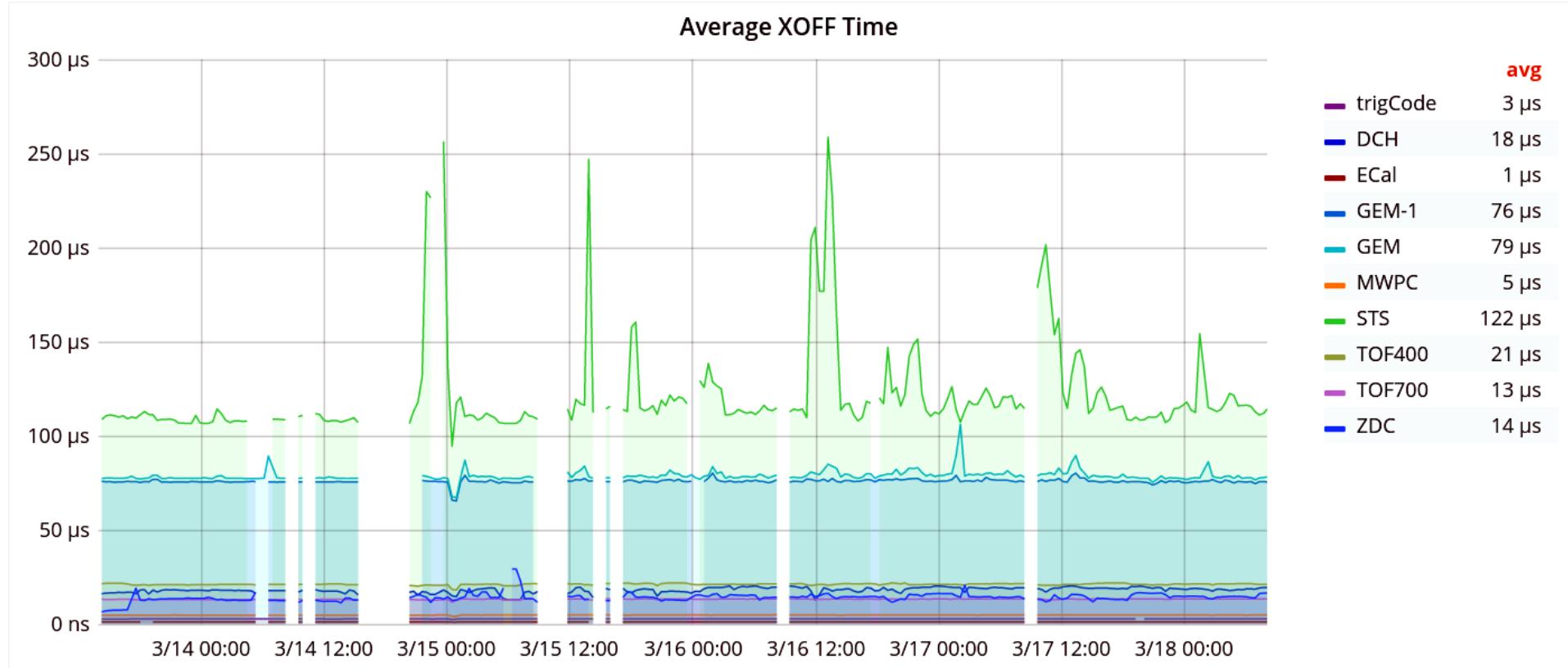
Extra slides

Run Control GUI for UT24VE



- ▶ Run Start/Stop control
- ▶ Subdetector status monitoring
- ▶ 14 busy backpressure channels
- ▶ Hardware histograms:
- ▶ Trigger Time Intervals (Log scale)
- ▶ Busy Time per channel
- ▶ Triggers vs Time plot
- ▶ Live counters
- ▶ Programmable periodic and random test trigger generator

BMN – Mar 2017 run, DAQ busy time



Time Synchronization Measurement

